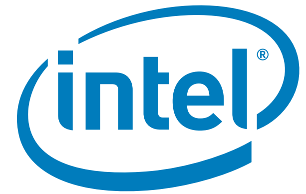


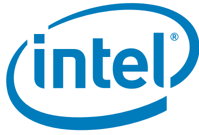
Intel® Core™ i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series

Datasheet- Volume One

This is volume 1 of 2. Refer to document 320766 for Volume 2

September 2009

Document Number: 320765 -001



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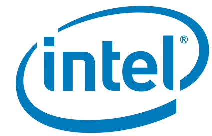
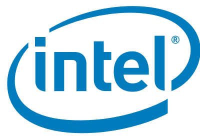


Contents

1 Features Summary ... 10
- 1.1 Introduction ... 10
- 1.2 Processor Feature Details ... 12
  - 1.2.1 Supported Technologies ... 12
- 1.3 Interfaces ... 12
  - 1.3.1 System Memory Support ... 12
  - 1.3.2 PCI Express* ... 13
  - 1.3.3 Direct Media Interface (DMI) ... 14
  - 1.3.4 Platform Environment Control Interface (PECI) ... 15
- 1.4 Power Management Support ... 15
  - 1.4.1 Processor Core ... 15
  - 1.4.2 System ... 15
  - 1.4.3 Memory Controller ... 15
  - 1.4.4 PCI Express* ... 15
  - 1.4.5 DMI ... 15
- 1.5 Thermal Management Support ... 15
- 1.6 Package ... 16
- 1.7 Terminology ... 16
- 1.8 Related Documents ... 18

2 Interfaces ... 20
- 2.1 System Memory Interface ... 20
  - 2.1.1 System Memory Technology Supported ... 20
  - 2.1.2 System Memory Timing Support ... 21
  - 2.1.3 System Memory Organization Modes ... 21
  - 2.1.4 Rules for Populating Memory Slots ... 23
  - 2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA) ... 23
  - 2.1.6 DRAM Clock Generation ... 24
  - 2.1.7 System Memory Pre-Charge Power Down Support Details ... 24
- 2.2 PCI Express Interface ... 24
  - 2.2.1 PCI Express Architecture ... 24
  - 2.2.2 PCI Express Configuration Mechanism ... 26
  - 2.2.3 PCI Express* Ports and Bifurcation ... 27
- 2.3 DMI ... 27
  - 2.3.1 DMI Error Flow ... 27
  - 2.3.2 Processor/PCH Compatibility Assumptions ... 27
  - 2.3.3 DMI Link Down ... 27
- 2.4 Platform Environment Control Interface (PECI) ... 28
- 2.5 Interface Clocking ... 28
  - 2.5.1 Internal Clocking Requirements ... 28

3 Technologies ... 30
- 3.1 Intel® Virtualization Technology (Intel® VT) ... 30
  - 3.1.1 Intel® VT-x Objectives ... 30
  - 3.1.2 Intel VT-x Features ... 31
  - 3.1.3 Intel® VT-d Objectives ... 31
  - 3.1.4 Intel VT-d Features Supported ... 32
  - 3.1.5 Intel VT-d Features Not Supported ... 32
- 3.2 Intel® Trusted Execution Technology (Intel® TXT) ... 32
- 3.3 Intel® Hyper-Threading Technology ... 33
- 3.4 Intel® Turbo Boost Technology ... 33



3.4.1 Intel Turbo Boost Technology Processor Frequency 34

4 Power Management 36

4.1 ACPI States Supported 36

4.1.1 System States 36

4.1.2 Processor Core/Package Idle States 36

4.1.3 Integrated Memory Controller States 37

4.1.4 PCIe Link States 37

4.1.5 DMI States 37

4.1.6 Interface State Combinations 38

4.2 Processor Core Power Management 38

4.2.1 Enhanced Intel SpeedStep® Technology 39

4.2.2 Low-Power Idle States 39

4.2.3 Requesting Low-Power Idle States 41

4.2.4 Core C-states 42

4.2.5 Package C-States 43

4.3 IMC Power Management 46

4.3.1 Disabling Unused System Memory Outputs 46

4.3.2 DRAM Power Management and Initialization 46

4.4 PCIe Power Management 48

4.5 DMI Power Management 48

5 Thermal Management 50

5.1 Thermal Design Power and Junction Temperature 50

5.1.1 Intel Turbo Boost Technology 50

5.1.2 Intel Turbo Boost Technology Thermal Design Considerations and Specifications 50

5.1.3 Idle Power Specifications 52

5.2 Thermal Management Features 52

5.2.1 Processor Core Thermal Features 52

5.2.2 Integrated Memory Controller Thermal Features 57

5.2.3 Platform Environment Control Interface (PECI) 58

6 Signal Description 60

6.1 System Memory Interface 61

6.2 Memory Reference and Compensation 63

6.3 Reset and Miscellaneous Signals 63

6.4 PCI Express Graphics Interface Signals 65

6.5 DMI 65

6.6 PLL Signals 66

6.7 TAP Signals 66

6.8 Error and Thermal Protection 67

6.9 Power Sequencing 68

6.10 Processor Power Signals 69

6.11 Ground and NCTF 70

6.12 Processor Internal Pull Up/Pull Down 70

7 Electrical Specifications 72

7.1 Power and Ground Pins 72

7.2 Decoupling Guidelines 72

7.2.1 Voltage Rail Decoupling 72

7.3 Processor Clocking (BCLK, BCLK#) 72

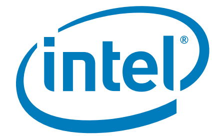
7.3.1 PLL Power Supply 72

7.4 Voltage Identification (VID) 73

7.5 Reserved or Unused Signals 77

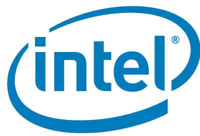
7.6 Signal Groups 78

7.7 Test Access Port (TAP) Connection 80



7.8 Absolute Maximum and Minimum Ratings 81
7.9 Storage Conditions Specifications 81
7.10 DC Specifications 82
7.10.1 Voltage and Current Specifications 83
7.10.2 V_{CC} Validation 90
7.10.3 Uncore Voltage Validation 90
7.11 Platform Environmental Control Interface (PECI) DC Specifications 91
7.11.1 DC Characteristics 91
7.11.2 Input Device Hysteresis 92

8 Processor Pin and Signal Information 93
8.1 Processor Pin Assignments 93
8.2 Package Mechanical Information 123

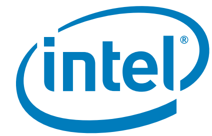


Figures

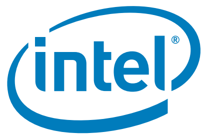
1 Intel® Core™ i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and Core i7-700 Mobile Processor Series Platform Diagram 11
2 Intel Flex Memory Technology Operation 22
3 Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes 23
4 PCI Express Layering Diagram 25
5 Packet Flow through the Layers 25
6 PCI Express-Related Register Structures 26
7 Idle Power Management Breakdown of the Processor Cores 40
8 Thread and Core C-State Entry and Exit 40
9 Package C-State Entry and Exit 44
10 Frequency and Voltage Ordering 53
11 Active V_{CC} and I_{CC} Loadline (PSI# Asserted) 84
12 Active V_{CC} and I_{CC} Loadline (PSI# Not Asserted) 85
13 Input Device Hysteresis 92
14 rPGA988A Pinmap (Top View, Upper-Left Quadrant) 94
15 rPGA988A Pinmap (Top View, Upper-Right Quadrant) 95
16 rPGA988A Pinmap (Top View, Lower-Left Quadrant) 96
17 rPGA988A Pinmap (Top View, Lower-Right Quadrant) 97
18 Intel Core i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series rPGA Mechanical Package (Sheet 1 of 2) 123
19 Intel Core i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series rPGA Mechanical Package (Sheet 2 of 2) 124

Tables

1 Supported SO-DIMM Module Configurations1 20
2 DDR3 System Memory Timing Support 21
3 Reference Clocks 28
4 System States 36
5 Processor Core/Package State Support 36
6 Integrated Memory Controller States 37
7 PCIe Link States 37
8 DMI States 37
9 G, S and C State Combinations 38
10 Coordination of Thread Power States at the Core Level 41
11 P_LVLx to MWAIT Conversion 41
12 Coordination of Core Power States at the Package Level 44
13 Targeted Memory State Conditions 47
14 Intel Core i7-900 Mobile Processor Extreme Edition Series Thermal Power Specification 51
15 Intel Core i7-800 Mobile Processor Series Thermal Power Specification 51
16 Intel Core i7-700 Mobile Processor Series Thermal Power Specification 51
17 Intel Core i7-900 Mobile Processor Extreme Edition Series Idle Power 52
18 Intel Core i7-800 and i7-700 Mobile Processor Series Idle Power 52
19 Signal Description Buffer Types 60
20 Memory Channel A 61
21 Memory Channel B 62
22 Memory Reference and Compensation 63
23 Reset and Miscellaneous Signals 63
24 PCI Express Graphics Interface Signals 65
25 DMI - Processor to PCH Serial Interface 65
26 PLL Signals 66
27 TAP Signals 66
28 Error and Thermal Protection 67
29 Power Sequencing 68



30 Processor Power Signals 69
31 Ground and NCTF 70
32 Processor Internal Pull Up/Pull Down 70
33 Voltage Identification Definition 74
34 Market Segment Selection Truth Table for MSID[2:0] 77
35 Signal Groups1 78
36 Processor Absolute Minimum and Maximum Ratings 81
37 Storage Condition Ratings 82
38 Processor Core (VCC) Active and Idle Mode DC Voltage and Current Specifications 83
39 Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications 86
40 DDR3 Signal Group DC Specifications 87
41 Control Sideband and TAP Signal Group DC Specifications 88
42 PCI Express DC Specifications 89
43 PECI DC Electrical Limits 91
44 Pins Unused by the Intel Core i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series on the rPGA988A Package 93
45 rPGA988A Processor Pin List by Pin Name 98
46 rPGA988A Processor Pin List by Pin Number 110



Revision History

Revision Number	Description	Revision Date
-001	Initial release	September 2009

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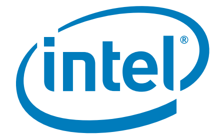
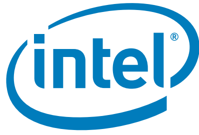




1 Features Summary

1.1 Introduction

The Intel Core i7-900 mobile processor extreme edition series, Intel Core i7-800 and i7-700 mobile processor series are the next generation of 64-bit, multi-core mobile processors built on 45-nanometer process technology. Based on the low-power/high-performance Nehalem micro-architecture, these processors are designed for a two-chip platform consisting of a processor and an Intel 5 Series Chipset. The Core i7 family of mobile processors features four processor cores, an integrated memory controller (IMC), and an integrated I/O (IIO) (PCI Express* and DMI) on a single-silicon die. This single-die solution is known as a monolithic processor.

This document provides DC and AC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, thermal specifications, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Note: Throughout this document, the Intel Core i7-900 mobile processor extreme edition series, Intel Core i7-800 and i7-700 mobile processor series may be referred to as "processor".

Note: Throughout this document, the Intel Core i7-900 mobile processor extreme edition series refers to the Intel Core i7-920XM processor.

Note: Throughout this document, the Intel Core i7-800 mobile processor series refers to the Intel Core i7-820QM processor.

Note: Throughout this document, the Intel Core i7-700 mobile processor series refers to the Intel Core i7-720QM processor.

Note: Throughout this document, the Intel 5 Series Chipset may also be referred to as the "platform controller hub" or "PCH"

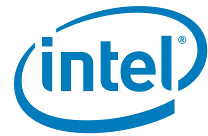


Figure 1. Intel® Core™ i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and Core i7-700 Mobile Processor Series Platform Diagram

Quad Core Processor with Integrated Memory Controller

Processor

Discrete Graphics (PEG)

PCI Express* x16

OR

PCI Express* x 8

PCI Express* x 8

1066/1333 MT/s

2 Channels
1 SO-DIMM / Channel

DDR3 SO-DIMMs

DMI2
(x4)

Intel® Management Engine

Mobile Intel® 5 Series Chipset (PCH)

Serial ATA

6 Ports
3 Gb/s

USB 2.0

14 Ports

WiMax

Intel® HD Audio

Dual Channel NAND Interface

SMBus 2.0

Controller Link 1

SPI Flash

SPI

PCI

PCI

PCI Express*

WiFi

Gigabit Network Connection

FWH

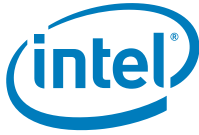
LPC

8 PCI Express* x1 Ports (2.5 GT/s)

Super I/O

PECI

GPIO



1.2 Processor Feature Details

- Four execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data second-level cache (L2) for each core
- Up to 8-MB shared instruction/data last-level cache (L3), shared among all cores

1.2.1 Supported Technologies

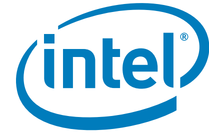
- Intel® Virtualization Technology (Intel® VT-x)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Supplemental Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology

Note: Some technologies may not be enabled on all processor SKUs. Refer to the Processor Specification Update for details.

1.3 Interfaces

1.3.1 System Memory Support

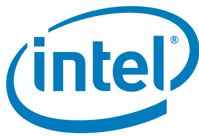
- One or two channels of DDR3 memory with a maximum of one SO-DIMM per channel
- Single- and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- Memory DDR3 data transfer rates of 1066 MT/s and 1333 MT/s
- 64-bit wide channels
- DDR3 I/O Voltage of 1.5 V
- Non-ECC, unbuffered DDR3 SO-DIMMs only
- Theoretical maximum memory bandwidth of:
  - 17.1 GB/s in dual-channel mode assuming DDR3 1066 MT/s
  - 21.3 GB/s in dual-channel mode assuming DDR3 1333 MT/s
- 1-Gb, and 2-Gb DDR3 DRAM technologies are supported for x8 and x16 devices.
- Using 2-Gb device technologies, the largest memory capacity possible is 8 GB, assuming dual-channel mode with two x8, double-sided, un-buffered, non-ECC, SO-DIMM memory configuration.
- Up to 32 simultaneous open pages, 16 per channel (assuming 4 Ranks of 8 Bank Devices)



- Memory organizations:
  - — Single-channel modes
  - — Dual-channel modes - Intel® Flex Memory Technology:
    Dual-channel symmetric (Interleaved)
    Dual-channel asymmetric
- Command launch modes of 1n/2n
- On-Die Termination (ODT)
- Intel® Fast Memory Access (Intel® FMA):
  - — Just-in-Time Command Scheduling
  - — Command Overlap
  - — Out-of-Order Scheduling

1.3.2 PCI Express*

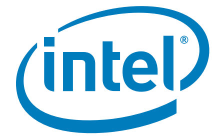
- Fully-compliant to the *PCI Express Base Specification Revision 2.0*.
- One, 16-lane PCI Express port configurable to two, 8-lane PCI Express ports intended for graphics attach.
- 2.5 GT/s and 5.0 GT/s PCI Express* frequencies are supported.
- The raw bit-rate on the data pins is 5.0 GB/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface is 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s for x16.
- Hierarchical PCI-compliant configuration mechanism for downstream devices.
- Traditional PCI style traffic (asynchronous snooped, PCI ordering).
- PCI Express extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as "extended configuration space."
- PCI Express Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset.
- Traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering).
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0:
  - — PCI Express Port 0 -> PCI Express Port 1
  - — PCI Express Port 1 -> PCI Express Port 0
  - — DMI -> PCI Express Port 0
  - — DMI -> PCI Express Port 1
  - — PCI Express Port 0 -> DMI
  - — PCI Express Port 1 -> DMI
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).



- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are non-zero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Re-issues configuration cycles that have been previously completed with the Configuration Retry status.
- PCI Express reference clock is 100-MHz differential clock buffered out of system clock generator.
- Power Management Event (PME) functions.
- Dynamic lane numbering reversal as defined by the *PCI Express Base Specification*.
- Dynamic frequency change capability (2.5 GT/s - 5.0 GT/s)
- Dynamic width capability
- Supports Half Swing "low-power/low-voltage" mode.
- Message Signaled Interrupt (MSI and MSI-X) messages
- Polarity inversion

1.3.3 Direct Media Interface (DMI)

- Compliant to Direct Media Interface second generation (DMI2).
- Four lanes in each direction.
- 2.5 GT/s point-to-point DMI interface to PCH is supported.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s when DMI x4.
- Shares 100-MHz PCI Express reference clock.
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Supports the following traffic types to or from the PCH:
  - DMI -> PCI Express Port 0 write traffic
  - DMI -> PCI Express Port 1 write traffic
  - DMI -> DRAM
  - DMI -> processor core (Virtual Legacy Wires (VLWs), Resetwarn, or MSIs only)
  - Processor core -> DMI
- APIC and MSI interrupt messaging support:
  - Message Signaled Interrupt (MSI and MSI-X) messages
- Downstream SMI, SCI and SERR error indication.
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters.
- DC coupling – no capacitors between the processor and the PCH.



- Polarity inversion.
- PCH end-to-end lane reversal across the link.
- Supports Half Swing "low-power/low-voltage."

1.3.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master (the PCH).

1.4 Power Management Support

1.4.1 Processor Core

- Full support of ACPI C-states as implemented by the following processor C-states:
  - C0, C1, C1E, C3, C6
- Enhanced Intel SpeedStep® Technology

1.4.2 System

- S0, S3, S4, S5

1.4.3 Memory Controller

- Conditional self-refresh (Intel® Rapid Memory Power Management (Intel® RMPM))
- Dynamic power-down

1.4.4 PCI Express*

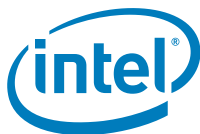
- L0s and L1 ASPM power management capability

1.4.5 DMI

- L0s and L1 ASPM power management capability

1.5 Thermal Management Support

- Digital Thermal Sensor
- Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Fan speed control with DTS

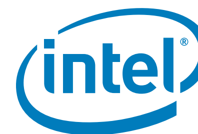


1.6 Package

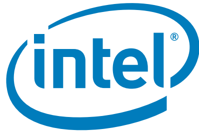
- The Intel Core i7-900 mobile processor extreme edition series, Intel Core i7-800 and i7-700 mobile processor series are available on a 37.5 x 37.5 mm rPGA package (rPGA988A)

1.7 Terminology

Term	Description
DDR3	Third-generation Double Data Rate SDRAM memory technology
DP	DisplayPort*
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Intel® DPST	Intel® Display Power Saving Technology
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
(G)MCH	Legacy component - Graphics Memory Controller Hub
ICH	The legacy I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the legacy (G)MCH over a proprietary interconnect called DMI.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® TXT	Intel® Trusted Execution Technology
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
ITPM	Integrated Trusted Platform Module
IOV	I/O Virtualization
LCD	Liquid Crystal Display



Term	Description
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
Nehalem	Intel's 45-nm processor design, follow-on to the 45-nm Penryn design.
PCH	Platform Controller Hub. The new, 2009 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features. The PCH may also be referred to using the name (Mobile) Intel® 5 Series Chipset
PECI	Platform Environment Control Interface.
PEG	PCI Express* Graphics. External Graphics using PCI Express Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications.
Processor	The 64-bit, single-core or multi-core component (package).
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant.
TDP	Thermal Design Power.
V_{CC}	Processor core power supply.
V_{SS}	Processor ground.
V_{TT}	L3 shared cache, memory controller, and processor I/O power rail.
V_{DDQ}	DDR3 power rail.
VLD	Variable Length Decoding.
x1	Refers to a Link or Port with one Physical Lane.
x4	Refers to a Link or Port with four Physical Lanes.
x8	Refers to a Link or Port with eight Physical Lanes.
x16	Refers to a Link or Port with sixteen Physical Lanes.



1.8 Related Documents

Refer to the following documents for additional information.

Document	Document Number/ Location
Intel® Core™ i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series Datasheet - Volume Two	intel.com/products/ processor/corei7/mobile/ techdocs.htm
Intel® Core™ i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series Specification Update	intel.com/products/ processor/corei7/mobile/ techdocs.htm
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/ specifications
PCI Express Base Specification 2.0	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/ products/processor/ manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

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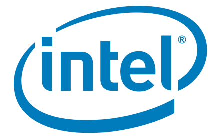


2 Interfaces

This chapter describes the interfaces supported by the processor.

2.1 System Memory Interface

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3 protocols with two, independent, 64-bit wide channels each accessing one SO-DIMM. It supports a maximum of one, unbuffered non-ECC DDR3 SO-DIMM per-channel thus allowing up to two device ranks per-channel.

DDR3 Data Transfer Rates:

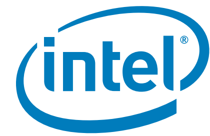
— 1066 MT/s (PC3-8500), and 1333 MT/s (PC3-10600)

- DDR3 SO-DIMM Modules:
  - — Raw Card A – double-sided x16 unbuffered non-ECC
  - — Raw Card B – single-sided x8 unbuffered non-ECC
  - — Raw Card C – single-sided x16 unbuffered non-ECC
  - — Raw Card D – double-sided x8 (stacked) unbuffered non-ECC
  - — Raw Card F – double-sided x8 (planar) unbuffered non-ECC
- DDR3 DRAM Device Technology:
  - — Standard 1-Gb, and 2-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

Table 1. Supported SO-DIMM Module Configurations[1]

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/ Col Address Bits	# of Banks Inside DRAM	Page Size
A	1 GB	1 Gb	64 M x 16	8	2	13/10	8	8K
A	2 GB	2 Gb	128 M x 16	8	2	14/10	8	8K
B	1 GB	1 Gb	128 M x 8	8	1	14/10	8	8K
B	2 GB	2 Gb	256 M x 8	8	1	15/10	8	8K
C	512 MB	1 Gb	64 M x 16	4	1	13/10	8	8K
C	1 GB	2 Gb	128 M x 16	4	1	14/10	8	8K
D[2]	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K
F	2 GB	1 Gb	128 M x 8	16	2	14/10	8	8K
F	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K

NOTES:
1. System memory configurations are based on availability and are subject to change.
2. Only Raw Card D SO-DIMMS at 1067 MT/s are supported.



2.1.2 System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Table 2. DDR3 System Memory Timing Support

<table>
<tr><th>Transfer Rate (MT/s)</th><th>tCL (tCK)</th><th>tRCD (tCK)</th><th>tRP (tCK)</th><th>CWL (tCK)</th><th>CMD Mode</th><th>Notes</th></tr>
<tr><td rowspan="2">1066</td><td>7</td><td>7</td><td>7</td><td rowspan="2">6</td><td rowspan="2">1n and 2n</td><td rowspan="2">1</td></tr>
<tr><td>8</td><td>8</td><td>8</td></tr>
<tr><td>1333</td><td>9</td><td>9</td><td>9</td><td>7</td><td>2n</td><td>1</td></tr>
</table>

NOTES:
1. System memory timing support is based on availability and is subject to change.

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the SO-DIMM Modules are populated in each memory channel, a number of different configurations can exist.

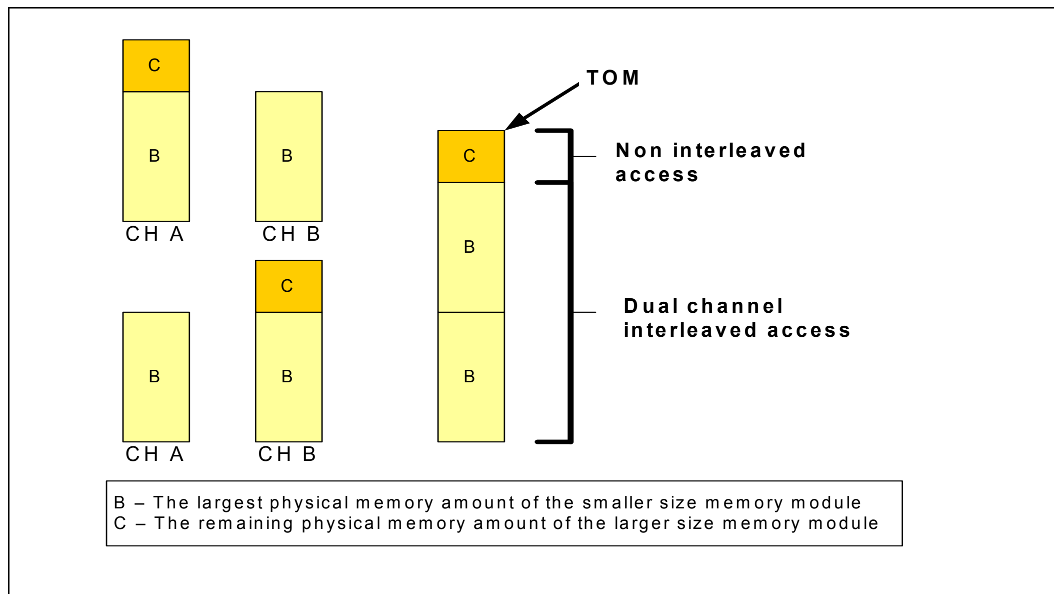
2.1.3.1 Single-Channel Mode

In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B SO-DIMM connectors are populated in any order, but not both.

2.1.3.2 Dual-Channel Mode - Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. This mode combines the advantages of the Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes. Memory is divided into a symmetric and a asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Figure 2. Intel Flex Memory Technology Operation



2.1.3.2.1 Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B SO-DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

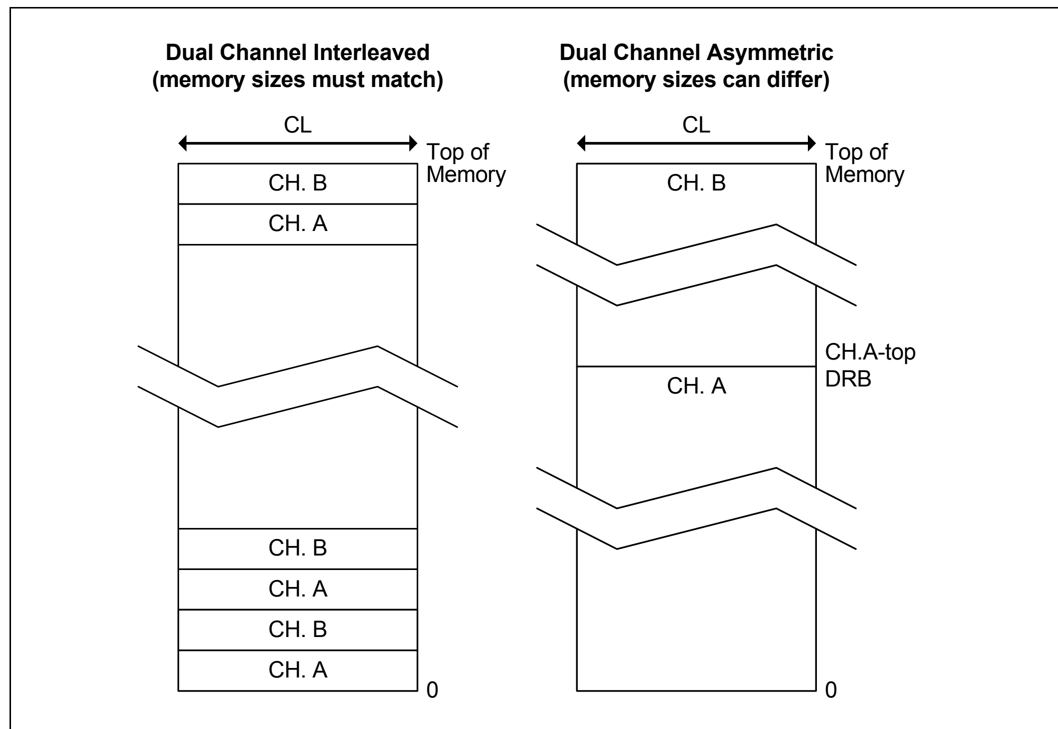
Note: The DRAM device technology and width may vary from one channel to the other.

2.1.3.2.2 Dual-Channel Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start at the bottom of Channel A and stay there until the end of the highest rank in Channel A, and then addresses continue from the bottom of Channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth is limited to a single channel.

This mode is used when Intel Flex Memory Technology is disabled and both Channel A and Channel B SO-DIMM connectors are populated in any order with the total amount of memory in each channel being different.

Figure 3. Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes



2.1.4 Rules for Populating Memory Slots

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports only one SO-DIMM connector per channel. For dual-channel modes both channels must have an SO-DIMM connector populated. For single-channel mode, only a single-channel can have an SO-DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

2.1.5.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

2.1.5.2 Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.1.5.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 DRAM Clock Generation

Every supported SO-DIMM has two differential clock pairs. There are total of four clock pairs driven directly by the processor to two SO-DIMMs.

2.1.7 System Memory Pre-Charge Power Down Support Details

The IMC supports and enables slow exit DDR3 DRAM Device pre-charge power down DLL control. During a pre-charge power down, a slow exit is where the DRAM device DLL is disabled after entering pre-charge power down for potential power savings.

2.2 PCI Express Interface

This section describes the PCI Express interface capabilities of the processor. See the *PCI Express Base Specification* for details of PCI Express.

The processor has two PCI Express controllers which can support either one external x16 PCI Express Graphics Device or two external x8 PCI Express Graphics Devices. The primary and secondary PCI Express Graphics ports are referred to as PEG 0 and PEG 1, respectively.

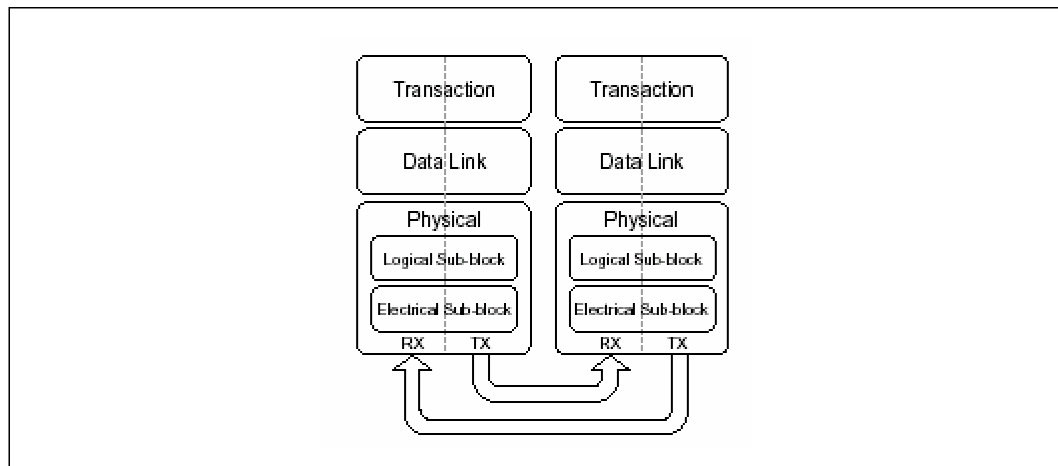
2.2.1 PCI Express Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial recovered clock speed of 1.25 GHz results in 2.5 Gb/s/direction which provides a 250 MB/s communications channel in each direction (500 MB/s total). That is close to twice the data rate of classic PCI. The fact that 8b/10b encoding is used accounts for the 250 MB/s where quick calculations would imply 300 MB/s. The external graphics ports support Gen2 speed as well. At 5.0 GT/s, Gen 2 operation results in twice as much bandwidth per lane as compared to Gen 1 operation. When operating with two PCIe controllers, each controller can be operating at either 2.5 GT/s or 5.0 GT/s.

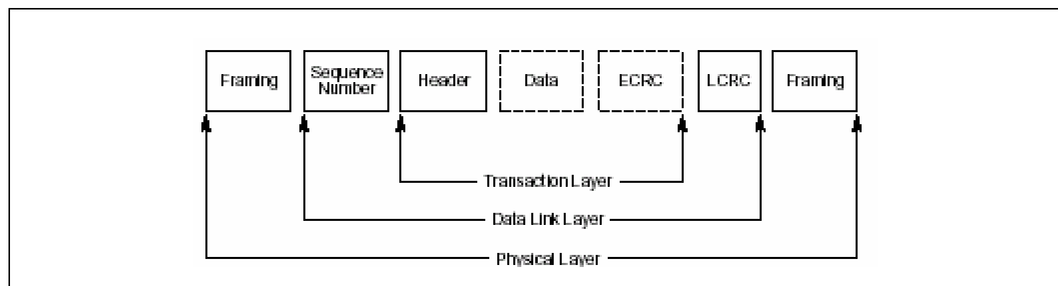
The PCI Express architecture is specified in three layers: Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to Figure 4 for the PCI Express Layering Diagram.

Figure 4. PCI Express Layering Diagram



PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 5. Packet Flow through the Layers



2.2.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.1.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets which are used for Link management functions.

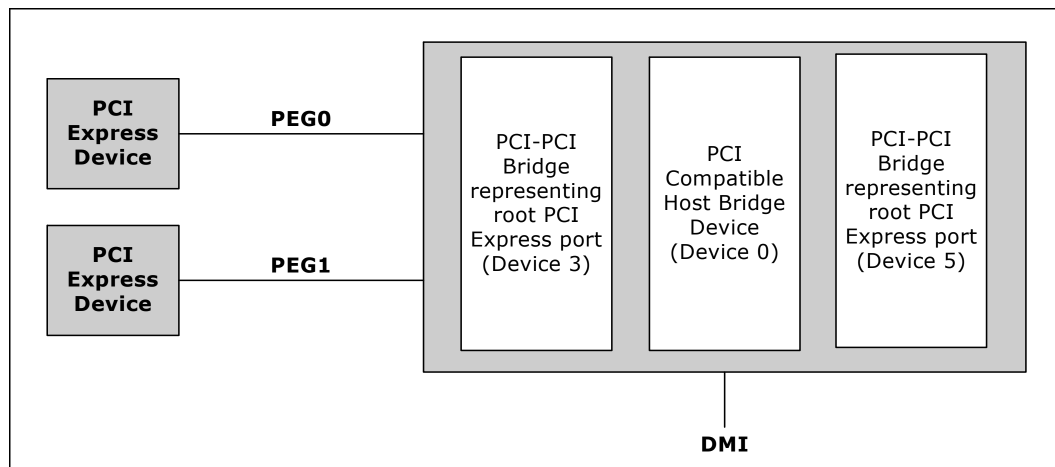
2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express Configuration Mechanism

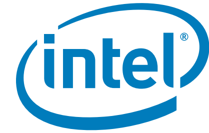
The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 6. PCI Express-Related Register Structures



PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the *Conventional PCI Specification*. PCI Express configuration space is divided into a PCI-compatible region (which consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (which consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the PCI Express Enhanced Configuration Mechanism section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the *PCI Express Base Specification* for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.



2.2.3 PCI Express* Ports and Bifurcation

The PCI Express Interface on the processor is a single 16 lane (x16) port that can be

- configured at narrower widths.
- bifucated into two x8 ports that may train to narrower widths.

The PCI Express port is designed to be compliant with the PCI Express Base Specification revision 2.0.

2.2.3.1 PCI Express* Bifurcated Mode

When bifurcated, the signals which had previously been assigned to lanes 15:8 of the single x16 Primary port are reassigned to lanes 7:0 of the x8 Secondary Port. This assignment applies whether the lane numbering is reversed or not. The controls for the Secondary port and the associated virtual PCI-to-PCI bridge can be found in PCI Device 5. Please refer to Table 6-5 for port bifurcation configuration settings and supported configurations.

PCI Express port 0 is mapped to PCI Device 3 and PCI Express port 1 is mapped to PCI Device 5. When the port is not bifurcated, Device 5 is hidden from the discovery mechanism used in PCI enumeration, such that configuration of the device is neither possible nor necessary.

2.3 DMI

DMI connects the processor and the PCH chip-to-chip. DMI2 is supported. The DMI is similar to a four-lane PCI Express supporting up to 1 GB/s of bandwidth in each direction.

Note: Only DMI x4 configuration is supported.

2.3.1 DMI Error Flow

DMI can only generate SERR in response to errors, never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

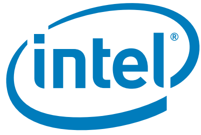
2.3.2 Processor/PCH Compatibility Assumptions

The processor is compatible with the PCH and is not compatible with any previous (G)MCH or ICH products.

2.3.3 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.



2.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (processor) and a PECI master, usually the PCH. The processor implements a PECI interface to:

- Allow communication of processor thermal and other information to the PECI master.
- Read averaged Digital Thermal Sensor (DTS) values for fan speed control.

2.5 Interface Clocking

2.5.1 Internal Clocking Requirements

Table 3. Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI

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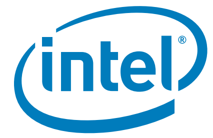


3 Technologies

3.1 Intel® Virtualization Technology (Intel® VT)

Intel Virtualization Technology (Intel VT) is the technology that makes a single system appear as multiple, independent systems to software. This allows multiple, independent operating systems to be running simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel Virtualization Technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VT-d) adds chipset hardware implementation to support and improve I/O virtualization performance and robustness.

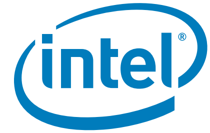
Intel VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at http://www.intel.com/products/processor/manuals/index.htm.

The Intel VT-d spec and other Intel VT documents can be referenced at http://www.intel.com/technology/virtualization/index.htm.

3.1.1 Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that they will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.



3.1.2 Intel VT-x Features

The processor core supports the following new Intel VT-x features:

- Extended Page Tables (EPT)
  - — Hardware-assisted page table virtualization.
  - — Eliminates VM exits from guest OS to the VMM for shadow page-table maintenance.
- Virtual Processor IDs (VPID)
  - — Ability to assign a VM ID to tag processor core hardware structures (e.g., TLBs).
  - — Avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - — Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
  - — The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees.
- Descriptor-Table Exiting
  - — Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - — A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.3 Intel® VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system, or there can be multiple operating system instances running on the same system, offering benefits such as system consolidation, legacy migration, activity partitioning or security.

3.1.4 Intel VT-d Features Supported

The processor supports the following Intel VT-d features:

- 48-bit max guest address width and 36-bit max host address width for non-isoch traffic in UP profiles
- 39-bit max guest address width and 36-bit max host address width for isoch traffic. Isoch traffic will always be associated with Intel® HD Audio and will not be associated with VCp traffic.
- Support for 4-K page sizes only.
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults,
  - Support for fault collapsing based on Requester ID, OS-visible Intel® ME PCI devices
- Support for both leaf and non-leaf caching.
- Support for boot protection of default page table.
- Support for non-caching of invalid page table entries.
- Support for hardware based flushing of translated but pending writes and pending reads on IOTLB invalidation.
- Support for page-selective IOTLB invalidation.
- Support for queue-based invalidation interface
- Support for Intel VT-d read prefetching/snarfing, e.g., translations within a cacheline are stored in an internal buffer for reuse for subsequent transactions
- Support for ARI (Alternative Requester ID - a PCI SIG ECR for increasing the function number count in a PCIe device) to support IOV devices.

3.1.5 Intel VT-d Features Not Supported

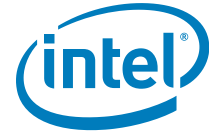
The following features are not supported by the processor with Intel VT-d:

- No support for PCI-SIG endpoint caching (ATS).
- No support for interrupt remapping.
- No support for advance fault reporting.
- No support for super pages.
- No support for 1 or 2 level page walks for isoch remap engine and 1, 2, or 3 level walks for non-isoch remap engine.
- No support for Intel VT-d translation bypass address range (such usage models need to be resolved with VMM help in setting up the page tables correctly).

3.2 Intel® Trusted Execution Technology (Intel® TXT)

Intel TXT defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.



Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

3.3 Intel® Hyper-Threading Technology

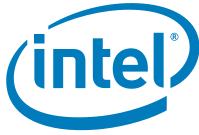
The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), which allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled via the BIOS and requires operating system support. For enabling details, please refer to the *RS-Nehalem Family BIOS Writer's Guide* for enabling details.

Intel recommends enabling Hyper-Threading Technology with Microsoft Windows Vista*, Microsoft Windows* XP Professional/Windows* XP Home, and disabling Hyper-Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see http://www.intel.com/products/ht/hyperthreading_more.htm.

3.4 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating frequency if it is operating below power, temperature, and current limits. Maximum frequency is dependant on the SKU an number of active cores. No special hardware support is necessary for Intel Turbo Boost Technology. It should be enabled in the BIOS for the processor to operate with maximum performance.

Note: Intel Turbo Boost Technology may not be available on all SKUs. Refer to the processor specification update for details.



3.4.1 Intel Turbo Boost Technology Processor Frequency

The processor's rated frequency assumes that all execution cores are running an application at the thermal design power (TDP). However, under typical operation, not all cores are active. Therefore most applications are consuming less than the TDP at the rated frequency. To take advantage of the available TDP headroom, the active cores can increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:

- The number of cores operating in the C0 state.
- The estimated current consumption.
- The estimated power consumption.
- The temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Boost Technology processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states refer to Chapter 4, "Power Management".

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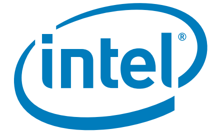


4 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- Integrated Memory Controller (IMC)
- PCI Express
- Direct Media Interface (DMI)

4.1 ACPI States Supported

The ACPI states supported by the processor are described in this section.

4.1.1 System States

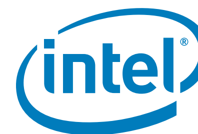
Table 4. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power (AC and battery) removed from system.

4.1.2 Processor Core/Package Idle States

Table 5. Processor Core/Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C1E	AutoHALT state with lowest frequency and voltage operating point.
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.



4.1.3 Integrated Memory Controller States

Table 6. Integrated Memory Controller States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed.
Active Power down	CKE deasserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE deasserted using device self-refresh.

4.1.4 PCIe Link States

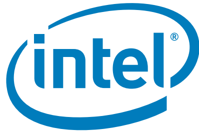
Table 7. PCIe Link States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

4.1.5 DMI States

Table 8. DMI States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.



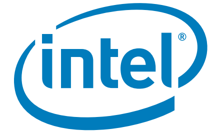
4.1.6 Interface State Combinations

Table 9. G, S and C State Combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6	Deep Power Down	On	Deep Power Down
G1	S3	Power off		Off, except RTC	Suspend to RAM
G1	S4	Power off		Off, except RTC	Suspend to Disk
G2	S5	Power off		Off, except RTC	Soft Off
G3	NA	Power off		Power off	Hard off

4.2 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.



4.2.1 Enhanced Intel SpeedStep® Technology

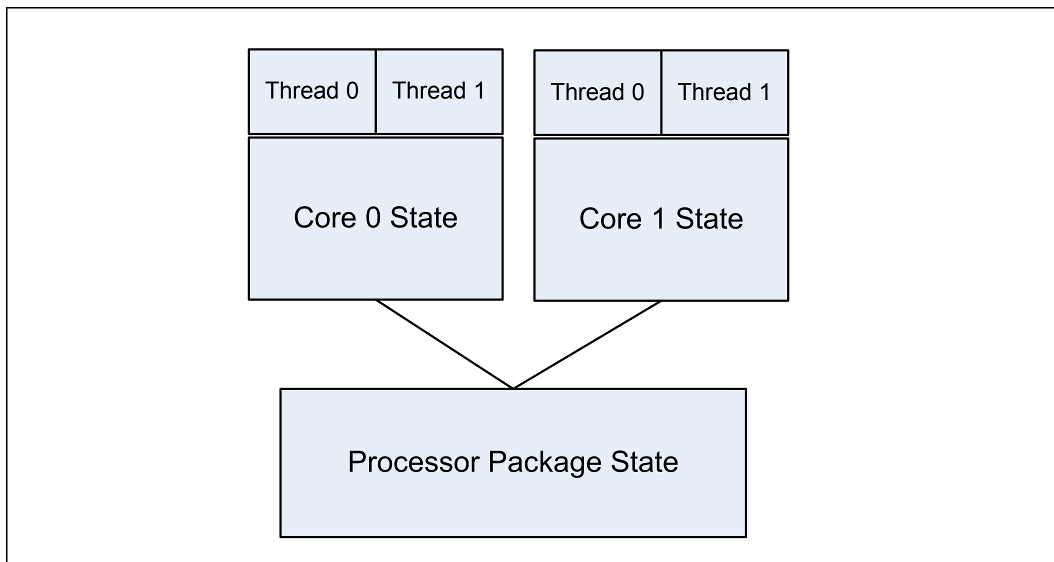
The following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor cores.
    - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps to an optimized voltage. This voltage is signaled by the VID[6:0] pins to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
    - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the VID[6:0] pins.
    - All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested amongst all active cores is selected.
    - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.2 Low-Power Idle States

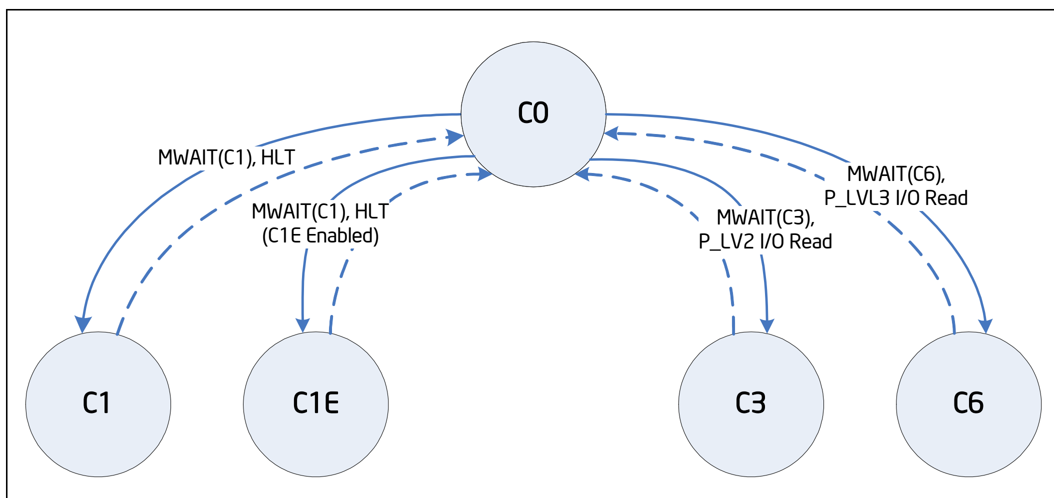
When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Figure 7. Idle Power Management Breakdown of the Processor Cores



Entry and exit of the C-States at the thread and core level are shown in Figure 8.

Figure 8. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

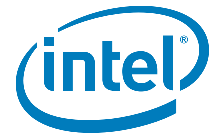


Table 10. Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1 C0	Thread 1 C1	Thread 1 C3	Thread 1 C6
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

NOTE: If enabled, the core C-state will be C1E if all actives cores have also resolved a core C1 state or higher.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions via I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

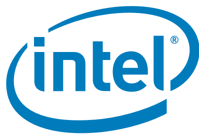
Note: The P_LVLx I/O Monitor address needs to be set up before using the P_LVLx I/O read interface. Each P-LVLx is mapped to the supported MWAIT(Cx) instruction as follows.

Table 11. P_LVLx to MWAIT Conversion

P_LVLx	MWAIT(Cx)	Notes
P_LVL2	MWAIT(C3)	C3 state
P_LVL3	MWAIT(C6)	C6. No sub-states allowed.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range does not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT substates cannot be defined. The MWAIT substate is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature which triggers a wakeup on an interrupt even if interrupts are masked by EFLAGS.IF.



4.2.4 Core C-states

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (e.g., Thread 0 requests C1E while Thread 1 requests C3, resulting in a core C1E state). See Table 9.
- A core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered via an MWAIT instruction
- For core C1/C1E, and core C3, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- For core C6, an interrupt coming into either thread wakes both threads into C0 state.
- Any interrupt coming into the processor package may wake any core.

4.2.4.1 Core C0 State

The normal operating state of a core where code is being executed.

4.2.4.2 Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.*

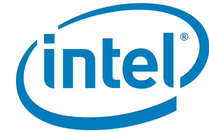
While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see "Package C1/C1E".

4.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

4.2.4.4 Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.



4.2.4.5 C-State Auto-Demotion

In general, deeper C-states such as C6 have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore incorrect or inefficient usage of deeper C-states have a negative impact on battery life. In order to increase residency and improve battery life in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C6 to C3
- C6/C3 To C1

The decision to demote a core from C6 to C3 or C3/C6to C1 is based on each core's immediate residency history. Upon each core C6 request, the core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C3/C6. Each option can be run concurrently or individually.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

The processor supports C0, C1/C1E, C3, and C6 package idle power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
  - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor. If given permission, Clarksfield will put the DRAM into self-refresh in the package C3 and C6 states. For more information see "Conditional Self-Refresh" on page 47
- For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected. If DRAM was allowed to go into self-refresh in package C3 or C6 state, it will be taken out of self-refresh. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.

- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

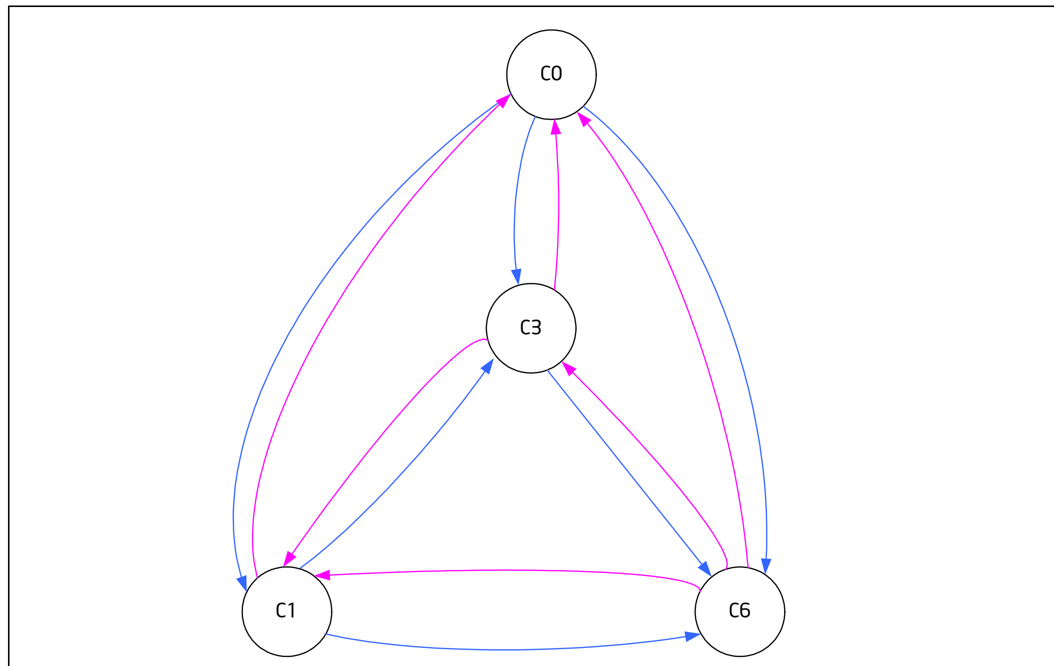
Table 12 shows package C-state resolution for a dual-core processor. Figure 9 summarizes package C-state transitions.

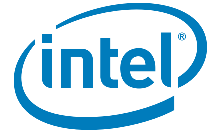
Table 12. Coordination of Core Power States at the Package Level

Package C-State		Core 1			
		C0	C1	C3	C6
Core 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

NOTE:
1. If enabled, the package C-state will be C1E if all actives cores have resolved a core C1 state or higher.

Figure 9. Package C-State Entry and Exit





4.2.5.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

4.2.5.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E via MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E via the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E.

4.2.5.3 Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6 state but has allowed a package C6 state.

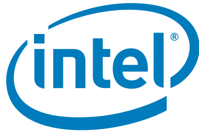
In package C3-state, the L3 shared cache is snoopable.

4.2.5.4 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The L3 shared cache is still powered and snoopable in this state. The processor remains in package C6 state as long as any part of the L3 cache is active.



4.2.5.5 Power Status Indicator (PSI#) and DPRSLPVR#

PSI# and DPRSLPVR# are signals used to optimize VR efficiency over a wide power range depending on amount of activity within the processor core. The PSI# signal is utilized by the processor core to:

- Improve intermediate and light load efficiency of the voltage regulator when the processor is active (P-states).
- Optimize voltage regulator efficiency in very low power states. Assertion of DPRSLPVR# indicates that the processor core is in a C6 low power state.

The VR efficiency gains result in overall platform power savings and extended battery life.

4.3 IMC Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

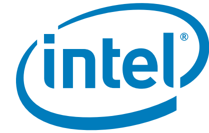
At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tristated with an SO-DIMM present, the SO-DIMM is not guaranteed to maintain data integrity.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.



4.3.2.2 Conditional Self-Refresh

The processor conditionally places memory into self-refresh in the package C3 and C6 low-power states.

When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then enters all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package C3 and C6 states as long as there are no memory requests to service. The target usage is shown in Table 13.

Table 13. Targeted Memory State Conditions

Mode	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power down based on idle conditions.
C3, C6	Dynamic memory rank power down based on idle conditions. If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power down based on idle conditions.
S3	Self Refresh Mode
S4	Memory power down (contents lost)

4.3.2.3 Dynamic Power Down Operation

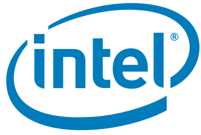
Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power down state. The processor core controller can be configured to put the devices in *active power down* (CKE deassertion with open pages) or *precharge power down* (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).



4.4 PCIe Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

4.5 DMI Power Management

- Active power management support using L0s/L1 state.

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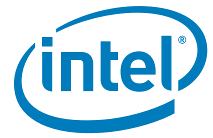


5 Thermal Management

A monolithic processor requires a thermal solution to maintain temperature of the processor die within operating limits. A complete thermal solution provides both the component-level and the system-level thermal management. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature ($T_{j,Max}$) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Thermal specifications given in this chapter are on the processor level and apply specifically to the Intel Core i7-900 mobile processor extreme edition series, Intel Core i7-800 and i7-700 mobile processor series.

Caution: Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1 Thermal Design Power and Junction Temperature

Processor TDP is the expected maximum power generated while running realistic, worst case applications (TDP applications). TDP is not the absolute worst case power of the processor. It could, for example, be exceeded under a synthetic worst case condition or under short power spikes. In production, a range of power is to be expected from the components due to the natural variation in the manufacturing process. The thermal solution, at a minimum, needs to ensure that the junction temperature of the processor does not exceed the maximum junction temperature ($T_{j,max}$) limit while running TDP applications.

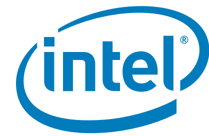
5.1.1 Intel Turbo Boost Technology

Intel Turbo Boost Technology allows the processor to have increased performance while running applications on a single core or multiple processor cores. Typical workloads are not intensive enough to push the processor to its TDP limit. Intel Turbo Boost Technology converts the available thermal power headroom into performance by increasing the frequency of all active cores above their rated TDP frequency provided that the processor is operating within its TDP, temperature, and electrical current limits. This is applicable to single-threaded and multi-threaded workloads. The performance increase (frequency) is dependent on upon the application and the number of active cores. The amount of time that Intel Turbo Boost Technology is active depends on the workload, operating environment, and system design.

5.1.2 Intel Turbo Boost Technology Thermal Design Considerations and Specifications

When designing a thermal solution for an Intel Turbo Boost-enabled processor:

- it must ensure that the $T_{j,max}$ limit is not exceeded in single-core and multi-core operation at the processor's TDP
- note that the processor can consume close to its maximum thermal power limit more frequently, and for prolonged periods of time.



The following notes apply to Table 14 and Table 15.

Note	Definition
1	The TDPs given are not the maximum power the processor can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time
2	Processor TDP is defined as the actual power consumed while running realistic applications concurrently in the systems.
3	The thermal solution needs to ensure that the temperature of the processor does not exceed the junction temperature ($T_{j,max}$) limit.
4	The processor junction temperature is monitored by DTS. A DTS outputs a temperature relative to the maximum supported junction temperature. The error associated with DTS measurements will not exceed ±5°C at $T_{j,max}$
5	The power supply to the processor should be designed as per Intel's guidelines
6	Processor current is to be monitored by IMON VR feedback (ISENSE). Error associated with power monitoring will depend upon individual VR design.
7	For efficient Intel Turbo Boost Technology operation, it is recommended to establish the full cooling capability within 10°C of the $T_{j,max}$ specification.
8	$T_{j,min}$ = 0ºC

Table 14. Intel Core i7-900 Mobile Processor Extreme Edition Series Thermal Power Specification

Processor Number	State	TDP[1,2,5,6,]	Frequency	$T_{j,max}$[3,4,7,8]
i7-920XM	HFM	55 W	2.0 GHz up to 3.20 GHz	100ºC
	LFM	37 W	1.2 GHz	100ºC

Table 15. Intel Core i7-800 Mobile Processor Series Thermal Power Specification

Processor Number	State	TDP[1,2,5,6,]	Frequency	$T_{j,max}$[3,4,7,8]
i7-820QM	HFM	45 W	1.73 GHz up to 3.06 GHz	100ºC
	LFM	35 W	1.2 GHz	100ºC

Table 16. Intel Core i7-700 Mobile Processor Series Thermal Power Specification

Processor Number	State	TDP[1,2,5,6,]	Frequency	$T_{j,max}$[3,4,7,8]
i7-720QM	HFM	45 W	1.60 GHz up to 2.80 GHz	100ºC
	LFM	35 W	933 MHz	100ºC

5.1.3 Idle Power Specifications

The idle power specifications in Table 17 and Table 18 are not 100% tested. These power specifications are determined by the characterization of the processor currents at higher temperatures and extrapolating the values for the junction temperature indicated.

Table 17. Intel Core i7-900 Mobile Processor Extreme Edition Series Idle Power

Symbol	Parameter	Min	Typ	Max	T_j
P_{C1E}	Idle power in the Package C1e state	-	-	20 W	50ºC
P_{C3}	Idle power in the Package C3 state	-	-	14.5 W	35ºC
P_{C6}	Idle power in the Package C6 state	-	-	2.6 W	35ºC

Table 18. Intel Core i7-800 and i7-700 Mobile Processor Series Idle Power

Symbol	Parameter	Min	Typ	Max	T_j
P_{C1E}	Idle power in the Package C1e state	-	-	18 W	50ºC
P_{C3}	Idle power in the Package C3 state	-	-	13 W	35ºC
P_{C6}	Idle power in the Package C6 state	-	-	2.6 W	35ºC

5.2 Thermal Management Features

This section will cover thermal management features for the processor.

5.2.1 Processor Core Thermal Features

Occasionally the processor core will operate in conditions that exceed its maximum allowable operating temperature. This can be due to internal overheating or due to overheating in the entire system. In order to protect itself and the system from thermal failure, the processor core is capable of reducing its power consumption and thereby its temperature until it is back within normal operating limits via the Adaptive Thermal Monitor.

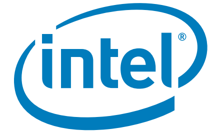
The Adaptive Thermal Monitor can be activated when any core temperature, monitored by a digital thermal sensor (DTS), exceeds its maximum junction temperature ($T_{j,Max}$) and asserts PROCHOT#. The assertion of PROCHOT# activates the thermal control circuit (TCC). The TCC will remain active as long as any core exceeds its temperature limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the processor core power consumption until the TCC is de-activated.

Caution: The Adaptive Thermal Monitor must be enabled for the processor to remain within specification.

5.2.1.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor core power consumption and temperature until it operates at or below its maximum operating temperature. Processor core power reduction is achieved by:

- Adjusting the operating frequency (via the core ratio multiplier) and input voltage (via the VID signals).



- Modulating (starting and stopping) the internal processor core clocks (duty cycle).

The Adaptive Thermal Monitor dynamically selects the appropriate method. BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) or Intel® Thermal Monitor 2 (TM2). The temperature at which the Adaptive Thermal Monitor activates the Thermal Control Circuit is not user configurable but is software visible in the IA32_TEMPERATURE_TARGET (0x1A2) MSR, Bits 23:16. The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. Note that the Adaptive Thermal Monitor is not intended as a mechanism to maintain processor TDP. The system design should provide a thermal solution that can maintain TDP within its intended usage range.

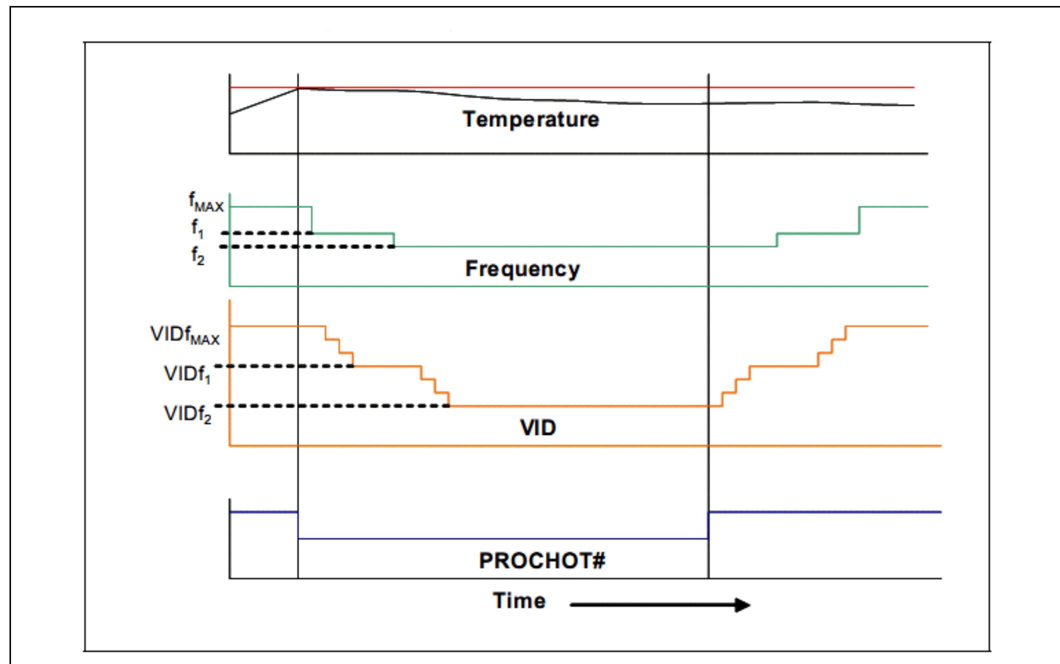
5.2.1.1.1 Frequency/VID Control

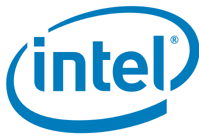
Upon TCC activation, the processor core attempts to dynamically reduce processor core power by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the core bus ratio, and number of cores in deep C-states.
- The core power and temperature are reduced while minimizing performance degradation.

A small amount of hysteresis has been included to prevent an excessive amount of operating point transitions when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. This is illustrated in Figure 10.

Figure 10. Frequency and Voltage Ordering





Once a target frequency/bus ratio is resolved, the processor core will transition to the new target automatically.

- On an upward operating point transition, the voltage transition precedes the frequency transition.
- On a downward transition, the frequency transition precedes the voltage transition.

When transitioning to a target core operating voltage, a new VID code to the voltage regulator is issued. The voltage regulator must support dynamic VID steps to support this method.

During the voltage change:

- It will be necessary to transition through multiple VID steps to reach the target operating voltage.
- Each step is 12.5 mV for Intel MVP-6.5 compliant VRs.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor core optimized target frequency, the p-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor core optimized target frequency, the processor will transition to the P-state operating point.

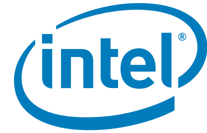
5.2.1.1.2 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 37.5% on and 62.5% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the TCC activation when the frequency/VID targets are at their minimum settings. Processor performance will be decreased by the same amount as the duty cycle when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

5.2.1.2 Digital Thermal Sensor

Each processor execution core has an on-die Digital Thermal Sensor (DTS) which detects the core's instantaneous temperature. The DTS is the preferred method of monitoring processor die temperature because

- It is located near the hottest portions of the die.
- It can accurately track the die temperature and ensure that the Adaptive Thermal Monitor is not excessively activated.



Temperature values from the DTS can be retrieved through

- A software interface via processor Model Specific Register (MSR).
- A processor hardware interface as described in "Platform Environment Control Interface (PECI)" on page 58.

Note: When temperature is retrieved by processor MSR, it is the instantaneous temperature of the given core. When temperature is retrieved via PECI, it is the average temperature of each execution core's DTS over a programmable window (default window of 256 ms.) Intel recommends using the PECI output reading for fan speed or other platform thermal control.

Code execution is halted in C1-C6. Therefore temperature cannot be read via the processor MSR without bringing a core back into C0. However, temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{j,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in an MSR. The temperature returned by the DTS is an implied negative integer indicating the relative offset from $T_{j,max}$. The DTS does not report temperatures greater than $T_{j,max}$.

The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a DTS indicates that the maximum processor core temperature has been reached (a reading of 0x0 on any core), the TCC will activate and indicate a Adaptive Thermal Monitor event.

Changes to the temperature can be detected via two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.2.1.3 PROCHOT# Signal

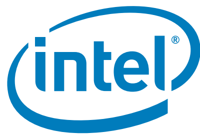
PROCHOT# (processor hot) is asserted when the processor core temperature has reached its maximum operating temperature ($T_{j,max}$). This will activate the TCC and signal a thermal event which is then resolved by the Adaptive Thermal Monitor. See Figure 10 (above) for a timing diagram of the PROCHOT# signal assertion relative to the Adaptive Thermal Response. Only a single PROCHOT# pin exists at a package level of the processor. When any core arrives at the TCC activation point, the PROCHOT# signal will be driven by the processor core. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

Note: Bus snooping and interrupt latching are active while the TCC is active.

5.2.1.3.1 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is defined as an output only. However, the signal may be configured as bi-directional. When configured as a bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is signaled externally:

- the processor core will immediately reduce processor power to the minimum voltage and frequency supported. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.



The TCC will remain active until the system deasserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and deassertion of the PROCHOT# signal.

5.2.1.3.2 Voltage Regulator Protection

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target thermal design current (I_{TDC}) instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.2.1.3.3 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable.

However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

5.2.1.3.4 Low-Power States and PROCHOT# Behavior

If the processor enters a low-power package idle state such as C3 or C6 with PROCHOT# asserted, PROCHOT# will remain asserted until:

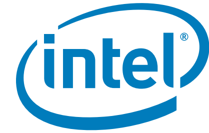
- The processor exits the low-power state
- The processor junction temperature drops below the thermal trip point.

Note that the PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor core thermals even during idle states by regularly polling for thermal data over PECI.

5.2.1.4 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption via clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. Platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be done via processor MSR or chipset I/O emulation.

On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.



5.2.1.4.1 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to a 1, the processor will immediately reduce its power consumption via modulation of the internal core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable via Bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed from 12.5% on/87.5% off to 87.5% on/12.5% off in 12.5% increments. Thermal throttling using this method will modulate each processor core’s clock independently.

5.2.1.4.2 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor cores simultaneously.

5.2.1.5 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the processor. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

5.2.1.6 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shutdown before the THERMTRIP# is activated. If the processor's Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the thermal status MSR register and also generates a thermal interrupt if enabled. For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*

5.2.2 Integrated Memory Controller Thermal Features

5.2.2.1 DRAM Throttling Options

The Integrated Memory Controller (IMC) has two, independent mechanisms that cause system memory throttling:

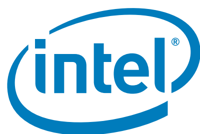
- Open Loop Throttling
- Closed Loop Throttling

5.2.2.1.1 Open Loop Throttling

Basic open loop thermal throttling can be achieved by using a virtual temperature sensor assuming current airspeeds and ambient temperature. No direct feedback is reported back from a physical thermal sensor, but the virtual temperature sensor models the DRAM die temp. The mechanism can be initiated by the virtual thermal sensor bandwidth measurement exceeding a programmed threshold via a weighted input averaging filter.

5.2.2.1.2 Closed Loop Throttling

Basic closed loop thermal throttling can be achieved using the PM_EXT_TS# signals. Temperature sensors placed on the motherboard near the DIMMs (TS-on-Board) or thermal sensors on the physical DIMMs (TS-on-DIMM) can be wire OR’d to produce an



PM_EXT_TS# signal to the memory controller. The temperature sensors will be configured to trip at the lowest temperature at which the associated DRAMs might exceed the thermal specification. If this situation occurs, the memory controller will throttle all ranks according to the duty cycle configured, trigger an SMI or SCI interrupt for software based thermal management.

5.2.2.2 External Thermal Sensor Interface Overview

The processor supports two inputs for external thermal sensor notifications, based on which it can regulate memory accesses.

Note: The thermal sensors should be capable of measuring the ambient temperature only and should be able to assert PM_EXT_TS#[0] and/or PM_EXT_TS#[1] if the pre-programmed thermal limits/conditions are met or exceeded.

An external thermal sensor with a serial interface may be placed next to a SO-DIMM (or any other appropriate platform location), or a remote Thermal Diode may be placed next to the SO-DIMM (or any other appropriate platform location) and connected to the external Thermal Sensor.

Additional external thermal sensor's outputs, for multiple sensors, can be wire-OR'd together allow signaling from multiple sensors that are physically located separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the overtemp through the serial interface. However, since the SO-DIMM's is located on the same Memory Bus Data lines, any IMC-based read throttle will apply equally.

Thermal sensors can either be directly routed to the PM_EXT_TS#[0] and PM_EXT_TS#[1] pins or indirectly routed to the processor by invoking an Embedded Controller (EC) connected in between the thermal sensor and processor core pins. Both routing methods are applicable for both thermal sensors placed on the motherboard (TS-on-Board) and/or thermal sensors located on the memory modules (TS-on-DIMM).

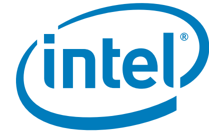
5.2.3 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices. The processor implements a PECI interface to allow communication of processor thermal information to other devices on the platform. The processor provides a digital thermal sensor (DTS) for fan speed control. The DTS is calibrated at the factory to provide a digital representation of relative processor temperature. Averaged DTS values are read via the PECI interface.

The PECI physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a Logic 0 or Logic 1. PECI also includes variable data transfer rate established with every message. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

5.2.3.1 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability well before the DTS reading reaches $T_{j,max}$. An example of this would be $T_{FAN} = T_{j,max}$ - 10ºC.



5.2.3.2 Processor Thermal Data Sample Rate and Filtering

The processor digital thermal sensor (DTS) provides an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. To reduce the sample rate requirements on PECI and improve thermal data stability vs. time the processor DTS implements an averaging algorithm that filters the incoming data. This filter is expressed mathematically as:

PECI(t) = PECI(t-1)+1/(2^^X)*[Temp - PECI(t-1)]

where:

- PECI(t) is the new averaged temperature.
- PECI(t-1) is the previous averaged temperature.
- Temp is the raw temperature data from the DTS.
- X is the Thermal Averaging Constant (TAC).

The Thermal Averaging Constant is a BIOS configurable value that determines the time in milliseconds over which the DTS temperature values are averaged (the default time is 256 ms). Short averaging times will make the averaged temperature values respond more quickly to DTS changes. Long averaging times will result in better overall thermal smoothing but also incur a larger time lag between fast DTS temperature changes and the value read via PECI.

Within the processor, the DTS converts an analog signal into a digital value representing the temperature relative to PROCHOT# circuit activation. The conversions are in integers with each single number change corresponding to approximately 1°C. DTS values reported via the internal processor MSR will be in whole integers.

As a result of the PECI averaging function described above, DTS values reported over PECI will include a 6-bit fractional value. Under typical operating conditions, where the temperature is close to PROCHOT#, the fractional values may not be of interest. But when the temperature approaches zero, the fractional values can be used to detect the activation of the PROCHOT# circuit. An averaged temperature value between 0 and 1 can only occur if the PROCHOT# circuit has been activated during the averaging window. As PROCHOT# circuit activation time increases, the fractional value will approach zero. Fan control circuits can detect this situation and take appropriate action as determined by the system designers. Of course, fan control chips can also monitor the PROCHOT# pin to detect PROCHOT# circuit activation via a dedicated input pin on the package.

§

6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type:

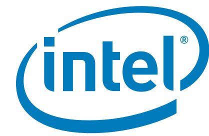
Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal:

Table 19. Signal Description Buffer Types

Signal	Description
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Asynchronous[1]	Signal has no timing relationship with any reference clock.
CMOS	CMOS buffers. 1.1-V tolerant
DDR3	DDR3 buffers: 1.5-V tolerant
DMI	Direct Media Interface signals. These signals are compatible with *PCI Express 2.0 Signaling Environment AC Specifications*, but are DC coupled. The buffers are not 3.3-V tolerant.
FDI	Intel Flexible Display interface signals. These signals are compatible with *PCI Express 2.0 Signaling Environment AC Specifications*, but are DC coupled. The buffers are not 3.3-V tolerant.
GTL	Gunning Transceiver Logic signaling technology
PCI Express*	PCI Express interface signals. These signals are compatible with *PCI Express 2.0 Signalling Environment AC Specifications* and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
Ref	Voltage reference signal

NOTES:
1. Qualifier for a buffer type.



6.1 System Memory Interface

Table 20. Memory Channel A

Signal Name	Description	Direction/Buffer Type
SA_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SA_CAS#	**CAS Control Signal:** Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_CK[1:0]	**SDRAM Differential Clock:** Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CK and the negative edge of its complement SA_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SA_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel A SDRAM Differential clock signal-pair complement.	O DDR3
SA_CKE[1:0]	**Clock Enable:** (1 per rank) Used to: - Initialize the SDRAMs during power-up - Power-down SDRAM ranks - Place all SDRAM ranks into and out of self-refresh during STR	O DDR3
SA_CS#[1:0]	**Chip Select:** (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SA_DQ[63:0]	**Data Bus:** Channel A data signal interface to the SDRAM data bus.	I/O DDR3
SA_DQS[7:0]	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS#[7:0] during read and write transactions	I/O DDR3
SA_DQS#[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O DDR3
SA_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SA_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3
SA_RAS#	**RAS Control Signal:** Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_WE#	**Write Enable Control Signal:** Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O DDR3

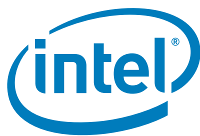
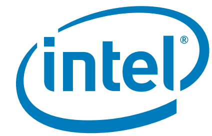


Table 21. Memory Channel B

Signal Name	Description	Direction/Buffer Type
SB_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SB_CAS#	**CAS Control Signal:** Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_CK[1:0]	**SDRAM Differential Clock:** Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CK and the negative edge of its complement SB_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SB_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel B SDRAM Differential clock signal-pair complement.	O DDR3
SB_CKE[1:0]	**Clock Enable:** (1 per rank) Used to: - Initialize the SDRAMs during power-up. - Power-down SDRAM ranks. - Place all SDRAM ranks into and out of self-refresh during STR.	O DDR3
SB_CS#[1:0]	**Chip Select:** (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SB_DQ[63:0]	**Data Bus:** Channel B data signal interface to the SDRAM data bus.	I/O DDR3
SB_DQS[7:0]	**Data Strobes:** SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS#[7:0] during read and write transactions.	I/O DDR3
SB_DQS#[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O DDR3
SB_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SB_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3
SB_RAS#	**RAS Control Signal:** Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_WE#	**Write Enable Control Signal:** Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O DDR3



6.2 Memory Reference and Compensation

Table 22. Memory Reference and Compensation

Signal Name	Description	Direction/Buffer Type
SA_DIMM_VREFDQ SB_DIMM_VREFDQ	Memory Channel A/B DIMM DQ Reference Voltage	O A
SM_RCOMP[2:0]	System Memory Impedance Compensation	I A

6.3 Reset and Miscellaneous Signals

Table 23. Reset and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description	Direction/Buffer Type
BPM#[7:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O GTL
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. **CFG[1:0]** - PCI Express* Port Bifucation: • 11 = 1 x16 PEG • 10 = 2 x8 PEG **CFG[2] -** Reserved Configuration pin. **CFG[3]** – Reserved **CFG[11:4] -** Reserved configuration pins. **CFG[12]** - N/A **CFG[17:13] -** Reserved configuration pins. **Note:** Hardware straps are sampled after RSTIN# de-assertion.	I CMOS
COMP0	Impedance compensation must be terminated on the system board using a precision resistor.	I A
DBR#	**Debug Reset:** Used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. This signal only routes through the package and does not connect to the the processor silicon itself.	O
PM_EXT_TS#[0] PM_EXT_TS#[1]	**External Thermal Sensor Input:** If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling.	I CMOS

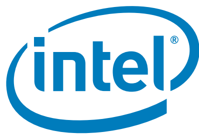
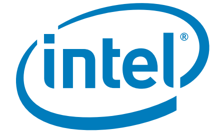


Table 23. Reset and Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Description	Direction/Buffer Type
PM_SYNC	**Power Management Sync:** A sideband signal to communicate power management status from the platform to the processor.	I CMOS
PRDY#	**PRDY#**: A processor output used by debug tools to determine processor debug readiness.	O Asynchronous GTL
PREQ#	**PREQ#:** Used by debug tools to request debug operation of the processor.	I Asynchronous GTL
RESET_OBS#	This signal is an indication of the processor being reset.	O Asynchronous CMOS
RSTIN#	**Reset In:** When asserted this signal will asynchronously reset the processor logic. This signal is connected to the PLTRST# output of the PCH.	I CMOS
RSVD RSVD_TP RSVD_NCTF	**RESERVED.** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. However, Intel recommends that all RSVD_TP signals have via test points.	No Connect Test Point Non-Critical to Function
SM_DRAMRST#	**DDR3 DRAM Reset:** Reset signal from processor to DRAM devices. One for all channels or SO-DIMMs.	O DDR3



6.4 PCI Express Graphics Interface Signals

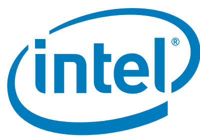
Table 24. PCI Express Graphics Interface Signals

Signal Name	Description	Direction/Buffer Type
PEG_ICOMPI	PCI Express Graphics Input Current Compensation	I A
PEG_ICOMPO	PCI Express Graphics Output Current Compensation	I A
PEG_RBIAS	PCI Express Resistor Bias Control	I A
PEG_RCOMPO	PCI Express Graphics Resistance Compensation	I A
PEG_RX[15:0] PEG_RX#[15:0]	PCI Express Graphics Receive Differential Pair	I PCI Express
PEG_TX[15:0] PEG_TX#[15:0]	PCI Express Graphics Transmit Differential Pair	O PCI Express

6.5 DMI

Table 25. DMI - Processor to PCH Serial Interface

Signal Name	Description	Direction/Buffer Type
DMI_RX[3:0] DMI_RX#[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pair.	I DMI
DMI_TX[3:0] DMI_TX#[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pair.	O DMI



6.6 PLL Signals

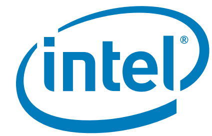
Table 26. PLL Signals

Signal Name	Description	Direction/Buffer Type
BCLK BCLK#	Differential bus clock input to the processor	I Diff Clk
BCLK_ITP BCLK_ITP#	Buffered differential bus clock pair to ITP	O Diff Clk
PEG_CLK PEG_CLK#	**Differential PCI Express Based Graphics/DMI Clock In:** These pins receive a 100-MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.	I Diff Clk

6.7 TAP Signals

Table 27. TAP Signals

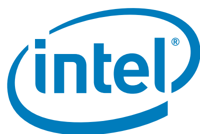
Signal Name	Description	Direction/Buffer Type
TAPPWRGOOD	Power good for ITP	O Asynchronous CMOS
TCK	**TCK (Test Clock):** Provides the clock input for the processor Test Bus (also known as the Test Access Port).	I CMOS
TDI	**TDI (Test Data In):** Transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I CMOS
TDI_M	**Test Data In for the GPU/Memory core:** Tie TDI_M and TDO_M together on the motherboard	I CMOS
TDO	Test Data Output	O CMOS
TDO_M	**Test Data Output from the processor core:** Tie TDO_M and TDI_M together on the motherboard.	O CMOS
TMS	**TMS (Test Mode Select):** A JTAG specification support signal used by debug tools.	I CMOS
TRST#	TRST# (Test Reset) Boundary-Scan test reset pin	I CMOS



6.8 Error and Thermal Protection

Table 28. Error and Thermal Protection

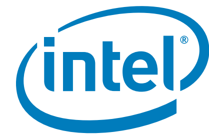
Signal Name	Description	Direction/Buffer Type
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. External agents are allowed to assert this pin which will cause the processor to take a machine check exception.	I/O GTL
PECI	**PECI (Platform Environment Control Interface):** A serial sideband interface to the processor, it is used primarily for thermal, power, and error management.	I/O Asynchronous
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O Asynchronous GTL
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130°C. This is signaled to the system by the THERMTRIP# pin.	O Asynchronous GTL



6.9 Power Sequencing

Table 29. Power Sequencing

Signal Name	Description	Direction/Buffer Type
SKTOCC#	**SKTOCC# (Socket Occupied):** pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	
SM_DRAMPWROK	**SM_DRAMPWROK Processor Input**: Connects to PCH DRAMPWROK.	I Asynchronous CMOS
VCCPWRGOOD_0	**VCCPWRGOOD_0 (Power Good) Processor Input:** The processor requires this signal to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. This signal must transition monotonically to a high state. VCCPWRGOOD_0 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of this signal. VCCPWRGOOD_0 should be connected to the PROCPWRGD output signal of the PCH.	I Asynchronous CMOS
VTTPWRGOOD	**VTTPWRGOOD Processor Input:** The processor requires this input signal to be a clean indication that the VTT power supply is stable and within specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Note it is not valid for VTTPWRGOOD to be deasserted while VCCPWRGOOD_0is asserted.	I Asynchronous CMOS



6.10 Processor Power Signals

Table 30. Processor Power Signals (Sheet 1 of 2)

Signal Name	Description	Direction/Buffer Type
VCC	Processor core power rail.	Ref
VTT (VTT0 and VTT1)	**Processor I/O power rail (1.1V).** VTT0 and VTT1 should be tied together	Ref
VDDQ	DDR3 power rail (1.5 V)	Ref
VCCPLL	Power rail for filters and PLLs (1.8 V)	Ref
ISENSE	Current Sense from an Intel MVP6.5 Compliant Regulator to the processor core.	I A
PROC_DPRSLPVR	Processor output signal to indicate that the processor is in the package C6state.	O CMOS
PSI#	**Processor Power Status Indicator:** This signal is asserted when the processor core current consumption is less than 15A. Assertion of this signal is an indication that the VR controller does not currently need to provide ICC above 15 A. The VR controller can use this information to move to a more efficient operating point. This signal will de-assert at least 3.3us before the current consumption will exceed 15 A. The minimum PSI# assertion and de-assertion time is 1 BCLK.	O Asynchronous CMOS
VID[6] VID[5:3]/CSC[2:0] VID[2:0]/MSID[2:0]	**VID[6:0] (Voltage ID) Pins:** Used to support automatic selection of power supply voltages (VCC). These are CMOS signals that are driven by the processor. **CSC[2:0]/VID[5:3]** - Current Sense Configuration bits, for ISENSE gain setting. . **MSID[2:0]/VID[2:0]-** Market Segment Identification is used to indicate the maximum platform capability to the processor. A processor will only boot if the MSID[2:0] pins are strapped to the appropriate setting (or higher) on the platform (see "Market Segment Selection Truth Table for MSID[2:0]" on page 77 for MSID encodings). MSID is used to help protect the platform by preventing a higher power processor from booting in a platform designed for lower power processors. Refer to the appropriate platform design guide for implementation details. MSID[2:0] are latched on the rising edge of VTTPWRGOOD. **NOTE:** VID[5:3] and VID[2:0] are bi-directional. As an input, they are CSC[2:0] and MSID[2:0] respectively.	O CMOS

Table 30. Processor Power Signals (Sheet 2 of 2)

Signal Name	Description	Direction/Buffer Type
VTT_SELECT	The VTT_SELECT signal is used to select the correct VTT voltage level for the processor.	O CMOS
VCC_SENSE VSS_SENSE	Voltage Feedback Signals. Use VCC_SENSE to sense voltage and VSS_SENSE to sense ground near the silicon with little noise.	O A
VTT_SENSE VSS_SENSE_VTT	Isolated low impedance connection to the processor VTT voltage and ground. They can be used to sense or measure voltage near the silicon.	O A

6.11 Ground and NCTF

Table 31. Ground and NCTF

Signal Name	Description	Direction/Buffer Type
VSS	Processor ground node	GND
VSS_NCTF	**Non-Critical to Function:** The pins are for package mechanical reliability.	

6.12 Processor Internal Pull Up/Pull Down

Table 32. Processor Internal Pull Up/Pull Down

Signal Name	Pull Up/Pull Down	Rail	Value
SM_DRAMPWROK	Pull Down	VSS	10-20 kΩ
VCCPWRGOOD_0 VCCPWRGOOD_1	Pull Down	VSS	10-20 kΩ
VTTPWRGOOD	Pull Down	VSS	10-20 kΩ
BPM#[7:0]	Pull Up	VSS	44-55 Ω
TCK	Pull Up	VTT	44-55 Ω
TDI	Pull Up	VTT	44-55 Ω
TMS	Pull Up	VTT	44-55 Ω
TRST#	Pull Up	VTT	1-5 kΩ
TDI_M	Pull Up	VTT	44-55 Ω
PREQ#	Pull Up	VTT	44-55 Ω
CFG[17:0]	Pull Up	VTT	5-14 kΩ

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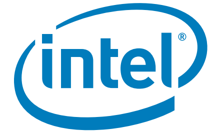


7 Electrical Specifications

7.1 Power and Ground Pins

The processor has V_{CC}, V_{TT}, V_{DDQ}, V_{CCPLL}, and V_{SS} (ground) inputs for on-chip power distribution. All power pins must be connected to their respective processor power planes, while all V_{SS} pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The V_{CC} pins must be supplied with the voltage determined by the processor **V**oltage **ID**entification (VID) signals. Table 33 specifies the voltage level for the various VIDs.

7.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low- and full-power states. To keep voltages within specification, output decoupling must be properly designed.

Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications listed in Table 33. Failure to do so can result in timing violations or reduced lifetime of the processor.

7.2.1 Voltage Rail Decoupling

The voltage regulator solution must:

- provide sufficient decoupling to compensate for large current swings generated during different power mode transitions.
- provide low parasitic resistance from the regulator to the socket.
- meet voltage and current specifications as defined in Table 33.

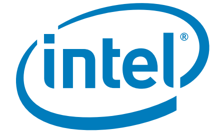
7.3 Processor Clocking (BCLK, BCLK#)

The processor utilizes a differential clock to generate the processor core(s) operating frequency, memory controller frequency, and other internal clocks. The processor core frequency is determined by multiplying the processor core ratio by 133 MHz. Clock multiplying within the processor is provided by an internal phase locked loop (PLL), which requires a constant frequency input, with exceptions for Spread Spectrum Clocking (SSC).

The processor’s maximum core frequency is configured during power-on reset by using its manufacturing default value. This value is the highest core multiplier at which the processor can operate.

7.3.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 33 for DC specifications.



7.4 Voltage Identification (VID)

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of the processor power supply voltages. VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 33 specifies the voltage level for VID[6:0]; 0 refers to a low-voltage level.

VID signals are CMOS push/pull drivers. Refer to Table 41 for the DC specifications for these signals. The VID codes will change due to temperature, frequency, and/or power mode load changes in order to minimize the power of the part. A voltage range is provided in Table 33. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 33. The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the loadline.

Note: A low-to-high or high-to-low voltage state change will result in as many VID transitions as necessary to reach the target core voltage. Transitions above the maximum or below the minimum specified VID are not permitted. One VID transition occurs in 2.5 µs.

The VR utilized must be capable of regulating its output to the value defined by the new VID values issued. DC specifications for dynamic VID transitions are included in Table 33.

Several of the VID signals (VID[5:3]/CSC[2:0] and VID[2:0]/MSID[2:0]) serve a dual purpose and are sampled during reset. Refer to the signal description table in Chapter 6 for more information.

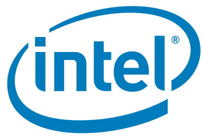


Table 33. Voltage Identification Definition (Sheet 1 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375

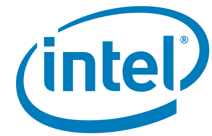


Table 33. Voltage Identification Definition (Sheet 2 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500

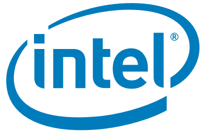


Table 33. Voltage Identification Definition (Sheet 3 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

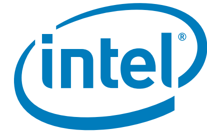


Table 34. Market Segment Selection Truth Table for MSID[2:0]

MSID[2]	MSID[1]	MSID[0]	Description[1,2]	Notes
0	0	0	Reserved	
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	Reserved	
1	0	0	Intel® Core™ i7-800 and i7-700 mobile processor series supported	3
1	0	1	Reserved	
1	1	0	Intel Core i7-900 mobile processor extreme edition series supported	4
1	1	1	Reserved	

NOTES:
1. MSID[2:0] signals are provided to indicate the maximum platform capability to the processor.
2. MSID is used on rPGA988A platforms only.
3. Processors specified for use with a -1.9 mΩ loadline
4. Processors specified for use with a -1.6 mΩ loadline

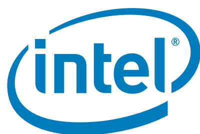
7.5 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

Arbitrary connection of these signals to V_{CC}, V_{TT}, V_{DDQ}, V_{CCPLL}, V_{SS}, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Chapter 8 for a pin listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines. For details see Table 41.



7.6 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Table 35. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR3 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

Table 35. Signal Groups[1] (Sheet 1 of 3)

Signal Group	Alpha Group	Type	Signals
System Reference Clock			
Differential	(a)	CMOS Input	BCLK, BCLK# PEG_CLK, PEG_CLK# DPLL_REF_SSCLK[3], DPLL_REF_SSCLK#[3]
Differential	(b)	CMOS Output	BCLK_ITP, BCLK_ITP#
DDR3 Reference Clocks[2]			
Differential	(c)	DDR3 Output	SA_CK[1:0], SA_CK#[1:0] SB_CK[1:0], SB_CK#[1:0]
DDR3 Command Signals[2]			
Single Ended	(d)	DDR3 Output	SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS# SA_WE#, SB_WE# SA_MA[15:0], SB_MA[15:0] SA_BS[2:0], SB_BS[2:0] SA_DM[7:0][3], SB_DM[7:0][3] SM_DRAMRST# SA_CS#[1:0], SB_CS#[1:0] SA_ODT[1:0], SB_ODT[1:0] SA_CKE[1:0], SB_CKE[1:0]
DDR3 Data Signals[2]			
Single ended	(e)	DDR3 Bi-directional	SA_DQ[63:0], SB_DQ[63:0]
Differential	(f)	DDR3 Bi-directional	SA_DQS[7:0], SA_DQS#[7:0] SB_DQS[7:0], SB_DQS#[7:0]
TAP (ITP/XDP)			
Single Ended	(g)	CMOS Input	TCK, TDI, TMS, TRST#, TDI_M
Single Ended	(h)	CMOS Open-Drain Output	TDO, TDO_M
Single Ended	(i)	Asynchronous CMOS Output	TAPPWRGOOD

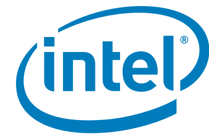


Table 35. Signal Groups[1] (Sheet 2 of 3)

Signal Group	Alpha Group	Type	Signals
Control Sideband			
Single Ended	(ja)	Asynchronous CMOS Input	$V_{CCPWRGOOD_0}$, $V_{CCPWRGOOD_1}$[3], $V_{TTPWRGOOD}$
Single Ended	(jb)	Asynchronous CMOS Input	SM_DRAMPWROK
Single Ended	(k)	Asynchronous CMOS Output	RESET_OBS#
Single Ended	(l)	Asynchronous GTL Output	PRDY#, THERMTRIP#
Single Ended	(m)	Asynchronous GTL Input	PREQ#
Single Ended	(n)	GTL Bi-directional	CATERR#, BPM#[7:0]
Single Ended	(o)	Asynchronous Bi-directional	PECI
Single Ended	(p)	Asynchronous GTL Bi-directional	PROCHOT#
Single Ended	(qa)	CMOS Input	PM_SYNC, PM_EXT_TS#[0], PM_EXT_TS#[1], CFG[17:0]
Single Ended	(qb)	CMOS Input	RSTIN#
Single Ended	(r)	CMOS Output	PROC_DPRSLPVR VID[6] V_{TT_SELECT}
Single Ended	(s)	CMOS Bi-directional	VID[5:3]/CSC[2:0] VID[2:0]/MSID[2:0]
Single Ended	(t)	Analog Input	COMP0, COMP1[3], COMP2[3], COMP3[3], SM_RCOMP[2:0], I_{SENSE}
Single Ended	(ta)	Analog Output	SA_DIMM_VREFDQ, SB_DIMM_VREFDQ
Power/Ground/Other			
Single Ended	(u)	Power	V_{CC}, V_{TT0}, V_{TT1}, V_{CCPLL}, V_{DDQ}, V_{AXG}[3]
Single Ended	(v)	Ground	V_{SS}, V_{SS_NCTF}
Single Ended	(w)	No Connect /Test Point	RSVD, RSVD_TP, RSVD_NCTF
Single Ended	(x)	Asynchronous CMOS Output	PSI#
Single Ended	(y)	Sense Points	V_{CC_SENSE}, V_{SS_SENSE}, V_{TT_SENSE}, $V_{SS_SENSE_VTT}$, V_{AXG_SENSE}[3], V_{SSAXG_SENSE}[3]
Single Ended	(z)	Other	SKTOCC#, DBR#

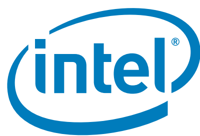


Table 35. Signal Groups[1] (Sheet 3 of 3)

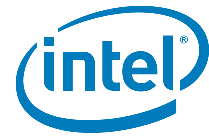
Signal Group	Alpha Group	Type	Signals
Integrated Graphics[3]			
Single Ended	(aa)	Analog Input	GFX_IMON
Single Ended	(ab)	CMOS Output	GFX_VID[6:0], GFX_VR_EN, GFX_DPRSLPVR
PCI Express* Graphics			
Differential	(ac)	PCI Express Input	PEG_RX[15:0], PEG_RX#[15:0]
Differential	(ad)	PCI Express Output	PEG_TX[15:0], PEG_TX#[15:0]
Single Ended	(ae)	Analog Input	PEG_ICOMP0, PEG_ICOMPI, PEG_RCOMP0, PEG_RBIAS
DMI			
Differential	(af)	DMI Input	DMI_RX[3:0], DMI_RX#[3:0]
Differential	(ag)	DMI Output	DMI_TX[3:0], DMI_TX#[3:0]
Intel® FDI[5]			
Single Ended	(ah)	CMOS Input	FDI_FSYNC[1:0], FDI_LSYNC[1:0], FDI_INT
Differential	(ai)	Analog Output	FDI_TX[7:0], FDI_TX#[7:0]

NOTES:
1. Refer to Chapter 6 for signal description details.
2. SA and SB refer to DDR3 Channel A and DDR3 Channel B.
3. These signals will not be actively used on Intel Core i7-900 mobile extreme edition processor series, Intel Core i7-800 and i7-700 mobile processor series.

All Control Sideband Asynchronous signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 7.10

7.7 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.



7.8 Absolute Maximum and Minimum Ratings

Table 36 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 36. Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}	Processor Core voltage with respect to V_{SS}	-0.3	1.45	V	1, 2, 3
V_{TT}	Voltage for the memory controller and Shared Cache with respect to V_{SS}	-0.3	1.155	V	1, 2
V_{DDQ}	Processor I/O supply voltage for DDR3 with respect to V_{SS}	-0.3	1.65	V	1, 2
V_{CCPLL}	Processor PLL voltage with respect to V_{SS}	-0.3	1.89	V	1, 2

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. V_{CC} is a VID based rail

7.9 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity to which the device is exposed to while being stored in a moisture barrier bag. The specified storage conditions are for component level prior to board attach.

Table 37 specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. these limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

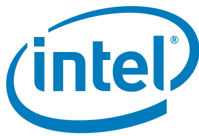


Table 37. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{absolute\ storage}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when exceeded for any length of time.	-25°C	125°C	1, 2, 3, 4
$T_{sustained\ storage}$	The ambient storage temperature (in shipping media) for a sustained period of time)	-5°C	40°C	5, 6
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24°C		6, 7
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	7

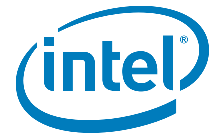
NOTES:
1. Refers to a component device that is not assembled in a board or socket and is not electrically connected to a voltage reference or I/O signal.
2. Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount reflow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
3. $T_{absolute\ storage}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags, or desiccant.
4. Component product device storage temperature qualification methods may follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards when applicable for volatile memory.
5. Intel® branded products are specified and certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40°C to 70°C and Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28°C.) Post board attach storage temperature limits are not specified for non-Intel branded boards.
6. The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
7. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{sustained\ storage}$ and customer shelf life in applicable Intel boxes and bags.

7.10 DC Specifications

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise. See Chapter 8 for the processor pin listings and Chapter 6 for signal definitions.

The DC specifications for the DDR3 signals are listed in Table 40 Control Sideband and Test Access Port (TAP) are listed in Table 41.

Table 38 lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.



7.10.1 Voltage and Current Specifications

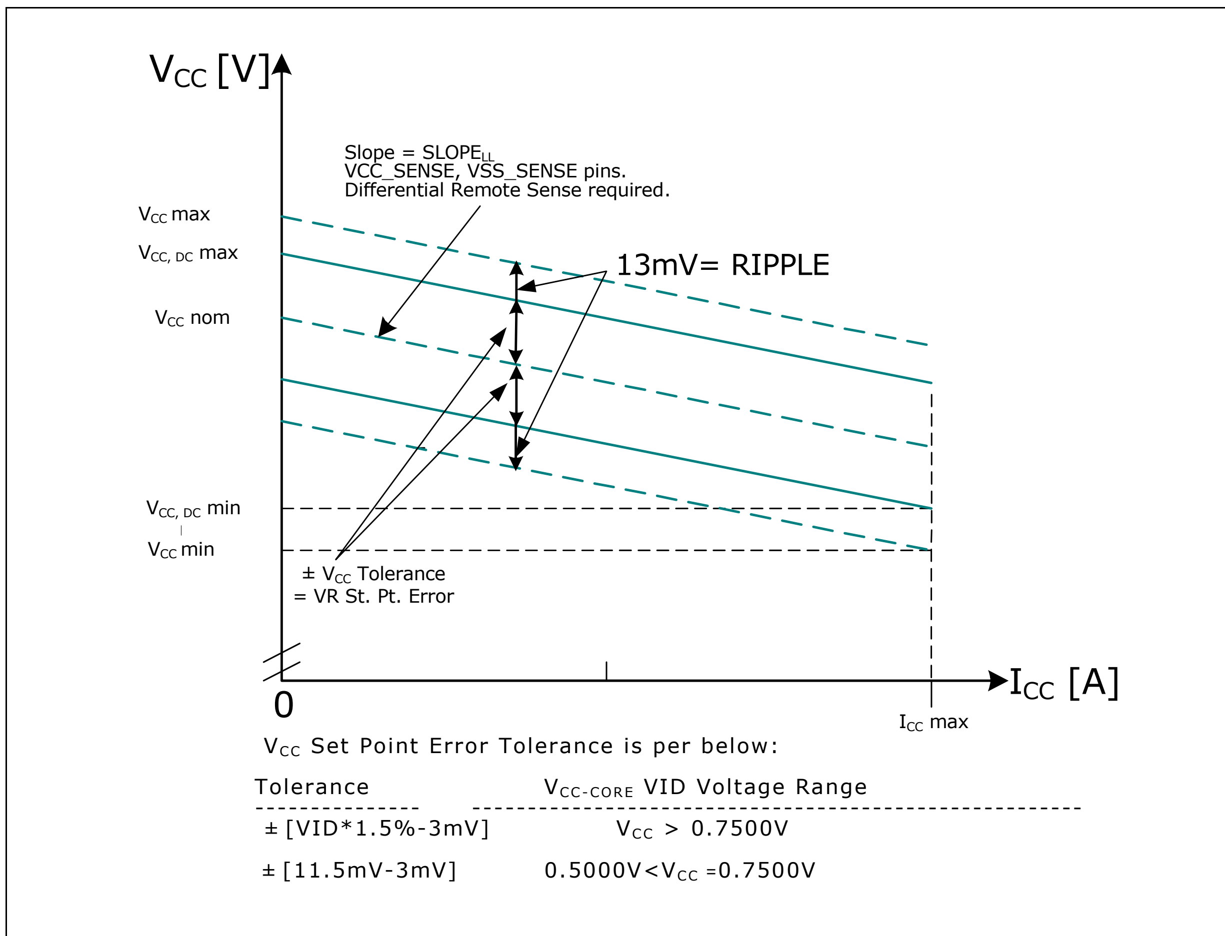
Table 38. Processor Core (VCC) Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter		Min	Typ	Max	Unit	Note
HFM_VID	Highest Frequency Mode VID Range		0.75		1.4	V	1,6
LFM_VID	Lowest Frequency Mode VID Range		0.65		1.0	V	1
V_{CC}	V_{CC} for processor core		See Figure 11 and Figure 12			V	1, 2, 3
TOL_{VID}	VID Tolerance		See Figure 11 and Figure 12				
I_{CCMAX}	Max Processor Core I_{CC}						
	Processor Number i7-720QM i7-820QM i7-920XM	Rated Frequency 1.60 GHz 1.73 GHz 2.00 GHz			52 52 65	A	4,6,7
I_{CC_TDC}	Thermal Design I_{CC}						
	Processor Number i7-720QM i7-820QM i7-920XM	Rated Frequency 1.60 GHz 1.73 GHz 2.00 GHz			38 38 48	A	5,6,7
I_{CC_LFM}	I_{CC} at LFM				30	A	7
I_{C6}	I_{CC} at C6 Idle-state				2	A	7
VR Step	VID resolution			12.5		mV	
$SLOPE_{LL}$	Processor Loadline						
	Processor Number i7-720QM i7-820QM i7-920XM	Rated Frequency 1.60 GHz 1.73 GHz 2.00 GHz		-1.9 -1.9 -1.6		mΩ	
Non-VR LL contribution	Non-VR Loadline Contribution for V_{CC}			-0.9		mΩ	

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
2. Refer to 8.10.2 for V_{CC} validation
3. Refer to Figure 11 and Figure 12for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current.
4. Processor core VR to be designed to electrically support this current.
5. Processor core VR to be designed to thermally support this current indefinitely.
6. This specification assumes that Intel Turbo Boost Technology is enabled.
7. This value is specified at nominal voltage.

Figure 11. Active V_{CC} and I_{CC} Loadline (PSI# Asserted)



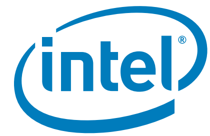
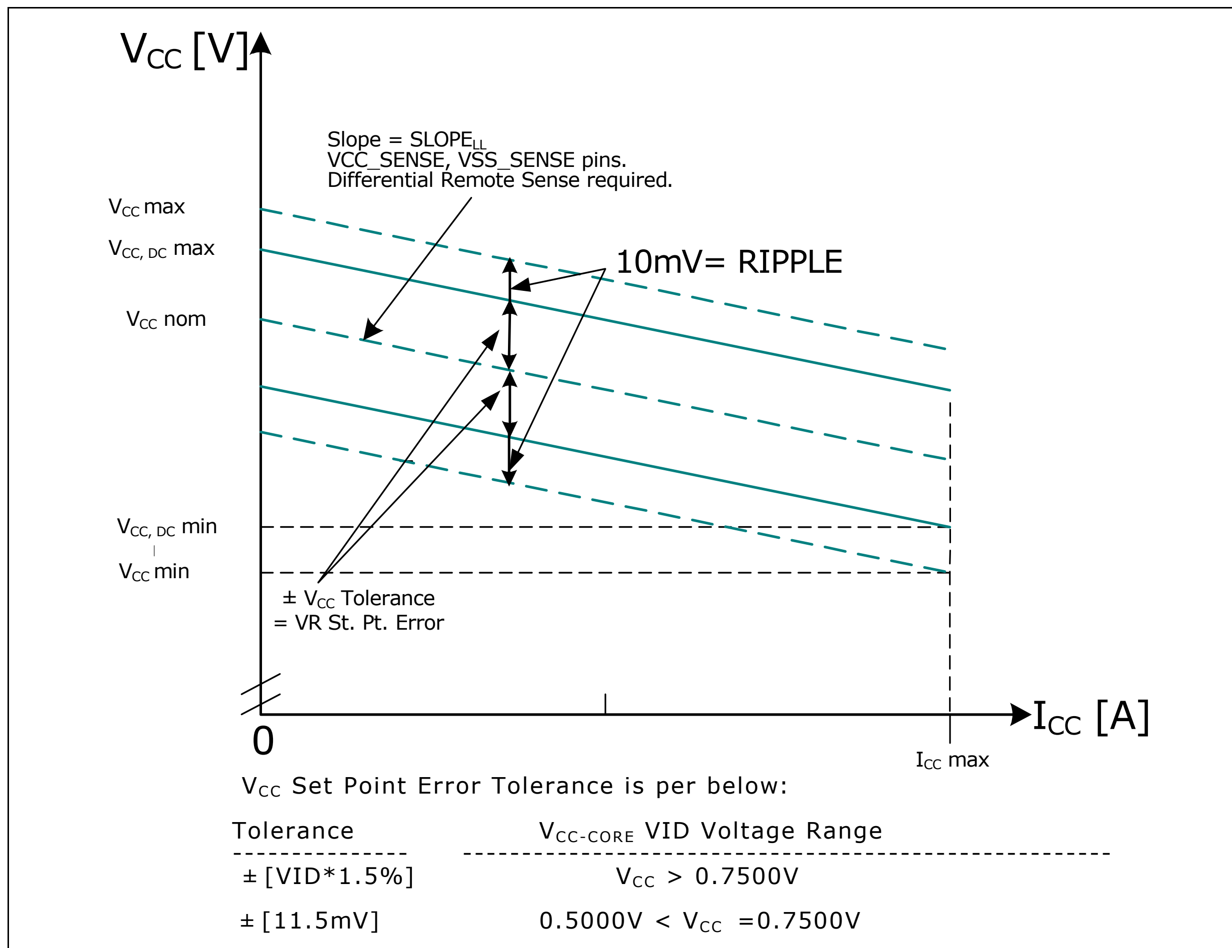


Figure 12. Active V_{CC} and I_{CC} Loadline (PSI# Not Asserted)



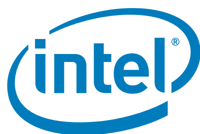


Table 39. Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{TT}	Voltage for the memory controller and shared cache at the socket motherboard V_{TT} pinfield via	1.045	1.10	1.155	V	1
	Voltage for the memory controller and shared cache defined across V_{TT_SENSE} and $V_{SS_SENSE_VTT}$	1.023	1.10	1.177	V	2
TOL_{TT}	V_{TT} Tolerance defined at the socket motherboard VTT pinfield via	DC: ±2 AC: ±3 including ripple			%	1
	V_{TT} Tolerance defined across V_{TT_SENSE} and $V_{SS_SENSE_VTT}$	DC: ±2 AC: ±5 including ripple			%	2
I_{CCMAX_VTT}	Max Current for V_{TT} Rail Intel® Core™ i7-800 and i7-700 mobile processor series Intel Core i7-900 mobile processor extreme edition series			 18 21	A	3
I_{CCTDC_VTT}	Thermal Design Current (TDC) for V_{TT} Rail Intel Core i7-800 and i7-700 mobile processor series Intel Core i7-900 mobile processor extreme edition series		-	 17 20	A	3
V_{DDQ}	Processor I/O supply voltage for DDR3 (DC + AC specification)	1.425	1.5	1.575	V	
TOL_{DDQ}	V_{DDQ} Tolerance	DC= ±3 AC= ±2			%	
I_{CCMAX_VDDQ}	Max Current for V_{DDQ} Rail		-	6	A	
I_{CCTDC_VDDQ}	Thermal Design Current (TDC) for V_{DDQ} Rail		-	5	A	
I_{CCAVG_VDDQ} (Standby)	Standby Current for V_{DDQ} Rail i		-	0.5	A	
V_{CCPLL}	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V	
TOL_{CCPLL}	V_{CCPLL} Tolerance	AC+DC= ±5%			%	
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail		-	1.1	A	
I_{CCTDC_VCCPLL}	Thermal Design Current (TDC) for V_{CCPLL} Rail		-	0.7	A	

NOTES:
1. The voltage specification requirements are defined across at the socket motherboard pinfield vias on the bottom side of the baseboard. Please refer to 8.10.3 for uncore voltage validation.
2. The voltage specification requirements are defined across V_{TT_SENSE} and $V_{SS_SENSE_VTT}$ pins on the bottom side of the baseboard. Please refer to 8.10.3 for uncore voltage validation.
3. Defined at nominal V_{TT} voltage

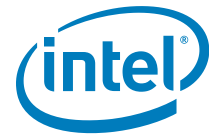


Table 40. DDR3 Signal Group DC Specifications

Symbol	Parameter	Alpha Group	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	(e,f)			$0.43*V_{DDQ}$	V	2,4
V_{IH}	Input High Voltage	(e,f)	$0.57*V_{DDQ}$			V	3
V_{OL}	Output Low Voltage	(c,d,e,f)		$(V_{DDQ} / 2)* (R_{ON} / (R_{ON}+R_{VTT_TERM}))$			6
V_{OH}	Output High Voltage	(c,d,e,f)		$V_{DDQ} - ((V_{DDQ} / 2)* (R_{ON}/ (R_{ON}+R_{VTT_TERM}))$		V	4,6
R_{ON}	DDR3 Clock Buffer On Resistance		21		36	Ω	5
R_{ON}	DDR3 Command Buffer On Resistance		20		31	Ω	5
R_{ON}	DDR3 Control Buffer On Resistance		20		31	Ω	5
R_{ON}	DDR3 Data Buffer On Resistance		21		36	Ω	5
Data ODT	On-Die Termination for Data Signals	(d)	102 51		138 69	Ω	7
I_{LI}	Input Leakage Current				±500	μA	
SM_RCOMP0	COMP Resistance	(t)	99	100	101	Ω	8
SM_RCOMP1	COMP Resistance	(t)	24.7	24.9	25.1	Ω	8
SM_RCOMP2	COMP Resistance	(t)	128.7	130	131.3	Ω	8

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance.
6. R_{VTT_TERM} is the termination on the DIMM and in not controlled by the Processor.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
8. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.

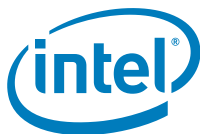


Table 41. Control Sideband and TAP Signal Group DC Specifications

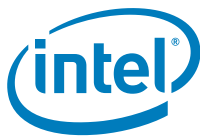
Symbol	Alpha Group	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	(m),(n),(p),(qa),(qb),(s)	Input Low Voltage			$0.64 * V_{TT}$	V	2
V_{IH}	(m),(n),(p),(qa),(qb),(s)	Input High Voltage	$0.76 * V_{TT}$			V	2,4
V_{IL}	(g)	Input Low Voltage			$0.40 * V_{TT}$	V	2
V_{IH}	(g)	Input High Voltage	$0.75 * V_{TT}$			V	2,4
V_{IL}	(ja)	Input Low Voltage			$0.25 * V_{TT}$		2
V_{IH}	(ja)	Input High Voltage	$0.75 * V_{TT}$			V	2,4
V_{IL}	(jb)	Input Low Voltage			0.29		2
V_{IH}	(jb)	Input High Voltage	0.87			V	2,4
V_{OL}	(k),(l),(n),(p),(r),(s),(h),(i)	Output Low Voltage			$V_{TT} * R_{ON} / (R_{ON} + R_{SYS_TERM})$	V	2,6
V_{OH}	(k),(l),(n),(p),(r),(s),(h),(i)	Output High Voltage	V_{TT}			V	2,4
R_{ON}		Buffer on Resistance	10		18	Ω	
I_{LI}	(ja),(jb),(m),(n),(p),(qa),(s),(t),(g)	Input Leakage Current			±200	µA	3
I_{LI}	(qb)	Input Leakage Current			±100	µA	3
COMP0	(t)	COMP Resistance	49.4	49.9	50.4	Ω	5
COMP1	(t)	COMP Resistance	49.4	49.9	50.4	Ω	5
COMP2	(t)	COMP Resistance	19.8	20	20.2	Ω	5
COMP3	(t)	COMP Resistance	19.8	20	20.2	Ω	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
3. For V_{IN} between “0” V and V_{TT}. Measured when the driver is tristated.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications.
5. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.
6. R_{SYS_TERM} is the system termination on the signal.

Table 42. PCI Express DC Specifications

Symbol	Alpha Group	Parameter	Min	Typ	Max	Units	Notes[1]
$V_{TX-DIFF-p-p-LOW}$	(ad)	Low Power Differential Peak-to-Peak Tx Voltage Swing	0.4		1.2	V	3
$V_{TX-DIFF-p-p}$	(ad)	Differential Peak-to-Peak Tx Voltage Swing	0.8		1.2	V	3
$V_{TX_CM-AC-p}$	(ad)	Tx AC Peak Common Mode Output Voltage (Gen 1 Only)			20	mV	1,2,6
$V_{TX_CM-AC-p-p}$	(ad)	Tx AC Peak Common Mode Output Voltage (Gen 2 Only)			100	mV	1,2
$Z_{TX-DIFF-DC}$	(ad)	DC Differential Tx Impedance (Gen 1 Only)	80		120	Ω	1,10
$Z_{TX-DIFF-DC}$	(ad)	DC Differential Tx Impedance (Gen 2 Only)			120	Ω	1,10
Z_{RX-DC}	(ac)	DC Common Mode Rx Impedance	40		60	Ω	1,8,9
$Z_{RX-DIFF-DC}$	(ac)	DC Differential Rx Impedance (Gen1 Only)	80		120	Ω	1
$V_{RX-DIFFp-p}$	(ac)	Differential Rx Input Peak-to-Peak Voltage (Gen 1 only)	0.175		1.2	V	1,11
$V_{RX-DIFFp-p}$	(ac)	Differential Rx Input Peak-to-Peak Voltage (Gen 2 Only)	0.120		1.2	V	1,11
$V_{RX_CM-AC-p}$	(ac)	Rx AC Peak Common Mode Input Voltage			150	mV	1,7
PEG_ICOMPO	(ae)	Comp Resistance	49.5	50	50.5	Ω	4,5
PEG_ICOMPI	(ae)	Comp Resistance	49.5	50	50.5	Ω	4,5
PEG_RCOMPO	(ae)	Comp Resistance	49.5	50	50.5	Ω	4,5
PEG_RBIAS	(ae)	Comp Resistance	742.5	750	757.5	Ω	4,5

NOTES:
1. Refer to the *PCI Express Base Specification* for more details.
2. $V_{TX-AC-CM-PP}$ and $V_{TX-AC-CM-P}$ are defined in the *PCI Express Base Specification*. Measurement is made over at least 10^6 UI.
3. As measured with compliance test load. Defined as $2*|V_{TXD+} - V_{TXD-}|$.
4. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.
5. PEG_ICOMPO, PEG_ICOMPI, PEG_RCOMPO are the same resistor
6. RMS value.
7. Measured at Rx pins into a pair of 50-Ω terminations into ground. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.
8. DC impedance limits are needed to guarantee Receiver detect.
9. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
10. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
11. This specification is the same as V_{RX-EYE}



7.10.2 V_{CC} Validation

The following calculation for spec minimum V_{CC} voltage is applicable at V_{CC_SENSE}/ V_{SS_SENSE} with 20-MHz bandwidth limiting.

$$V\min = VID - I_{CCMAX} * Slope_{LL} - x\% * VID - ripple$$

VID under maximum load, x% set-point tolerance, and ripple have to be measured on the system under test. Use the loadline slope and I_{CCMAX} for the minimum voltage Vmin calculation. It might be difficult to reach max current in lab environment. Please try different stresses on V_{CC_CORE} rail. Compare the measured Vmin to the calculated Vmin to determine if system passes or fails.

The following step-by-step procedure is recommended for minimum V_{CC} and V_{AXG} validation. Step 1 to 5 is for the calculation of spec minimum voltage and step 6 is to collect actual minimum voltage on the system under test.

1. Measure the DC voltage at test points with V_{RTT} or Chroma load. Calculate set-point tolerance.
2. Land differential probes at the designated test points under CPU on the secondary layer.
3. Operating the CPU with maximum load on all threads.
4. Measure VID signals and find the corresponding voltage in EDS. The VID signals should be very stable with max load.
5. Measure ripple. 20-MHz bandwidth limiting or Low-pass filter function can be applied.

Set manual trigger on the voltage waveform. Lower the trigger level slowly to capture the worst case Vmin with 20-MHz bandwidth limiting. Low-pass filtering function with 20-MHz cut-off frequency can be used for bandwidth limiting.

7.10.3 Uncore Voltage Validation

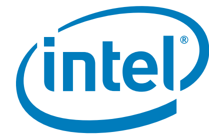
AC tolerance is defined at power/ground pins where the voltage transient has to be within spec with 20-MHz bandwidth limiting. DC tolerance is defined at power/ground pins where the DC voltage error has to be within spec. The new tolerance spec for V_{TT} rail defined at V_{TT_SENSE}/$V_{SS_SENSE_VTT}$ pins with 20-MHz bandwidth limiting has to be met along with the tolerance spec defined at power/ground pins.

The following procedure is recommended for DC tolerance validation.

1. Connect Chroma load
2. Start at 0 A
3. Measure DC voltage at test points with multimeter.
4. Increase load current by small step and re-measure DC voltage again till reach spec maximum current. Check if all voltage points are within DC tolerance spec.

The following procedure is recommended for AC tolerance validation.

1. Land differential probes at test points under CPU on the secondary layer.
2. Operate the CPU with maximum load on all threads. For V_{DDQ}, try Mem stress and other DDR stresses
3. Measure the average voltage on scope with at least 2 μs/div



4. Set manual trigger on the voltage waveform.

- Lower the trigger level slowly to capture the worst case V_{MIN} with 20-MHz bandwidth limiting.
  - Check Vmin against min voltage spec
  - Droop (undershoot) = V_{AVG}-V_{MIN} has to be within AC tolerance spec
- Raise the trigger level slowly to capture the worst case V_{MAX} with 20-MHz bandwidth limiting.
  - Check V_{MAX} against max voltage spec
  - Overshoot = V_{MAX}-V_{AVG} has to be within AC tolerance spec

7.11 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external Adaptive Thermal Monitor devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read the DTS temperature for thermal management and fan speed control.

7.11.1 DC Characteristics

The PECI interface operates at a nominal voltage set by V_{TT}. The set of DC electrical specifications shown in Table 43 is used with devices normally operating from a V_{TT} interface supply. V_{TT} nominal levels will vary between processor families. All PECI devices will operate at the V_{TT} level determined by the processor installed in the system. For specific nominal V_{TT} levels, refer to Table 40.

Table 43. PECI DC Electrical Limits

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{in}	Input Voltage Range	-0.150	V_{TT}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{TT}	N/A	V	
V_n	Negative-edge Threshold Voltage	0.275 * V_{TT}	0.500 * V_{TT}	V	
V_p	Positive-edge Threshold Voltage	0.550 * V_{TT}	0.725 * V_{TT}	V	
I_{source}	High-Level Output Source (V_{OH} = 0.75 * V_{TT})	-6.0	N/A	mA	
I_{sink}	Low-Level Output Sink (V_{OL} = 0.25 * V_{TT})	0.5	1.0	mA	
I_{leak+}	High-Impedance State Leakage to V_{TT} (V_{leak} = V_{OL})	N/A	100	µA	2
I_{leak-}	High-Impedance Leakage to GND (V_{leak} = V_{OH})	N/A	100	µA	2
C_{bus}	Bus Capacitance Per Node	N/A	10	pF	
V_{noise}	Signal Noise Immunity above 300 MHz	0.1 * V_{TT}	N/A	V_{p-p}	

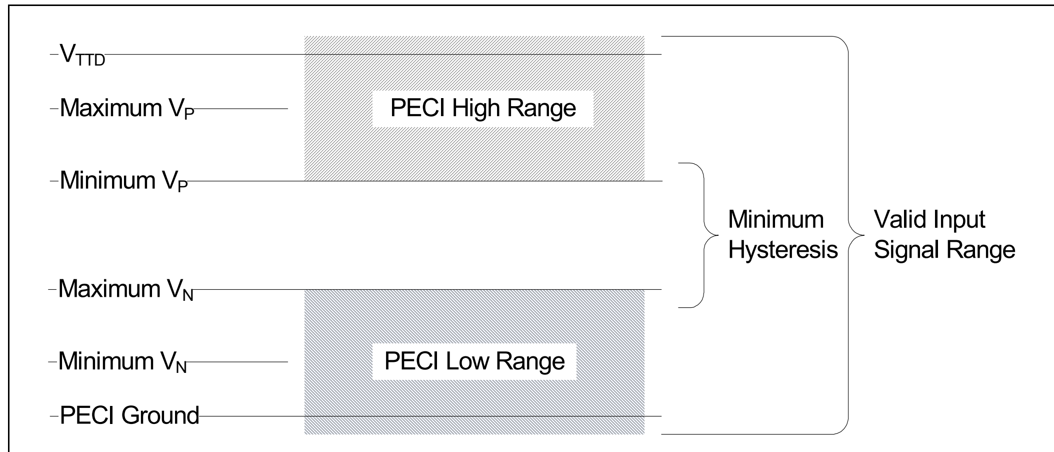
NOTES: See next page

1. V_{TT} supplies the PECI interface. PECI behavior does not affect V_{TT} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.

7.11.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 13 as a guide for input buffer design.

Figure 13. Input Device Hysteresis



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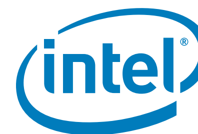


8 Processor Pin and Signal Information

8.1 Processor Pin Assignments

- Table 45 provides a listing of all processor pins ordered alphabetically by pin name for the rPGA988A package.
- Table 46 provides a listing of all processor pins ordered alphabetically by pin number for the rPGA988A package.
- Figure 14, Figure 15, Figure 16, Figure 17 show the Top-Down view of the rPGA988A pinmap.

Table 44. Pins Unused by the Intel Core i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series on the rPGA988A Package

GFX_DPRSLPVR
GFX_IMON
GFX_VID[6:0]
GFX_VR_EN
SA_DM[7:0], SB_DM[7:0]
DPLL_REF_SSCLK, DPLL_REF_SSCLK#
FDI_FSYNC[1:0]
FDI_LSYNC[1:0]
FDI_INT
FDI_TX[7:0], FDI_TX#[7:0]
VAXG
VAXG_SENSE, VSSAXG_SENSE
VCCPWRGOOD_1
CFG[12]
COMP1, COMP2, COMP3

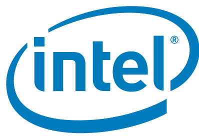


Figure 14. rPGA988A Pinmap (Top View, Upper-Left Quadrant)

	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
AT	VSS_NCTF	RSVD_NCTF	RSVD_NCTF	RSVD	RSVD	BCLK_ITP#	TDI	PRDY#	TRST#	COMP0	GFX_DPRSLPVR	COMP2	COMP3	VSSAXG_SENSE	VAXG	VSS	VAXG	VAXG
AR	RSVD_NCTF	VSS_NCTF	RSVD	RSVD	VSS	BCLK_ITP	TDI_M	VSS	TDO	VSS	GFX_VR_EN	VSS	VSS	VAXG_SENSE	VAXG	VSS	VAXG	VAXG
AP	RSVD_NCTF	VSS	RSVD	RSVD	CFG[2]	RSVD	TDO_M	TMS	PREQ#	RESET_OBS#	RSVD	GFX_VID[5]	GFX_VID[3]	GFX_VID[1]	VAXG	VSS	VAXG	VAXG
AN	ISENSE	VSS	PSI#	CFG[13]	VSS	CFG[12]	CFG[6]	TCK	VCCPWRGOOD_0	PROCHOT#	DBR#	GFX_VID[6]	VSS	GFX_VID[2]	VAXG	VSS	VAXG	VAXG
AM	VID[6]	PROC_DPRSLPVR	VID[5]	CFG[7]	CFG[5]	CFG[0]	VSS	CFG[1]	VSS	TAPPWRGOOD	VSS	GFX_IMON	GFX_VID[4]	GFX_VID[0]	VAXG	VSS	VAXG	VAXG
AL	VID[3]	VSS	VID[4]	CFG[3]	VSS	CFG[4]	RSVD	RSVD	RSVD	RSVD_TP	RSVD	RSVD	VSS	RSVD	VAXG	VSS	VAXG	VAXG
AK	VID[0]	VID[2]	VID[1]	CFG[8]	CFG[9]	CFG[17]	VSS	CFG[10]	VSS	RSVD_TP	VSS	BPM#[2]	BPM#[6]	BPM#[1]	VAXG	VSS	VAXG	VAXG
AJ	VSS_SENSE	VCC_SENSE	RSVD	CFG[14]	VSS	CFG[16]	CFG[15]	CFG[11]	RSVD	RSVD	BPM#[4]	BPM#[3]	VSS	BPM#[0]	VAXG	VSS	VAXG	VAXG
AH	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	SKTOCC#	BPM#[7]	BPM#[5]	VAXG	VSS	VAXG	VAXG
AG	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AF	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AB	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AA	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
Y	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
V	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								

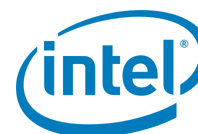


Figure 15. rPGA988A Pinmap (Top View, Upper-Right Quadrant)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS	VAXG	PECI	SA_DQ[59]	SA_DQS#[7]	SA_DQ[60]	SA_DQ[54]	SB_DQ[63]	SB_DQ[59]	SB_DM[7]	SB_DQ[60]	SB_DQ[55]	SB_DQ[54]	SB_DQ[50]	RSVD_NCTF	RSVD_TP	VSS_NCTF	AT
VSS	VAXG	VSS	SA_DQ[62]	SA_DQS[7]	VSS	SA_DQ[50]	SB_DQ[62]	VSS	SB_DQS#[7]	SB_DQS[7]	VSS	SB_DQS#[6]	SB_DM[6]	VSS	RSVD_NCTF	RSVD_NCTF	AR
VSS	VAXG	PM_EXT_TS#[1]	SA_DQ[63]	VSS	SA_DQ[55]	SA_DQS#[6]	VSS	SB_DQ[61]	SB_DQ[58]	VSS	SB_DQ[57]	SB_DQS[6]	VSS	SB_DQ[48]	VSS	RSVD_NCTF	AP
VSS	VAXG	PM_EXT_TS#[0]	VCCPWRGOOD_1	SA_DM[7]	SA_DQ[57]	SA_DQS[6]	SA_DM[6]	SA_DQ[53]	SA_DQ[48]	SB_DQ[56]	SB_DQ[51]	SB_DQ[49]	SB_DQ[52]	SB_DQ[53]	SB_DQ[43]	SM_RCOMP[2]	AN
VSS	VAXG	VTTPWRGOOD	VSS	SA_DQ[58]	SA_DQ[56]	VSS	SA_DQ[49]	SA_DQ[52]	VSS	SA_DM[5]	SB_DQ[42]	VSS	SB_DQ[46]	SB_DQ[47]	VSS	SM_RCOMP[1]	AM
VSS	VAXG	PM_SYNC	RSTIN#	SA_DQ[61]	VSS	SA_DQ[51]	SA_DQ[42]	VSS	SA_DQ[47]	SA_DQ[45]	VSS	SB_DQS[5]	SB_DQS#[5]	VSS	SB_DM[5]	SM_RCOMP[0]	AL
VSS	VAXG	THERMTRIP#	CATERR#	SM_DRAMPWROK	SA_DQ[43]	SA_DQ[46]	SA_DQS[5]	SA_DQS#[5]	SA_DQ[44]	SA_DQ[35]	SA_DQ[34]	SB_DQ[44]	SB_DQ[41]	SB_DQ[40]	SB_DQ[45]	SB_DQ[35]	AK
VSS	VAXG	RSVD	VSS	RSVD_TP	RSVD_TP	VSS	SA_DQ[40]	SA_DQ[41]	VSS	SA_DQ[38]	SA_DQ[39]	VSS	SB_DQ[38]	SB_DQ[34]	VSS	VDDQ	AJ
VSS	VAXG	RSVD	VTT0	VSS	VTT0	VTT0	VTT0	VSS	SA_DQS[4]	SA_DQS#[4]	VSS	SA_DQ[32]	SB_DQ[39]	VSS	SB_DQS#[4]	SB_DM[4]	AH
							VSS	RSVD	SA_MA[13]	RSVD_TP	SA_DM[4]	SA_DQ[37]	SB_DQ[36]	SB_DQ[37]	SB_DQS[4]	SB_DQ[33]	AG
							VTT0	SA_ODT[1]	VSS	SB_MA[13]	SA_DQ[36]	SA_DQ[33]	VSS	SB_DQ[32]	VSS	VDDQ	AF
							VTT0	SA_WE#	SA_CS#[1]	VDDQ	VSS	RSVD_TP	VDDQ	RSVD_TP	SA_CS#[0]	SA_CAS#	AE
							VSS	RSVD_TP	SA_ODT[0]	RSVD_TP	SB_CS#[1]	RSVD_TP	SA_MA[10]	RSVD_TP	RSVD_TP	SB_ODT[1]	AD
							VTT0	RSVD	VSS	SB_ODT[0]	SB_WE#	SB_CAS#	VSS	SA_BS[0]	VSS	VDDQ	AC
							VTT0	RSVD	SB_CS#[0]	VDDQ	VSS	SB_MA[10]	VDDQ	SA_RAS#	SA_BS[1]	SB_BS[0]	AB
							VSS	SA_MA[5]	SA_MA[2]	SA_CK#[0]	SA_CK[0]	RSVD_TP	RSVD_TP	SA_MA[3]	RSVD_TP	RSVD_TP	AA
							VTT0	SA_MA[8]	VSS	SB_RAS#	SA_CK[1]	SA_CK#[1]	VSS	SA_MA[0]	VSS	VDDQ	Y
							VTT0	SB_CK#[0]	SB_CK[0]	VDDQ	VSS	SB_BS[1]	VDDQ	RSVD_TP	RSVD_TP	SA_MA[1]	W
							VSS	SA_MA[15]	SA_MA[6]	SB_CK[1]	SB_CK#[1]	RSVD_TP	RSVD_TP	SB_MA[3]	SB_MA[1]	SA_MA[4]	V

Figure 16. rPGA988A Pinmap (Top View, Lower-Left Quadrant)

	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
U	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
T	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
R	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
P	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
M	PEG_TX#[1]	PEG_TX[1]	PEG_TX#[2]	PEG_TX[2]	PEG_TX[4]	PEG_TX#[3]	PEG_TX#[6]	PEG_TX[6]	RSVD	VCCPLL								
L	VSS	PEG_TX[0]	PEG_TX#[0]	VSS	PEG_TX#[4]	PEG_TX[3]	VSS	RSVD	VCCPLL	VCCPLL								
K	PEG_RX#[0]	VSS	VSS	PEG_TX#[5]	PEG_TX[5]	VSS	PEG_TX#[8]	PEG_TX[8]	VSS	VTT1								
J	PEG_RX[0]	PEG_RX#[1]	PEG_RX#[2]	VSS	PEG_TX#[7]	VSS	RSVD	RSVD	VTT1	VTT1	VTT1	VTT1	VTT1	VTT1	VSS	VTT1	VSS	VTT1
H	VSS	PEG_RX[1]	PEG_RX[2]	VSS	PEG_TX[7]	PEG_TX#[9]	PEG_TX#[10]	VSS	VTT1	VSS	VTT1	VSS	DMI_TX#[3]	VSS	VTT1	VTT1	VTT1	VSS
G	PEG_RX#[3]	VSS	PEG_RX[4]	PEG_RX#[4]	VSS	PEG_TX[9]	PEG_TX[10]	VTT1	VTT1	VTT1	RSVD	DMI_TX#[1]	DMI_TX[3]	FDI_TX[4]	FDI_TX#[4]	VSS	FDI_TX[7]	FDI_TX#[7]
F	PEG_RX[3]	PEG_RX#[5]	PEG_RX[8]	PEG_RX[6]	PEG_RX#[6]	VSS	PEG_TX#[11]	PEG_TX[11]	VSS	VTT1	VSS	DMI_TX[1]	DMI_TX#[2]	VSS	FDI_TX#[6]	FDI_TX[6]	VSS	FDI_LSYNC[0]
E	VSS	PEG_RX[5]	PEG_RX#[8]	VSS	RSVD	RSVD	VSS	PEG_TX#[12]	PEG_TX[12]	VTT1	VTT1	VSS	DMI_TX[2]	FDI_TX#[0]	VSS	FDI_TX[5]	FDI_TX#[5]	VSS
D	PEG_RX#[7]	PEG_RX[7]	VSS	PEG_RX#[10]	PEG_RX[10]	VSS	PEG_TX#[13]	PEG_TX[13]	PEG_TX#[14]	VSS	DMI_TX[0]	DMI_TX#[0]	DMI_RX[1]	FDI_TX[0]	FDI_TX#[1]	FDI_TX[2]	FDI_TX#[2]	FDI_TX#[3]
C	RSVD_NCTF	VSS	PEG_RX#[9]	VSS	PEG_RX#[12]	PEG_RX[12]	VSS	VSS	PEG_TX[14]	PEG_TX#[15]	PEG_TX[15]	VSS	DMI_RX#[1]	VSS	FDI_TX[1]	VSS	VSS	FDI_TX[3]
B	RSVD_NCTF	VSS_NCTF	PEG_RX[9]	PEG_RX#[11]	VSS	PEG_RX#[14]	PEG_RX[14]	PEG_RX#[13]	PEG_RCOMPO	PEG_ICOMPI	VSS	DMI_RX[0]	DMI_RX[2]	DMI_RX#[2]	VSS	RSVD	RSVD	VSS
A	VSS_NCTF	RSVD_NCTF	RSVD_NCTF	PEG_RX[11]	PEG_RX#[15]	PEG_RX[15]	VSS	PEG_RX[13]	VSS	PEG_ICOMPO	PEG_RBIAS	DMI_RX#[0]	VSS	DMI_RX[3]	DMI_RX#[3]	RSVD	RSVD	DPLL_REF_SSCLK

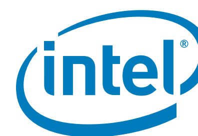


Figure 17. rPGA988A Pinmap (Top View, Lower-Right Quadrant)

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
U								VTT0	RSVD	VSS	SA_BS[2]	SA_MA[9]	SB_MA[0]	VSS	SA_MA[12]	VSS	VDDQ
T								VTT0	RSVD	SB_MA[5]	VDDQ	VSS	SB_MA[2]	VDDQ	SA_MA[14]	SA_MA[11]	SA_MA[7]
R								VSS	RSVD_TP	RSVD_TP	SB_BS[2]	SB_MA[7]	SB_MA[9]	SB_MA[8]	SB_MA[12]	SB_MA[6]	SB_MA[4]
P								VTT0	SA_DQ[31]	VSS	SA_CKE[0]	SA_CKE[1]	SB_MA[14]	VSS	SB_MA[11]	VSS	VDDQ
N								VTT0	SA_DQS#[3]	SA_DQ[30]	VDDQ	VSS	SB_DQ[31]	VDDQ	RSVD_TP	RSVD_TP	SB_MA[15]
M								VSS	SA_DQS[3]	SA_DQ[26]	SA_DM[3]	SA_DQ[25]	SB_DQS[3]	SB_DQ[30]	SB_CKE[0]	SB_CKE[1]	SB_DQ[27]
L								VTT0	SA_DQ[27]	VSS	SA_DQ[24]	SA_DQ[28]	VSS	SB_DQS#[3]	SB_DQ[26]	VSS	VDDQ
K								VTT0	VSS	SA_DQ[29]	SA_DQ[18]	VSS	SB_DQ[28]	SB_DQ[29]	VSS	SB_DQ[25]	SB_DM[3]
J	SA_DIMM_VREF	VTT0	VTT0	VTT0	VTT0	VTT0	VTT0	SA_DQ[23]	SA_DQS#[2]	SA_DQ[19]	SA_DQ[22]	SB_DQ[18]	SB_DQ[24]	SB_DQS#[2]	SB_DQ[19]	SB_DQ[22]	SB_DQ[23]
H	SB_DIMM_VREF	RSVD_TP	VSS	VTT0	VSS	VTT0	VSS	SA_DQ[16]	SA_DQS[2]	VSS	SA_DM[2]	SB_DQ[16]	VSS	SB_DQS[2]	SB_DM[2]	VSS	VDDQ
G	RSVD	COMP1	VTT_SELECT	VTT0	VTT0	VTT0	VTT0	SA_DQ[21]	VSS	SA_DQ[17]	SA_DQ[20]	VSS	SB_DQ[21]	SB_DQ[15]	VSS	SB_DQ[17]	SB_DQ[20]
F	FDI_FSYNC[0]	VSS	RSVD_TP	VTT0	VTT0	VTT0	VTT0	SA_DQ[9]	SA_DQS[1]	SA_DQS#[1]	SA_DQ[11]	SM_DRAMRST#	SB_DQ[13]	SB_DQS#[1]	SB_DQ[14]	SB_DQ[10]	SB_DQ[11]
E	FDI_FSYNC[1]	PEG_CLK	RSVD_TP	VTT0	VSS	VTT0	VSS	SA_DQ[6]	SA_DQ[12]	VSS	SA_DQ[14]	SA_DQ[10]	VSS	SB_DQ[4]	SB_DQS[1]	VSS	SB_DM[1]
D	FDI_LSYNC[1]	PEG_CLK#	RSVD	VTT0	VTT0	VTT0	VTT0	SA_DQ[5]	VSS	SA_DQ[8]	SA_DM[1]	VSS	SB_DQS#[0]	SB_DM[0]	VSS	SB_DQ[9]	SB_DQ[8]
C	FDI_INT	VSS	RSVD	VTT0	VTT0	VTT0	VTT0	SA_DQ[1]	SA_DQS#[0]	SA_DQS[0]	SA_DQ[2]	SA_DQ[15]	SB_DQS[0]	SB_DQ[7]	SB_DQ[2]	SB_DQ[12]	RSVD_NCTF
B	VSS	BCLK#	VTT_SENSE	VTT0	VSS	VTT0	VSS	SA_DQ[4]	SA_DM[0]	VSS	SA_DQ[13]	VSS	SB_DQ[0]	VSS	SB_DQ[3]	VSS_NCTF	VSS_NCTF
A	DPLL_REF_SSCLK#	BCLK	VSS_SENSE_VTT	VTT0	VTT0	VTT0	VTT0	SA_DQ[0]	VSS	SA_DQ[7]	SA_DQ[3]	SB_DQ[5]	SB_DQ[1]	SB_DQ[6]	RSVD_NCTF	KEY	

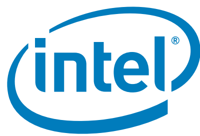


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
BCLK	A16	DIFF CLK	I
BCLK_ITP	AR30	DIFF CLK	O
BCLK_ITP#	AT30	DIFF CLK	O
BCLK#	B16	DIFF CLK	I
BPM#[0]	AJ22	GTL	I/O
BPM#[1]	AK22	GTL	I/O
BPM#[2]	AK24	GTL	I/O
BPM#[3]	AJ24	GTL	I/O
BPM#[4]	AJ25	GTL	I/O
BPM#[5]	AH22	GTL	I/O
BPM#[6]	AK23	GTL	I/O
BPM#[7]	AH23	GTL	I/O
CATERR#	AK14	GTL	I/O
CFG[0]	AM30	CMOS	I
CFG[1]	AM28	CMOS	I
CFG[2]	AP31	CMOS	I
CFG[3]	AL32	CMOS	I
CFG[4]	AL30	CMOS	I
CFG[5]	AM31	CMOS	I
CFG[6]	AN29	CMOS	I
CFG[7]	AM32	CMOS	I
CFG[8]	AK32	CMOS	I
CFG[9]	AK31	CMOS	I
CFG[10]	AK28	CMOS	I
CFG[11]	AJ28	CMOS	I
CFG[12]	AN30	CMOS	I
CFG[13]	AN32	CMOS	I
CFG[14]	AJ32	CMOS	I
CFG[15]	AJ29	CMOS	I
CFG[16]	AJ30	CMOS	I
CFG[17]	AK30	CMOS	I
COMP0	AT26	Analog	I
COMP1	G16	Analog	I
COMP2	AT24	Analog	I
COMP3	AT23	Analog	I
DBR#	AN25		O
DMI_RX[0]	B24	DMI	I
DMI_RX[1]	D23	DMI	I
DMI_RX[2]	B23	DMI	I

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
DMI_RX[3]	A22	DMI	I
DMI_RX#[0]	A24	DMI	I
DMI_RX#[1]	C23	DMI	I
DMI_RX#[2]	B22	DMI	I
DMI_RX#[3]	A21	DMI	I
DMI_TX[0]	D25	DMI	O
DMI_TX[1]	F24	DMI	O
DMI_TX[2]	E23	DMI	O
DMI_TX[3]	G23	DMI	O
DMI_TX#[0]	D24	DMI	O
DMI_TX#[1]	G24	DMI	O
DMI_TX#[2]	F23	DMI	O
DMI_TX#[3]	H23	DMI	O
DPLL_REF_SSCLK	A18	DIFF CLK	I
DPLL_REF_SSCLK#	A17	DIFF CLK	I
FDI_FSYNC[0]	F17	CMOS	I
FDI_FSYNC[1]	E17	CMOS	I
FDI_INT	C17	CMOS	I
FDI_LSYNC[0]	F18	CMOS	I
FDI_LSYNC[1]	D17	CMOS	I
FDI_TX[0]	D22	FDI	O
FDI_TX[1]	C21	FDI	O
FDI_TX[2]	D20	FDI	O
FDI_TX[3]	C18	FDI	O
FDI_TX[4]	G22	FDI	O
FDI_TX[5]	E20	FDI	O
FDI_TX[6]	F20	FDI	O
FDI_TX[7]	G19	FDI	O
FDI_TX#[0]	E22	FDI	O
FDI_TX#[1]	D21	FDI	O
FDI_TX#[2]	D19	FDI	O
FDI_TX#[3]	D18	FDI	O
FDI_TX#[4]	G21	FDI	O
FDI_TX#[5]	E19	FDI	O
FDI_TX#[6]	F21	FDI	O
FDI_TX#[7]	G18	FDI	O
GFX_DPRSLPVR	AT25	CMOS	O
GFX_IMON	AM24	Analog	I
GFX_VID[0]	AM22	CMOS	O

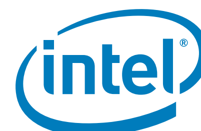


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
GFX_VID[1]	AP22	CMOS	O
GFX_VID[2]	AN22	CMOS	O
GFX_VID[3]	AP23	CMOS	O
GFX_VID[4]	AM23	CMOS	O
GFX_VID[5]	AP24	CMOS	O
GFX_VID[6]	AN24	CMOS	O
GFX_VR_EN	AR25	CMOS	O
ISENSE	AN35	Analog	I
KEY	A2		
PECI	AT15	Async	I/O
PEG_CLK	E16	DIFF CLK	I
PEG_CLK#	D16	DIFF CLK	I
PEG_ICOMPI	B26	Analog	I
PEG_ICOMPO	A26	Analog	I
PEG_RBIAS	A25	Analog	I
PEG_RCOMPO	B27	Analog	I
PEG_RX[0]	J35	PCIe	I
PEG_RX[1]	H34	PCIe	I
PEG_RX[2]	H33	PCIe	I
PEG_RX[3]	F35	PCIe	I
PEG_RX[4]	G33	PCIe	I
PEG_RX[5]	E34	PCIe	I
PEG_RX[6]	F32	PCIe	I
PEG_RX[7]	D34	PCIe	I
PEG_RX[8]	F33	PCIe	I
PEG_RX[9]	B33	PCIe	I
PEG_RX[10]	D31	PCIe	I
PEG_RX[11]	A32	PCIe	I
PEG_RX[12]	C30	PCIe	I
PEG_RX[13]	A28	PCIe	I
PEG_RX[14]	B29	PCIe	I
PEG_RX[15]	A30	PCIe	I
PEG_RX#[0]	K35	PCIe	I
PEG_RX#[1]	J34	PCIe	I
PEG_RX#[2]	J33	PCIe	I
PEG_RX#[3]	G35	PCIe	I
PEG_RX#[4]	G32	PCIe	I
PEG_RX#[5]	F34	PCIe	I
PEG_RX#[6]	F31	PCIe	I
PEG_RX#[7]	D35	PCIe	I

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
PEG_RX#[8]	E33	PCIe	I
PEG_RX#[9]	C33	PCIe	I
PEG_RX#[10]	D32	PCIe	I
PEG_RX#[11]	B32	PCIe	I
PEG_RX#[12]	C31	PCIe	I
PEG_RX#[13]	B28	PCIe	I
PEG_RX#[14]	B30	PCIe	I
PEG_RX#[15]	A31	PCIe	I
PEG_TX[0]	L34	PCIe	O
PEG_TX[1]	M34	PCIe	O
PEG_TX[2]	M32	PCIe	O
PEG_TX[3]	L30	PCIe	O
PEG_TX[4]	M31	PCIe	O
PEG_TX[5]	K31	PCIe	O
PEG_TX[6]	M28	PCIe	O
PEG_TX[7]	H31	PCIe	O
PEG_TX[8]	K28	PCIe	O
PEG_TX[9]	G30	PCIe	O
PEG_TX[10]	G29	PCIe	O
PEG_TX[11]	F28	PCIe	O
PEG_TX[12]	E27	PCIe	O
PEG_TX[13]	D28	PCIe	O
PEG_TX[14]	C27	PCIe	O
PEG_TX[15]	C25	PCIe	O
PEG_TX#[0]	L33	PCIe	O
PEG_TX#[1]	M35	PCIe	O
PEG_TX#[2]	M33	PCIe	O
PEG_TX#[3]	M30	PCIe	O
PEG_TX#[4]	L31	PCIe	O
PEG_TX#[5]	K32	PCIe	O
PEG_TX#[6]	M29	PCIe	O
PEG_TX#[7]	J31	PCIe	O
PEG_TX#[8]	K29	PCIe	O
PEG_TX#[9]	H30	PCIe	O
PEG_TX#[10]	H29	PCIe	O
PEG_TX#[11]	F29	PCIe	O
PEG_TX#[12]	E28	PCIe	O
PEG_TX#[13]	D29	PCIe	O
PEG_TX#[14]	D27	PCIe	O
PEG_TX#[15]	C26	PCIe	O

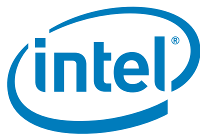


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
PM_EXT_ TS#[0]	AN15	CMOS	I
PM_EXT_ TS#[1]	AP15	CMOS	I
PM_SYNC	AL15	CMOS	I
PRDY#	AT28	Async GTL	O
PREQ#	AP27	Async GTL	I
PROC_ DPRSLPVR	AM34	CMOS	O
PROCHOT#	AN26	Async GTL	I/O
PSI#	AN33	Async CMOS	O
RESET_OBS#	AP26	Async CMOS	O
RSTIN#	AL14	CMOS	I
RSVD	A19		
RSVD	A20		
RSVD	AB9		
RSVD	AC9		
RSVD	AG9		
RSVD	AH15		
RSVD	AH25		
RSVD	AJ15		
RSVD	AJ26		
RSVD	AJ27		
RSVD	AJ33		
RSVD	AL22		
RSVD	AL24		
RSVD	AL25		
RSVD	AL27		
RSVD	AL28		
RSVD	AL29		
RSVD	AP25		
RSVD	AP30		
RSVD	AP32		
RSVD	AP33		
RSVD	AR32		
RSVD	AR33		
RSVD	AT31		
RSVD	AT32		
RSVD	B19		
RSVD	B20		

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD	C15		
RSVD	D15		
RSVD	E30		
RSVD	E31		
RSVD	G17		
RSVD	G25		
RSVD	J28		
RSVD	J29		
RSVD	L28		
RSVD	M27		
RSVD	T9		
RSVD	U9		
RSVD_NCTF	A3		
RSVD_NCTF	A33		
RSVD_NCTF	A34		
RSVD_NCTF	AP1		
RSVD_NCTF	AP35		
RSVD_NCTF	AR1		
RSVD_NCTF	AR2		
RSVD_NCTF	AR35		
RSVD_NCTF	AT3		
RSVD_NCTF	AT33		
RSVD_NCTF	AT34		
RSVD_NCTF	B35		
RSVD_NCTF	C1		
RSVD_NCTF	C35		
RSVD_TP	AA1		
RSVD_TP	AA2		
RSVD_TP	AA4		
RSVD_TP	AA5		
RSVD_TP	AD2		
RSVD_TP	AD3		
RSVD_TP	AD5		
RSVD_TP	AD7		
RSVD_TP	AD9		
RSVD_TP	AE3		
RSVD_TP	AE5		
RSVD_TP	AG7		
RSVD_TP	AJ12		
RSVD_TP	AJ13		

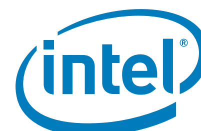


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD_TP	AK26		
RSVD_TP	AL26		
RSVD_TP	AT2		
RSVD_TP	E15		
RSVD_TP	F15		
RSVD_TP	H16		
RSVD_TP	N2		
RSVD_TP	N3		
RSVD_TP	R8		
RSVD_TP	R9		
RSVD_TP	V4		
RSVD_TP	V5		
RSVD_TP	W2		
RSVD_TP	W3		
SA_BS[0]	AC3	DDR3	O
SA_BS[1]	AB2	DDR3	O
SA_BS[2]	U7	DDR3	O
SA_CAS#	AE1	DDR3	O
SA_CK[0]	AA6	DDR3	O
SA_CK[1]	Y6	DDR3	O
SA_CK#[0]	AA7	DDR3	O
SA_CK#[1]	Y5	DDR3	O
SA_CKE[0]	P7	DDR3	O
SA_CKE[1]	P6	DDR3	O
SA_CS#[0]	AE2	DDR3	O
SA_CS#[1]	AE8	DDR3	O
SA_DIMM_ VREFDQ	J17	A	O
SA_DM[0]	B9	DDR3	O
SA_DM[1]	D7	DDR3	O
SA_DM[2]	H7	DDR3	O
SA_DM[3]	M7	DDR3	O
SA_DM[4]	AG6	DDR3	O
SA_DM[5]	AM7	DDR3	O
SA_DM[6]	AN10	DDR3	O
SA_DM[7]	AN13	DDR3	O
SA_DQ[0]	A10	DDR3	I/O
SA_DQ[1]	C10	DDR3	I/O
SA_DQ[2]	C7	DDR3	I/O
SA_DQ[3]	A7	DDR3	I/O
SA_DQ[4]	B10	DDR3	I/O

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_DQ[5]	D10	DDR3	I/O
SA_DQ[6]	E10	DDR3	I/O
SA_DQ[7]	A8	DDR3	I/O
SA_DQ[8]	D8	DDR3	I/O
SA_DQ[9]	F10	DDR3	I/O
SA_DQ[10]	E6	DDR3	I/O
SA_DQ[11]	F7	DDR3	I/O
SA_DQ[12]	E9	DDR3	I/O
SA_DQ[13]	B7	DDR3	I/O
SA_DQ[14]	E7	DDR3	I/O
SA_DQ[15]	C6	DDR3	I/O
SA_DQ[16]	H10	DDR3	I/O
SA_DQ[17]	G8	DDR3	I/O
SA_DQ[18]	K7	DDR3	I/O
SA_DQ[19]	J8	DDR3	I/O
SA_DQ[20]	G7	DDR3	I/O
SA_DQ[21]	G10	DDR3	I/O
SA_DQ[22]	J7	DDR3	I/O
SA_DQ[23]	J10	DDR3	I/O
SA_DQ[24]	L7	DDR3	I/O
SA_DQ[25]	M6	DDR3	I/O
SA_DQ[26]	M8	DDR3	I/O
SA_DQ[27]	L9	DDR3	I/O
SA_DQ[28]	L6	DDR3	I/O
SA_DQ[29]	K8	DDR3	I/O
SA_DQ[30]	N8	DDR3	I/O
SA_DQ[31]	P9	DDR3	I/O
SA_DQ[32]	AH5	DDR3	I/O
SA_DQ[33]	AF5	DDR3	I/O
SA_DQ[34]	AK6	DDR3	I/O
SA_DQ[35]	AK7	DDR3	I/O
SA_DQ[36]	AF6	DDR3	I/O
SA_DQ[37]	AG5	DDR3	I/O
SA_DQ[38]	AJ7	DDR3	I/O
SA_DQ[39]	AJ6	DDR3	I/O
SA_DQ[40]	AJ10	DDR3	I/O
SA_DQ[41]	AJ9	DDR3	I/O
SA_DQ[42]	AL10	DDR3	I/O
SA_DQ[43]	AK12	DDR3	I/O
SA_DQ[44]	AK8	DDR3	I/O

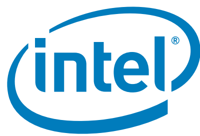


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_DQ[45]	AL7	DDR3	I/O
SA_DQ[46]	AK11	DDR3	I/O
SA_DQ[47]	AL8	DDR3	I/O
SA_DQ[48]	AN8	DDR3	I/O
SA_DQ[49]	AM10	DDR3	I/O
SA_DQ[50]	AR11	DDR3	I/O
SA_DQ[51]	AL11	DDR3	I/O
SA_DQ[52]	AM9	DDR3	I/O
SA_DQ[53]	AN9	DDR3	I/O
SA_DQ[54]	AT11	DDR3	I/O
SA_DQ[55]	AP12	DDR3	I/O
SA_DQ[56]	AM12	DDR3	I/O
SA_DQ[57]	AN12	DDR3	I/O
SA_DQ[58]	AM13	DDR3	I/O
SA_DQ[59]	AT14	DDR3	I/O
SA_DQ[60]	AT12	DDR3	I/O
SA_DQ[61]	AL13	DDR3	I/O
SA_DQ[62]	AR14	DDR3	I/O
SA_DQ[63]	AP14	DDR3	I/O
SA_DQS[0]	C8	DDR3	I/O
SA_DQS[1]	F9	DDR3	I/O
SA_DQS[2]	H9	DDR3	I/O
SA_DQS[3]	M9	DDR3	I/O
SA_DQS[4]	AH8	DDR3	I/O
SA_DQS[5]	AK10	DDR3	I/O
SA_DQS[6]	AN11	DDR3	I/O
SA_DQS[7]	AR13	DDR3	I/O
SA_DQS#[0]	C9	DDR3	I/O
SA_DQS#[1]	F8	DDR3	I/O
SA_DQS#[2]	J9	DDR3	I/O
SA_DQS#[3]	N9	DDR3	I/O
SA_DQS#[4]	AH7	DDR3	I/O
SA_DQS#[5]	AK9	DDR3	I/O
SA_DQS#[6]	AP11	DDR3	I/O
SA_DQS#[7]	AT13	DDR3	I/O
SA_MA[0]	Y3	DDR3	O
SA_MA[1]	W1	DDR3	O
SA_MA[2]	AA8	DDR3	O
SA_MA[3]	AA3	DDR3	O
SA_MA[4]	V1	DDR3	O

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_MA[5]	AA9	DDR3	O
SA_MA[6]	V8	DDR3	O
SA_MA[7]	T1	DDR3	O
SA_MA[8]	Y9	DDR3	O
SA_MA[9]	U6	DDR3	O
SA_MA[10]	AD4	DDR3	O
SA_MA[11]	T2	DDR3	O
SA_MA[12]	U3	DDR3	O
SA_MA[13]	AG8	DDR3	O
SA_MA[14]	T3	DDR3	O
SA_MA[15]	V9	DDR3	O
SA_ODT[0]	AD8	DDR3	O
SA_ODT[1]	AF9	DDR3	O
SA_RAS#	AB3	DDR3	O
SA_WE#	AE9	DDR3	O
SB_BS[0]	AB1	DDR3	O
SB_BS[1]	W5	DDR3	O
SB_BS[2]	R7	DDR3	O
SB_CAS#	AC5	DDR3	O
SB_CK[0]	W8	DDR3	O
SB_CK[1]	V7	DDR3	O
SB_CK#[0]	W9	DDR3	O
SB_CK#[1]	V6	DDR3	O
SB_CKE[0]	M3	DDR3	O
SB_CKE[1]	M2	DDR3	O
SB_CS#[0]	AB8	DDR3	O
SB_CS#[1]	AD6	DDR3	O
SB_DIMM_ VREFDQ	H17	A	O
SB_DM[0]	D4	DDR3	O
SB_DM[1]	E1	DDR3	O
SB_DM[2]	H3	DDR3	O
SB_DM[3]	K1	DDR3	O
SB_DM[4]	AH1	DDR3	O
SB_DM[5]	AL2	DDR3	O
SB_DM[6]	AR4	DDR3	O
SB_DM[7]	AT8	DDR3	O
SB_DQ[0]	B5	DDR3	I/O
SB_DQ[1]	A5	DDR3	I/O
SB_DQ[2]	C3	DDR3	I/O
SB_DQ[3]	B3	DDR3	I/O

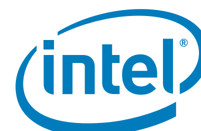


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SB_DQ[4]	E4	DDR3	I/O
SB_DQ[5]	A6	DDR3	I/O
SB_DQ[6]	A4	DDR3	I/O
SB_DQ[7]	C4	DDR3	I/O
SB_DQ[8]	D1	DDR3	I/O
SB_DQ[9]	D2	DDR3	I/O
SB_DQ[10]	F2	DDR3	I/O
SB_DQ[11]	F1	DDR3	I/O
SB_DQ[12]	C2	DDR3	I/O
SB_DQ[13]	F5	DDR3	I/O
SB_DQ[14]	F3	DDR3	I/O
SB_DQ[15]	G4	DDR3	I/O
SB_DQ[16]	H6	DDR3	I/O
SB_DQ[17]	G2	DDR3	I/O
SB_DQ[18]	J6	DDR3	I/O
SB_DQ[19]	J3	DDR3	I/O
SB_DQ[20]	G1	DDR3	I/O
SB_DQ[21]	G5	DDR3	I/O
SB_DQ[22]	J2	DDR3	I/O
SB_DQ[23]	J1	DDR3	I/O
SB_DQ[24]	J5	DDR3	I/O
SB_DQ[25]	K2	DDR3	I/O
SB_DQ[26]	L3	DDR3	I/O
SB_DQ[27]	M1	DDR3	I/O
SB_DQ[28]	K5	DDR3	I/O
SB_DQ[29]	K4	DDR3	I/O
SB_DQ[30]	M4	DDR3	I/O
SB_DQ[31]	N5	DDR3	I/O
SB_DQ[32]	AF3	DDR3	I/O
SB_DQ[33]	AG1	DDR3	I/O
SB_DQ[34]	AJ3	DDR3	I/O
SB_DQ[35]	AK1	DDR3	I/O
SB_DQ[36]	AG4	DDR3	I/O
SB_DQ[37]	AG3	DDR3	I/O
SB_DQ[38]	AJ4	DDR3	I/O
SB_DQ[39]	AH4	DDR3	I/O
SB_DQ[40]	AK3	DDR3	I/O
SB_DQ[41]	AK4	DDR3	I/O
SB_DQ[42]	AM6	DDR3	I/O
SB_DQ[43]	AN2	DDR3	I/O

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SB_DQ[44]	AK5	DDR3	I/O
SB_DQ[45]	AK2	DDR3	I/O
SB_DQ[46]	AM4	DDR3	I/O
SB_DQ[47]	AM3	DDR3	I/O
SB_DQ[48]	AP3	DDR3	I/O
SB_DQ[49]	AN5	DDR3	I/O
SB_DQ[50]	AT4	DDR3	I/O
SB_DQ[51]	AN6	DDR3	I/O
SB_DQ[52]	AN4	DDR3	I/O
SB_DQ[53]	AN3	DDR3	I/O
SB_DQ[54]	AT5	DDR3	I/O
SB_DQ[55]	AT6	DDR3	I/O
SB_DQ[56]	AN7	DDR3	I/O
SB_DQ[57]	AP6	DDR3	I/O
SB_DQ[58]	AP8	DDR3	I/O
SB_DQ[59]	AT9	DDR3	I/O
SB_DQ[60]	AT7	DDR3	I/O
SB_DQ[61]	AP9	DDR3	I/O
SB_DQ[62]	AR10	DDR3	I/O
SB_DQ[63]	AT10	DDR3	I/O
SB_DQS[0]	C5	DDR3	I/O
SB_DQS[1]	E3	DDR3	I/O
SB_DQS[2]	H4	DDR3	I/O
SB_DQS[3]	M5	DDR3	I/O
SB_DQS[4]	AG2	DDR3	I/O
SB_DQS[5]	AL5	DDR3	I/O
SB_DQS[6]	AP5	DDR3	I/O
SB_DQS[7]	AR7	DDR3	I/O
SB_DQS#[0]	D5	DDR3	I/O
SB_DQS#[1]	F4	DDR3	I/O
SB_DQS#[2]	J4	DDR3	I/O
SB_DQS#[3]	L4	DDR3	I/O
SB_DQS#[4]	AH2	DDR3	I/O
SB_DQS#[5]	AL4	DDR3	I/O
SB_DQS#[6]	AR5	DDR3	I/O
SB_DQS#[7]	AR8	DDR3	I/O
SB_MA[0]	U5	DDR3	O
SB_MA[1]	V2	DDR3	O
SB_MA[2]	T5	DDR3	O
SB_MA[3]	V3	DDR3	O

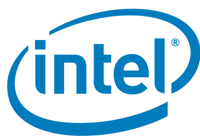


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SB_MA[4]	R1	DDR3	O
SB_MA[5]	T8	DDR3	O
SB_MA[6]	R2	DDR3	O
SB_MA[7]	R6	DDR3	O
SB_MA[8]	R4	DDR3	O
SB_MA[9]	R5	DDR3	O
SB_MA[10]	AB5	DDR3	O
SB_MA[11]	P3	DDR3	O
SB_MA[12]	R3	DDR3	O
SB_MA[13]	AF7	DDR3	O
SB_MA[14]	P5	DDR3	O
SB_MA[15]	N1	DDR3	O
SB_ODT[0]	AC7	DDR3	O
SB_ODT[1]	AD1	DDR3	O
SB_RAS#	Y7	DDR3	O
SB_WE#	AC6	DDR3	O
SKTOCC#	AH24		
SM_DRAMPWR OK	AK13	DDR3	O
SM_DRAMRST#	F6	DDR3	O
SM_RCOMP[0]	AL1	Analog	I
SM_RCOMP[1]	AM1	Analog	I
SM_RCOMP[2]	AN1	Analog	I
TAPPWRGOOD	AM26	Async CMOS	O
TCK	AN28	CMOS	I
TDI	AT29	CMOS	I
TDI_M	AR29	CMOS	I
TDO	AR27	CMOS	O
TDO_M	AP29	CMOS	O
THERMTRIP#	AK15	Async GTL	O
TMS	AP28	CMOS	I
TRST#	AT27	CMOS	I
VAXG	AH16	REF	
VAXG	AH18	REF	
VAXG	AH19	REF	
VAXG	AH21	REF	
VAXG	AJ16	REF	
VAXG	AJ18	REF	
VAXG	AJ19	REF	
VAXG	AJ21	REF	
VAXG	AK16	REF	
VAXG	AK18	REF	
VAXG	AK19	REF	
VAXG	AK21	REF	
VAXG	AL16	REF	
VAXG	AL18	REF	
VAXG	AL19	REF	
VAXG	AL21	REF	
VAXG	AM16	REF	
VAXG	AM18	REF	
VAXG	AM19	REF	
VAXG	AM21	REF	
VAXG	AN16	REF	
VAXG	AN18	REF	
VAXG	AN19	REF	
VAXG	AN21	REF	
VAXG	AP16	REF	
VAXG	AP18	REF	
VAXG	AP19	REF	
VAXG	AP21	REF	
VAXG	AR16	REF	
VAXG	AR18	REF	
VAXG	AR19	REF	
VAXG	AR21	REF	
VAXG	AT16	REF	
VAXG	AT18	REF	
VAXG	AT19	REF	
VAXG	AT21	REF	
VAXG_SENSE	AR22	Analog	O
VCC	AA26	REF	
VCC	AA27	REF	
VCC	AA28	REF	
VCC	AA29	REF	
VCC	AA30	REF	
VCC	AA31	REF	
VCC	AA32	REF	
VCC	AA33	REF	
VCC	AA34	REF	
VCC	AA35	REF	
VCC	AC26	REF	

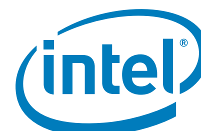


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VCC	AC27	REF	
VCC	AC28	REF	
VCC	AC29	REF	
VCC	AC30	REF	
VCC	AC31	REF	
VCC	AC32	REF	
VCC	AC33	REF	
VCC	AC34	REF	
VCC	AC35	REF	
VCC	AD26	REF	
VCC	AD27	REF	
VCC	AD28	REF	
VCC	AD29	REF	
VCC	AD30	REF	
VCC	AD31	REF	
VCC	AD32	REF	
VCC	AD33	REF	
VCC	AD34	REF	
VCC	AD35	REF	
VCC	AF26	REF	
VCC	AF27	REF	
VCC	AF28	REF	
VCC	AF29	REF	
VCC	AF30	REF	
VCC	AF31	REF	
VCC	AF32	REF	
VCC	AF33	REF	
VCC	AF34	REF	
VCC	AF35	REF	
VCC	AG26	REF	
VCC	AG27	REF	
VCC	AG28	REF	
VCC	AG29	REF	
VCC	AG30	REF	
VCC	AG31	REF	
VCC	AG32	REF	
VCC	AG33	REF	
VCC	AG34	REF	
VCC	AG35	REF	
VCC	P26	REF	

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VCC	P27	REF	
VCC	P28	REF	
VCC	P29	REF	
VCC	P30	REF	
VCC	P31	REF	
VCC	P32	REF	
VCC	P33	REF	
VCC	P34	REF	
VCC	P35	REF	
VCC	R26	REF	
VCC	R27	REF	
VCC	R28	REF	
VCC	R29	REF	
VCC	R30	REF	
VCC	R31	REF	
VCC	R32	REF	
VCC	R33	REF	
VCC	R34	REF	
VCC	R35	REF	
VCC	U26	REF	
VCC	U27	REF	
VCC	U28	REF	
VCC	U29	REF	
VCC	U30	REF	
VCC	U31	REF	
VCC	U32	REF	
VCC	U33	REF	
VCC	U34	REF	
VCC	U35	REF	
VCC	V26	REF	
VCC	V27	REF	
VCC	V28	REF	
VCC	V29	REF	
VCC	V30	REF	
VCC	V31	REF	
VCC	V32	REF	
VCC	V33	REF	
VCC	V34	REF	
VCC	V35	REF	
VCC	Y26	REF	

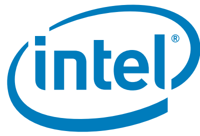


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VCC	Y27	REF	
VCC	Y28	REF	
VCC	Y29	REF	
VCC	Y30	REF	
VCC	Y31	REF	
VCC	Y32	REF	
VCC	Y33	REF	
VCC	Y34	REF	
VCC	Y35	REF	
VCC_SENSE	AJ34	Analog	O
VCCPLL	L26	REF	
VCCPLL	L27	REF	
VCCPLL	M26	REF	
VCCPWRGOOD_0	AN27	Async CMOS	I
VCCPWRGOOD_1	AN14	Async CMOS	I
VDDQ	AB4	REF	
VDDQ	AB7	REF	
VDDQ	AC1	REF	
VDDQ	AE4	REF	
VDDQ	AE7	REF	
VDDQ	AF1	REF	
VDDQ	AJ1	REF	
VDDQ	H1	REF	
VDDQ	L1	REF	
VDDQ	N4	REF	
VDDQ	N7	REF	
VDDQ	P1	REF	
VDDQ	T4	REF	
VDDQ	T7	REF	
VDDQ	U1	REF	
VDDQ	W4	REF	
VDDQ	W7	REF	
VDDQ	Y1	REF	
VID[0]/MSID[0]	AK35	CMOS	I/O
VID[1]/MSID[1]	AK33	CMOS	I/O
VID[2]/MSID[2]	AK34	CMOS	I/O
VID[3]/CSC[0]	AL35	CMOS	I/O

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VID[4]/CSC[1]	AL33	CMOS	I/O
VID[5]/CSC[2]	AM33	CMOS	I/O
VID[6]	AM35	CMOS	O
VSS	A23	GND	
VSS	A27	GND	
VSS	A29	GND	
VSS	A9	GND	
VSS	AA10	GND	
VSS	AB26	GND	
VSS	AB27	GND	
VSS	AB28	GND	
VSS	AB29	GND	
VSS	AB30	GND	
VSS	AB31	GND	
VSS	AB32	GND	
VSS	AB33	GND	
VSS	AB34	GND	
VSS	AB35	GND	
VSS	AB6	GND	
VSS	AC2	GND	
VSS	AC4	GND	
VSS	AC8	GND	
VSS	AD10	GND	
VSS	AE26	GND	
VSS	AE27	GND	
VSS	AE28	GND	
VSS	AE29	GND	
VSS	AE30	GND	
VSS	AE31	GND	
VSS	AE32	GND	
VSS	AE33	GND	
VSS	AE34	GND	
VSS	AE35	GND	
VSS	AE6	GND	
VSS	AF2	GND	
VSS	AF4	GND	
VSS	AF8	GND	
VSS	AG10	GND	
VSS	AH13	GND	
VSS	AH17	GND	

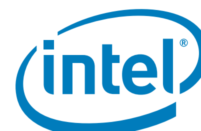


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	AH20	GND	
VSS	AH26	GND	
VSS	AH27	GND	
VSS	AH28	GND	
VSS	AH29	GND	
VSS	AH3	GND	
VSS	AH30	GND	
VSS	AH31	GND	
VSS	AH32	GND	
VSS	AH33	GND	
VSS	AH34	GND	
VSS	AH35	GND	
VSS	AH6	GND	
VSS	AH9	GND	
VSS	AJ11	GND	
VSS	AJ14	GND	
VSS	AJ17	GND	
VSS	AJ2	GND	
VSS	AJ20	GND	
VSS	AJ23	GND	
VSS	AJ31	GND	
VSS	AJ5	GND	
VSS	AJ8	GND	
VSS	AK17	GND	
VSS	AK20	GND	
VSS	AK25	GND	
VSS	AK27	GND	
VSS	AK29	GND	
VSS	AL12	GND	
VSS	AL17	GND	
VSS	AL20	GND	
VSS	AL23	GND	
VSS	AL3	GND	
VSS	AL31	GND	
VSS	AL34	GND	
VSS	AL6	GND	
VSS	AL9	GND	
VSS	AM11	GND	
VSS	AM14	GND	
VSS	AM17	GND	

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	AM2	GND	
VSS	AM20	GND	
VSS	AM25	GND	
VSS	AM27	GND	
VSS	AM29	GND	
VSS	AM5	GND	
VSS	AM8	GND	
VSS	AN17	GND	
VSS	AN20	GND	
VSS	AN23	GND	
VSS	AN31	GND	
VSS	AN34	GND	
VSS	AP10	GND	
VSS	AP13	GND	
VSS	AP17	GND	
VSS	AP2	GND	
VSS	AP20	GND	
VSS	AP34	GND	
VSS	AP4	GND	
VSS	AP7	GND	
VSS	AR12	GND	
VSS	AR15	GND	
VSS	AR17	GND	
VSS	AR20	GND	
VSS	AR23	GND	
VSS	AR24	GND	
VSS	AR26	GND	
VSS	AR28	GND	
VSS	AR3	GND	
VSS	AR31	GND	
VSS	AR6	GND	
VSS	AR9	GND	
VSS	AT17	GND	
VSS	AT20	GND	
VSS	B11	GND	
VSS	B13	GND	
VSS	B17	GND	
VSS	B18	GND	
VSS	B21	GND	
VSS	B25	GND	

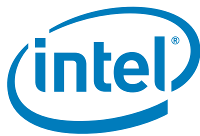


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	B31	GND	
VSS	B4	GND	
VSS	B6	GND	
VSS	B8	GND	
VSS	C16	GND	
VSS	C19	GND	
VSS	C20	GND	
VSS	C22	GND	
VSS	C24	GND	
VSS	C28	GND	
VSS	C29	GND	
VSS	C32	GND	
VSS	C34	GND	
VSS	D26	GND	
VSS	D3	GND	
VSS	D30	GND	
VSS	D33	GND	
VSS	D6	GND	
VSS	D9	GND	
VSS	E11	GND	
VSS	E13	GND	
VSS	E18	GND	
VSS	E2	GND	
VSS	E21	GND	
VSS	E24	GND	
VSS	E29	GND	
VSS	E32	GND	
VSS	E35	GND	
VSS	E5	GND	
VSS	E8	GND	
VSS	F16	GND	
VSS	F19	GND	
VSS	F22	GND	
VSS	F25	GND	
VSS	F27	GND	
VSS	F30	GND	
VSS	G20	GND	
VSS	G3	GND	
VSS	G31	GND	
VSS	G34	GND	

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	G6	GND	
VSS	G9	GND	
VSS	H11	GND	
VSS	H13	GND	
VSS	H15	GND	
VSS	H18	GND	
VSS	H2	GND	
VSS	H22	GND	
VSS	H24	GND	
VSS	H26	GND	
VSS	H28	GND	
VSS	H32	GND	
VSS	H35	GND	
VSS	H5	GND	
VSS	H8	GND	
VSS	J19	GND	
VSS	J21	GND	
VSS	J30	GND	
VSS	J32	GND	
VSS	K27	GND	
VSS	K3	GND	
VSS	K30	GND	
VSS	K33	GND	
VSS	K34	GND	
VSS	K6	GND	
VSS	K9	GND	
VSS	L2	GND	
VSS	L29	GND	
VSS	L32	GND	
VSS	L35	GND	
VSS	L5	GND	
VSS	L8	GND	
VSS	M10	GND	
VSS	N26	GND	
VSS	N27	GND	
VSS	N28	GND	
VSS	N29	GND	
VSS	N30	GND	
VSS	N31	GND	
VSS	N32	GND	

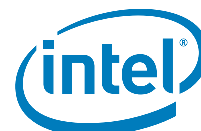


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	N33	GND	
VSS	N34	GND	
VSS	N35	GND	
VSS	N6	GND	
VSS	P2	GND	
VSS	P4	GND	
VSS	P8	GND	
VSS	R10	GND	
VSS	T26	GND	
VSS	T27	GND	
VSS	T28	GND	
VSS	T29	GND	
VSS	T30	GND	
VSS	T31	GND	
VSS	T32	GND	
VSS	T33	GND	
VSS	T34	GND	
VSS	T35	GND	
VSS	T6	GND	
VSS	U2	GND	
VSS	U4	GND	
VSS	U8	GND	
VSS	V10	GND	
VSS	W26	GND	
VSS	W27	GND	
VSS	W28	GND	
VSS	W29	GND	
VSS	W30	GND	
VSS	W31	GND	
VSS	W32	GND	
VSS	W33	GND	
VSS	W34	GND	
VSS	W35	GND	
VSS	W6	GND	
VSS	Y2	GND	
VSS	Y4	GND	
VSS	Y8	GND	
VSS_NCTF	A35		
VSS_NCTF	AR34		
VSS_NCTF	AT1		

Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS_NCTF	AT35		
VSS_NCTF	B1		
VSS_NCTF	B2		
VSS_NCTF	B34		
VSS_SENSE	AJ35	Analog	O
VSS_SENSE_VTT	A15	Analog	O
VSSAXG_SENSE	AT22	Analog	O
VTT_SELECT	G15	CMOS	O
VTT_SENSE	B15	Analog	O
VTT0	A11	REF	
VTT0	A12	REF	
VTT0	A13	REF	
VTT0	A14	REF	
VTT0	AB10	REF	
VTT0	AC10	REF	
VTT0	AE10	REF	
VTT0	AF10	REF	
VTT0	AH10	REF	
VTT0	AH11	REF	
VTT0	AH12	REF	
VTT0	AH14	REF	
VTT0	B12	REF	
VTT0	B14	REF	
VTT0	C11	REF	
VTT0	C12	REF	
VTT0	C13	REF	
VTT0	C14	REF	
VTT0	D11	REF	
VTT0	D12	REF	
VTT0	D13	REF	
VTT0	D14	REF	
VTT0	E12	REF	
VTT0	E14	REF	
VTT0	F11	REF	
VTT0	F12	REF	
VTT0	F13	REF	
VTT0	F14	REF	
VTT0	G11	REF	
VTT0	G12	REF	

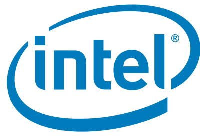


Table 45. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VTT0	G13	REF	
VTT0	G14	REF	
VTT0	H12	REF	
VTT0	H14	REF	
VTT0	J11	REF	
VTT0	J12	REF	
VTT0	J13	REF	
VTT0	J14	REF	
VTT0	J15	REF	
VTT0	J16	REF	
VTT0	K10	REF	
VTT0	L10	REF	
VTT0	N10	REF	
VTT0	P10	REF	
VTT0	T10	REF	
VTT0	U10	REF	
VTT0	W10	REF	
VTT0	Y10	REF	
VTT1	E25	REF	
VTT1	E26	REF	
VTT1	F26	REF	
VTT1	G26	REF	
VTT1	G27	REF	
VTT1	G28	REF	
VTT1	H19	REF	
VTT1	H20	REF	
VTT1	H21	REF	
VTT1	H25	REF	
VTT1	H27	REF	
VTT1	J18	REF	
VTT1	J20	REF	
VTT1	J22	REF	
VTT1	J23	REF	
VTT1	J24	REF	
VTT1	J25	REF	
VTT1	J26	REF	
VTT1	J27	REF	
VTT1	K26	REF	
VTTPWRGOOD	AM15	Async CMOS	I

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
A2	KEY		
A3	RSVD_NCTF		
A4	SB_DQ[6]	DDR3	I/O
A5	SB_DQ[1]	DDR3	I/O
A6	SB_DQ[5]	DDR3	I/O
A7	SA_DQ[3]	DDR3	I/O
A8	SA_DQ[7]	DDR3	I/O
A9	VSS	GND	
A10	SA_DQ[0]	DDR3	I/O
A11	VTT0	REF	
A12	VTT0	REF	
A13	VTT0	REF	
A14	VTT0	REF	
A15	VSS_SENSE_VTT	Analog	O
A16	BCLK	DIFF CLK	I
A17	DPLL_REF_SSCLK#	DIFF CLK	I
A18	DPLL_REF_SSCLK	DIFF CLK	I
A19	RSVD		
A20	RSVD		
A21	DMI_RX#[3]	DMI	I
A22	DMI_RX[3]	DMI	I
A23	VSS	GND	
A24	DMI_RX#[0]	DMI	I
A25	PEG_RBIAS	Analog	I
A26	PEG_ICOMPO	Analog	I
A27	VSS	GND	
A28	PEG_RX[13]	PCIe	I
A29	VSS	GND	
A30	PEG_RX[15]	PCIe	I
A31	PEG_RX#[15]	PCIe	I
A32	PEG_RX[11]	PCIe	I
A33	RSVD_NCTF		
A34	RSVD_NCTF		
A35	VSS_NCTF		
AA1	RSVD_TP		

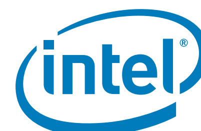


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AA2	RSVD_TP		
AA3	SA_MA[3]	DDR3	O
AA4	RSVD_TP		
AA5	RSVD_TP		
AA6	SA_CK[0]	DDR3	O
AA7	SA_CK#[0]	DDR3	O
AA8	SA_MA[2]	DDR3	O
AA9	SA_MA[5]	DDR3	O
AA10	VSS	GND	
AA26	VCC	REF	
AA27	VCC	REF	
AA28	VCC	REF	
AA29	VCC	REF	
AA30	VCC	REF	
AA31	VCC	REF	
AA32	VCC	REF	
AA33	VCC	REF	
AA34	VCC	REF	
AA35	VCC	REF	
AB1	SB_BS[0]	DDR3	O
AB2	SA_BS[1]	DDR3	O
AB3	SA_RAS#	DDR3	O
AB4	VDDQ	REF	
AB5	SB_MA[10]	DDR3	O
AB6	VSS	GND	
AB7	VDDQ	REF	
AB8	SB_CS#[0]	DDR3	O
AB9	RSVD		
AB10	VTT0	REF	
AB26	VSS	GND	
AB27	VSS	GND	
AB28	VSS	GND	
AB29	VSS	GND	
AB30	VSS	GND	
AB31	VSS	GND	
AB32	VSS	GND	
AB33	VSS	GND	
AB34	VSS	GND	
AB35	VSS	GND	
AC1	VDDQ	REF	

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AC2	VSS	GND	
AC3	SA_BS[0]	DDR3	O
AC4	VSS	GND	
AC5	SB_CAS#	DDR3	O
AC6	SB_WE#	DDR3	O
AC7	SB_ODT[0]	DDR3	O
AC8	VSS	GND	
AC9	RSVD		
AC10	VTT0	REF	
AC26	VCC	REF	
AC27	VCC	REF	
AC28	VCC	REF	
AC29	VCC	REF	
AC30	VCC	REF	
AC31	VCC	REF	
AC32	VCC	REF	
AC33	VCC	REF	
AC34	VCC	REF	
AC35	VCC	REF	
AD1	SB_ODT[1]	DDR3	O
AD2	RSVD_TP		
AD3	RSVD_TP		
AD4	SA_MA[10]	DDR3	O
AD5	RSVD_TP		
AD6	SB_CS#[1]	DDR3	O
AD7	RSVD_TP		
AD8	SA_ODT[0]	DDR3	O
AD9	RSVD_TP		
AD10	VSS	GND	
AD26	VCC	REF	
AD27	VCC	REF	
AD28	VCC	REF	
AD29	VCC	REF	
AD30	VCC	REF	
AD31	VCC	REF	
AD32	VCC	REF	
AD33	VCC	REF	
AD34	VCC	REF	
AD35	VCC	REF	
AE1	SA_CAS#	DDR3	O

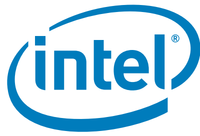


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AE2	SA_CS#[0]	DDR3	O
AE3	RSVD_TP		
AE4	VDDQ	REF	
AE5	RSVD_TP		
AE6	VSS	GND	
AE7	VDDQ	REF	
AE8	SA_CS#[1]	DDR3	O
AE9	SA_WE#	DDR3	O
AE10	VTT0	REF	
AE26	VSS	GND	
AE27	VSS	GND	
AE28	VSS	GND	
AE29	VSS	GND	
AE30	VSS	GND	
AE31	VSS	GND	
AE32	VSS	GND	
AE33	VSS	GND	
AE34	VSS	GND	
AE35	VSS	GND	
AF1	VDDQ	REF	
AF2	VSS	GND	
AF3	SB_DQ[32]	DDR3	I/O
AF4	VSS	GND	
AF5	SA_DQ[33]	DDR3	I/O
AF6	SA_DQ[36]	DDR3	I/O
AF7	SB_MA[13]	DDR3	O
AF8	VSS	GND	
AF9	SA_ODT[1]	DDR3	O
AF10	VTT0	REF	
AF26	VCC	REF	
AF27	VCC	REF	
AF28	VCC	REF	
AF29	VCC	REF	
AF30	VCC	REF	
AF31	VCC	REF	
AF32	VCC	REF	
AF33	VCC	REF	
AF34	VCC	REF	
AF35	VCC	REF	
AG1	SB_DQ[33]	DDR3	I/O

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AG2	SB_DQS[4]	DDR3	I/O
AG3	SB_DQ[37]	DDR3	I/O
AG4	SB_DQ[36]	DDR3	I/O
AG5	SA_DQ[37]	DDR3	I/O
AG6	SA_DM[4]	DDR3	O
AG7	RSVD_TP		
AG8	SA_MA[13]	DDR3	O
AG9	RSVD		
AG10	VSS	GND	
AG26	VCC	REF	
AG27	VCC	REF	
AG28	VCC	REF	
AG29	VCC	REF	
AG30	VCC	REF	
AG31	VCC	REF	
AG32	VCC	REF	
AG33	VCC	REF	
AG34	VCC	REF	
AG35	VCC	REF	
AH1	SB_DM[4]	DDR3	O
AH2	SB_DQS#[4]	DDR3	I/O
AH3	VSS	GND	
AH4	SB_DQ[39]	DDR3	I/O
AH5	SA_DQ[32]	DDR3	I/O
AH6	VSS	GND	
AH7	SA_DQS#[4]	DDR3	I/O
AH8	SA_DQS[4]	DDR3	I/O
AH9	VSS	GND	
AH10	VTT0	REF	
AH11	VTT0	REF	
AH12	VTT0	REF	
AH13	VSS	GND	
AH14	VTT0	REF	
AH15	RSVD		
AH16	VAXG	REF	
AH17	VSS	GND	
AH18	VAXG	REF	
AH19	VAXG	REF	
AH20	VSS	GND	
AH21	VAXG	REF	

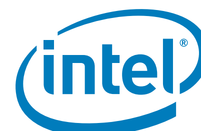


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AH22	BPM#[5]	GTL	I/O
AH23	BPM#[7]	GTL	I/O
AH24	SKTOCC#		
AH25	RSVD		
AH26	VSS	GND	
AH27	VSS	GND	
AH28	VSS	GND	
AH29	VSS	GND	
AH30	VSS	GND	
AH31	VSS	GND	
AH32	VSS	GND	
AH33	VSS	GND	
AH34	VSS	GND	
AH35	VSS	GND	
AJ1	VDDQ	REF	
AJ2	VSS	GND	
AJ3	SB_DQ[34]	DDR3	I/O
AJ4	SB_DQ[38]	DDR3	I/O
AJ5	VSS	GND	
AJ6	SA_DQ[39]	DDR3	I/O
AJ7	SA_DQ[38]	DDR3	I/O
AJ8	VSS	GND	
AJ9	SA_DQ[41]	DDR3	I/O
AJ10	SA_DQ[40]	DDR3	I/O
AJ11	VSS	GND	
AJ12	RSVD_TP		
AJ13	RSVD_TP		
AJ14	VSS	GND	
AJ15	RSVD		
AJ16	VAXG	REF	
AJ17	VSS	GND	
AJ18	VAXG	REF	
AJ19	VAXG	REF	
AJ20	VSS	GND	
AJ21	VAXG	REF	
AJ22	BPM#[0]	GTL	I/O
AJ23	VSS	GND	
AJ24	BPM#[3]	GTL	I/O
AJ25	BPM#[4]	GTL	I/O
AJ26	RSVD		

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AJ27	RSVD		
AJ28	CFG[11]	CMOS	I
AJ29	CFG[15]	CMOS	I
AJ30	CFG[16]	CMOS	I
AJ31	VSS	GND	
AJ32	CFG[14]	CMOS	I
AJ33	RSVD		
AJ34	VCC_SENSE	Analog	O
AJ35	VSS_SENSE	Analog	O
AK1	SB_DQ[35]	DDR3	I/O
AK2	SB_DQ[45]	DDR3	I/O
AK3	SB_DQ[40]	DDR3	I/O
AK4	SB_DQ[41]	DDR3	I/O
AK5	SB_DQ[44]	DDR3	I/O
AK6	SA_DQ[34]	DDR3	I/O
AK7	SA_DQ[35]	DDR3	I/O
AK8	SA_DQ[44]	DDR3	I/O
AK9	SA_DQS#[5]	DDR3	I/O
AK10	SA_DQS[5]	DDR3	I/O
AK11	SA_DQ[46]	DDR3	I/O
AK12	SA_DQ[43]	DDR3	I/O
AK13	SM_DRAMPWRO K	DDR3	O
AK14	CATERR#	GTL	I/O
AK15	THERMTRIP#	Async GTL	O
AK16	VAXG	REF	
AK17	VSS	GND	
AK18	VAXG	REF	
AK19	VAXG	REF	
AK20	VSS	GND	
AK21	VAXG	REF	
AK22	BPM#[1]	GTL	I/O
AK23	BPM#[6]	GTL	I/O
AK24	BPM#[2]	GTL	I/O
AK25	VSS	GND	
AK26	RSVD_TP		
AK27	VSS	GND	
AK28	CFG[10]	CMOS	I
AK29	VSS	GND	
AK30	CFG[17]	CMOS	I
AK31	CFG[9]	CMOS	I

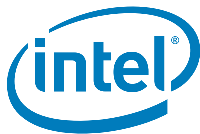


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AK32	CFG[8]	CMOS	I
AK33	VID[1]/MSID[1]	CMOS	I/O
AK34	VID[2]/MSID[2]	CMOS	I/O
AK35	VID[0]/MSID[0]	CMOS	I/O
AL1	SM_RCOMP[0]	Analog	I
AL2	SB_DM[5]	DDR3	O
AL3	VSS	GND	
AL4	SB_DQS#[5]	DDR3	I/O
AL5	SB_DQS[5]	DDR3	I/O
AL6	VSS	GND	
AL7	SA_DQ[45]	DDR3	I/O
AL8	SA_DQ[47]	DDR3	I/O
AL9	VSS	GND	
AL10	SA_DQ[42]	DDR3	I/O
AL11	SA_DQ[51]	DDR3	I/O
AL12	VSS	GND	
AL13	SA_DQ[61]	DDR3	I/O
AL14	RSTIN#	CMOS	I
AL15	PM_SYNC	CMOS	I
AL16	VAXG	REF	
AL17	VSS	GND	
AL18	VAXG	REF	
AL19	VAXG	REF	
AL20	VSS	GND	
AL21	VAXG	REF	
AL22	RSVD		
AL23	VSS	GND	
AL24	RSVD		
AL25	RSVD		
AL26	RSVD_TP		
AL27	RSVD		
AL28	RSVD		
AL29	RSVD		
AL30	CFG[4]	CMOS	I
AL31	VSS	GND	
AL32	CFG[3]	CMOS	I
AL33	VID[4]/CSC[1]	CMOS	I/O
AL34	VSS	GND	
AL35	VID[3]/CSC[0]	CMOS	I/O
AM1	SM_RCOMP[1]	Analog	I

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AM2	VSS	GND	
AM3	SB_DQ[47]	DDR3	I/O
AM4	SB_DQ[46]	DDR3	I/O
AM5	VSS	GND	
AM6	SB_DQ[42]	DDR3	I/O
AM7	SA_DM[5]	DDR3	O
AM8	VSS	GND	
AM9	SA_DQ[52]	DDR3	I/O
AM10	SA_DQ[49]	DDR3	I/O
AM11	VSS	GND	
AM12	SA_DQ[56]	DDR3	I/O
AM13	SA_DQ[58]	DDR3	I/O
AM14	VSS	GND	
AM15	VTTPWRGOOD	Async CMOS	I
AM16	VAXG	REF	
AM17	VSS	GND	
AM18	VAXG	REF	
AM19	VAXG	REF	
AM20	VSS	GND	
AM21	VAXG	REF	
AM22	GFX_VID[0]	CMOS	O
AM23	GFX_VID[4]	CMOS	O
AM24	GFX_IMON	Analog	I
AM25	VSS	GND	
AM26	TAPPWRGOOD	Async CMOS	O
AM27	VSS	GND	
AM28	CFG[1]	CMOS	I
AM29	VSS	GND	
AM30	CFG[0]	CMOS	I
AM31	CFG[5]	CMOS	I
AM32	CFG[7]	CMOS	I
AM33	VID[5]/CSC[2]	CMOS	I/O
AM34	PROC_DPRSLPVR	CMOS	O
AM35	VID[6]	CMOS	O
AN1	SM_RCOMP[2]	Analog	I
AN2	SB_DQ[43]	DDR3	I/O
AN3	SB_DQ[53]	DDR3	I/O
AN4	SB_DQ[52]	DDR3	I/O
AN5	SB_DQ[49]	DDR3	I/O

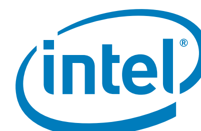


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AN6	SB_DQ[51]	DDR3	I/O
AN7	SB_DQ[56]	DDR3	I/O
AN8	SA_DQ[48]	DDR3	I/O
AN9	SA_DQ[53]	DDR3	I/O
AN10	SA_DM[6]	DDR3	O
AN11	SA_DQS[6]	DDR3	I/O
AN12	SA_DQ[57]	DDR3	I/O
AN13	SA_DM[7]	DDR3	O
AN14	VCCPWRGOOD_1	Async CMOS	I
AN15	PM_EXT_TS#[0]	CMOS	I
AN16	VAXG	REF	
AN17	VSS	GND	
AN18	VAXG	REF	
AN19	VAXG	REF	
AN20	VSS	GND	
AN21	VAXG	REF	
AN22	GFX_VID[2]	CMOS	O
AN23	VSS	GND	
AN24	GFX_VID[6]	CMOS	O
AN25	DBR#		O
AN26	PROCHOT#	Async GTL	I/O
AN27	VCCPWRGOOD_0	Async CMOS	I
AN28	TCK	CMOS	I
AN29	CFG[6]	CMOS	I
AN30	CFG[12]	CMOS	I
AN31	VSS	GND	
AN32	CFG[13]	CMOS	I
AN33	PSI#	Async CMOS	O
AN34	VSS	GND	
AN35	ISENSE	Analog	I
AP1	RSVD_NCTF		
AP2	VSS	GND	
AP3	SB_DQ[48]	DDR3	I/O
AP4	VSS	GND	
AP4	VSS	GND	
AP5	SB_DQS[6]	DDR3	I/O
AP6	SB_DQ[57]	DDR3	I/O
AP7	VSS	GND	
AP8	SB_DQ[58]	DDR3	I/O

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AP9	SB_DQ[61]	DDR3	I/O
AP10	VSS	GND	
AP11	SA_DQS#[6]	DDR3	I/O
AP12	SA_DQ[55]	DDR3	I/O
AP13	VSS	GND	
AP14	SA_DQ[63]	DDR3	I/O
AP15	PM_EXT_TS#[1]	CMOS	I
AP16	VAXG	REF	
AP17	VSS	GND	
AP18	VAXG	REF	
AP19	VAXG	REF	
AP20	VSS	GND	
AP21	VAXG	REF	
AP22	GFX_VID[1]	CMOS	O
AP23	GFX_VID[3]	CMOS	O
AP24	GFX_VID[5]	CMOS	O
AP25	RSVD		
AP26	RESET_OBS#	Async CMOS	O
AP27	PREQ#	Async GTL	I
AP28	TMS	CMOS	I
AP29	TDO_M	CMOS	O
AP30	RSVD		
AP31	CFG[2]	CMOS	I
AP32	RSVD		
AP33	RSVD		
AP34	VSS	GND	
AP35	RSVD_NCTF		
AR1	RSVD_NCTF		
AR2	RSVD_NCTF		
AR3	VSS	GND	
AR4	SB_DM[6]	DDR3	O
AR5	SB_DQS#[6]	DDR3	I/O
AR6	VSS	GND	
AR7	SB_DQS[7]	DDR3	I/O
AR8	SB_DQS#[7]	DDR3	I/O
AR9	VSS	GND	
AR10	SB_DQ[62]	DDR3	I/O
AR11	SA_DQ[50]	DDR3	I/O
AR12	VSS	GND	
AR13	SA_DQS[7]	DDR3	I/O

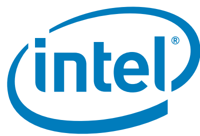


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AR14	SA_DQ[62]	DDR3	I/O
AR15	VSS	GND	
AR16	VAXG	REF	
AR17	VSS	GND	
AR18	VAXG	REF	
AR19	VAXG	REF	
AR20	VSS	GND	
AR21	VAXG	REF	
AR22	VAXG_SENSE	Analog	O
AR23	VSS	GND	
AR24	VSS	GND	
AR25	GFX_VR_EN	CMOS	O
AR26	VSS	GND	
AR27	TDO	CMOS	O
AR28	VSS	GND	
AR29	TDI_M	CMOS	I
AR30	BCLK_ITP	DIFF CLK	O
AR31	VSS	GND	
AR32	RSVD		
AR33	RSVD		
AR34	VSS_NCTF		
AR35	RSVD_NCTF		
AT1	VSS_NCTF		
AT2	RSVD_TP		
AT3	RSVD_NCTF		
AT4	SB_DQ[50]	DDR3	I/O
AT5	SB_DQ[54]	DDR3	I/O
AT6	SB_DQ[55]	DDR3	I/O
AT7	SB_DQ[60]	DDR3	I/O
AT8	SB_DM[7]	DDR3	O
AT9	SB_DQ[59]	DDR3	I/O
AT10	SB_DQ[63]	DDR3	I/O
AT11	SA_DQ[54]	DDR3	I/O
AT12	SA_DQ[60]	DDR3	I/O
AT13	SA_DQS#[7]	DDR3	I/O
AT14	SA_DQ[59]	DDR3	I/O
AT15	PECI	Async	I/O
AT16	VAXG	REF	
AT17	VSS	GND	
AT18	VAXG	REF	

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AT19	VAXG	REF	
AT20	VSS	GND	
AT21	VAXG	REF	
AT22	VSSAXG_SENSE	Analog	O
AT23	COMP3	Analog	I
AT24	COMP2	Analog	I
AT25	GFX_DPRSLPVR	CMOS	O
AT26	COMP0	Analog	I
AT27	TRST#	CMOS	I
AT28	PRDY#	Async GTL	O
AT29	TDI	CMOS	I
AT30	BCLK_ITP#	DIFF CLK	O
AT31	RSVD		
AT32	RSVD		
AT33	RSVD_NCTF		
AT34	RSVD_NCTF		
AT35	VSS_NCTF		
B1	VSS_NCTF		
B2	VSS_NCTF		
B3	SB_DQ[3]	DDR3	I/O
B4	VSS	GND	
B5	SB_DQ[0]	DDR3	I/O
B6	VSS	GND	
B7	SA_DQ[13]	DDR3	I/O
B8	VSS	GND	
B9	SA_DM[0]	DDR3	O
B10	SA_DQ[4]	DDR3	I/O
B11	VSS	GND	
B12	VTT0	REF	
B13	VSS	GND	
B14	VTT0	REF	
B15	VTT_SENSE	Analog	O
B16	BCLK#	DIFF CLK	I
B17	VSS	GND	
B18	VSS	GND	
B19	RSVD		
B20	RSVD		
B21	VSS	GND	
B22	DMI_RX#[2]	DMI	I
B23	DMI_RX[2]	DMI	I

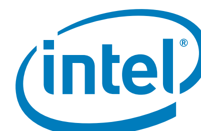


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
B24	DMI_RX[0]	DMI	I
B25	VSS	GND	
B26	PEG_ICOMPI	Analog	I
B27	PEG_RCOMPO	Analog	I
B28	PEG_RX#[13]	PCIe	I
B29	PEG_RX[14]	PCIe	I
B30	PEG_RX#[14]	PCIe	I
B31	VSS	GND	
B32	PEG_RX#[11]	PCIe	I
B33	PEG_RX[9]	PCIe	I
B34	VSS_NCTF		
B35	RSVD_NCTF		
C1	RSVD_NCTF		
C2	SB_DQ[12]	DDR3	I/O
C3	SB_DQ[2]	DDR3	I/O
C4	SB_DQ[7]	DDR3	I/O
C5	SB_DQS[0]	DDR3	I/O
C6	SA_DQ[15]	DDR3	I/O
C7	SA_DQ[2]	DDR3	I/O
C8	SA_DQS[0]	DDR3	I/O
C9	SA_DQS#[0]	DDR3	I/O
C10	SA_DQ[1]	DDR3	I/O
C11	VTT0	REF	
C12	VTT0	REF	
C13	VTT0	REF	
C14	VTT0	REF	
C15	RSVD		
C16	VSS	GND	
C17	FDI_INT	CMOS	I
C18	FDI_TX[3]	FDI	O
C19	VSS	GND	
C20	VSS	GND	
C21	FDI_TX[1]	FDI	O
C22	VSS	GND	
C23	DMI_RX#[1]	DMI	I
C24	VSS	GND	
C25	PEG_TX[15]	PCIe	O
C26	PEG_TX#[15]	PCIe	O
C27	PEG_TX[14]	PCIe	O
C28	VSS	GND	

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
C29	VSS	GND	
C30	PEG_RX[12]	PCIe	I
C31	PEG_RX#[12]	PCIe	I
C32	VSS	GND	
C33	PEG_RX#[9]	PCIe	I
C34	VSS	GND	
C35	RSVD_NCTF		
D1	SB_DQ[8]	DDR3	I/O
D2	SB_DQ[9]	DDR3	I/O
D3	VSS	GND	
D4	SB_DM[0]	DDR3	O
D5	SB_DQS#[0]	DDR3	I/O
D6	VSS	GND	
D7	SA_DM[1]	DDR3	O
D8	SA_DQ[8]	DDR3	I/O
D9	VSS	GND	
D10	SA_DQ[5]	DDR3	I/O
D11	VTT0	REF	
D12	VTT0	REF	
D13	VTT0	REF	
D14	VTT0	REF	
D15	RSVD		
D16	PEG_CLK#	DIFF CLK	I
D17	FDI_LSYNC[1]	CMOS	I
D18	FDI_TX#[3]	FDI	O
D19	FDI_TX#[2]	FDI	O
D20	FDI_TX[2]	FDI	O
D21	FDI_TX#[1]	FDI	O
D22	FDI_TX[0]	FDI	O
D23	DMI_RX[1]	DMI	I
D24	DMI_TX#[0]	DMI	O
D25	DMI_TX[0]	DMI	O
D26	VSS	GND	
D27	PEG_TX#[14]	PCIe	O
D28	PEG_TX[13]	PCIe	O
D29	PEG_TX#[13]	PCIe	O
D30	VSS	GND	
D31	PEG_RX[10]	PCIe	I
D32	PEG_RX#[10]	PCIe	I
D33	VSS	GND	

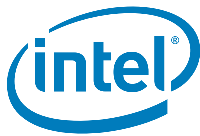


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
D34	PEG_RX[7]	PCIe	I
D35	PEG_RX#[7]	PCIe	I
E1	SB_DM[1]	DDR3	O
E2	VSS	GND	
E3	SB_DQS[1]	DDR3	I/O
E4	SB_DQ[4]	DDR3	I/O
E5	VSS	GND	
E6	SA_DQ[10]	DDR3	I/O
E7	SA_DQ[14]	DDR3	I/O
E8	VSS	GND	
E9	SA_DQ[12]	DDR3	I/O
E10	SA_DQ[6]	DDR3	I/O
E11	VSS	GND	
E12	VTT0	REF	
E13	VSS	GND	
E14	VTT0	REF	
E15	RSVD_TP		
E16	PEG_CLK	DIFF CLK	I
E17	FDI_FSYNC[1]	CMOS	I
E18	VSS	GND	
E19	FDI_TX#[5]	FDI	O
E20	FDI_TX[5]	FDI	O
E21	VSS	GND	
E22	FDI_TX#[0]	FDI	O
E23	DMI_TX[2]	DMI	O
E24	VSS	GND	
E25	VTT1	REF	
E26	VTT1	REF	
E27	PEG_TX[12]	PCIe	O
E28	PEG_TX#[12]	PCIe	O
E29	VSS	GND	
E30	RSVD		
E31	RSVD		
E32	VSS	GND	
E33	PEG_RX#[8]	PCIe	I
E34	PEG_RX[5]	PCIe	I
E35	VSS	GND	
F1	SB_DQ[11]	DDR3	I/O
F2	SB_DQ[10]	DDR3	I/O
F3	SB_DQ[14]	DDR3	I/O

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
F4	SB_DQS#[1]	DDR3	I/O
F5	SB_DQ[13]	DDR3	I/O
F6	SM_DRAMRST#	DDR3	O
F7	SA_DQ[11]	DDR3	I/O
F8	SA_DQS#[1]	DDR3	I/O
F9	SA_DQS[1]	DDR3	I/O
F10	SA_DQ[9]	DDR3	I/O
F11	VTT0	REF	
F12	VTT0	REF	
F13	VTT0	REF	
F14	VTT0	REF	
F15	RSVD_TP		
F16	VSS	GND	
F17	FDI_FSYNC[0]	CMOS	I
F18	FDI_LSYNC[0]	CMOS	I
F19	VSS	GND	
F20	FDI_TX[6]	FDI	O
F21	FDI_TX#[6]	FDI	O
F22	VSS	GND	
F23	DMI_TX#[2]	DMI	O
F24	DMI_TX[1]	DMI	O
F25	VSS	GND	
F26	VTT1	REF	
F27	VSS	GND	
F28	PEG_TX[11]	PCIe	O
F29	PEG_TX#[11]	PCIe	O
F30	VSS	GND	
F31	PEG_RX#[6]	PCIe	I
F32	PEG_RX[6]	PCIe	I
F33	PEG_RX[8]	PCIe	I
F34	PEG_RX#[5]	PCIe	I
F35	PEG_RX[3]	PCIe	I
G1	SB_DQ[20]	DDR3	I/O
G2	SB_DQ[17]	DDR3	I/O
G3	VSS	GND	
G4	SB_DQ[15]	DDR3	I/O
G5	SB_DQ[21]	DDR3	I/O
G6	VSS	GND	
G7	SA_DQ[20]	DDR3	I/O
G8	SA_DQ[17]	DDR3	I/O

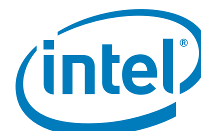


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
G9	VSS	GND	
G10	SA_DQ[21]	DDR3	I/O
G11	VTT0	REF	
G12	VTT0	REF	
G13	VTT0	REF	
G14	VTT0	REF	
G15	VTT_SELECT	CMOS	O
G16	COMP1	Analog	I
G17	RSVD		
G18	FDI_TX#[7]	FDI	O
G19	FDI_TX[7]	FDI	O
G20	VSS	GND	
G21	FDI_TX#[4]	FDI	O
G22	FDI_TX[4]	FDI	O
G23	DMI_TX[3]	DMI	O
G24	DMI_TX#[1]	DMI	O
G25	RSVD		
G26	VTT1	REF	
G27	VTT1	REF	
G28	VTT1	REF	
G29	PEG_TX[10]	PCIe	O
G30	PEG_TX[9]	PCIe	O
G31	VSS	GND	
G32	PEG_RX#[4]	PCIe	I
G33	PEG_RX[4]	PCIe	I
G34	VSS	GND	
G35	PEG_RX#[3]	PCIe	I
H1	VDDQ	REF	
H2	VSS	GND	
H3	SB_DM[2]	DDR3	O
H4	SB_DQS[2]	DDR3	I/O
H5	VSS	GND	
H6	SB_DQ[16]	DDR3	I/O
H7	SA_DM[2]	DDR3	O
H8	VSS	GND	
H9	SA_DQS[2]	DDR3	I/O
H10	SA_DQ[16]	DDR3	I/O
H11	VSS	GND	
H12	VTT0	REF	
H13	VSS	GND	

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
H14	VTT0	REF	
H15	VSS	GND	
H16	RSVD_TP		
H17	SB_DIMM_ VREFDQ	A	O
H18	VSS	GND	
H19	VTT1	REF	
H20	VTT1	REF	
H21	VTT1	REF	
H22	VSS	GND	
H23	DMI_TX#[3]	DMI	O
H24	VSS	GND	
H25	VTT1	REF	
H26	VSS	GND	
H27	VTT1	REF	
H28	VSS	GND	
H29	PEG_TX#[10]	PCIe	O
H30	PEG_TX#[9]	PCIe	O
H31	PEG_TX[7]	PCIe	O
H32	VSS	GND	
H33	PEG_RX[2]	PCIe	I
H34	PEG_RX[1]	PCIe	I
H35	VSS	GND	
J1	SB_DQ[23]	DDR3	I/O
J2	SB_DQ[22]	DDR3	I/O
J3	SB_DQ[19]	DDR3	I/O
J4	SB_DQS#[2]	DDR3	I/O
J5	SB_DQ[24]	DDR3	I/O
J6	SB_DQ[18]	DDR3	I/O
J7	SA_DQ[22]	DDR3	I/O
J8	SA_DQ[19]	DDR3	I/O
J9	SA_DQS#[2]	DDR3	I/O
J10	SA_DQ[23]	DDR3	I/O
J11	VTT0	REF	
J12	VTT0	REF	
J13	VTT0	REF	
J14	VTT0	REF	
J15	VTT0	REF	
J16	VTT0	REF	
J17	SA_DIMM_ VREFDQ	A	O

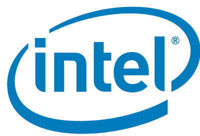


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
J18	VTT1	REF	
J19	VSS	GND	
J20	VTT1	REF	
J21	VSS	GND	
J22	VTT1	REF	
J23	VTT1	REF	
J24	VTT1	REF	
J25	VTT1	REF	
J26	VTT1	REF	
J27	VTT1	REF	
J28	RSVD		
J29	RSVD		
J30	VSS	GND	
J31	PEG_TX#[7]	PCIe	O
J32	VSS	GND	
J33	PEG_RX#[2]	PCIe	I
J34	PEG_RX#[1]	PCIe	I
J35	PEG_RX[0]	PCIe	I
K1	SB_DM[3]	DDR3	O
K2	SB_DQ[25]	DDR3	I/O
K3	VSS	GND	
K4	SB_DQ[29]	DDR3	I/O
K5	SB_DQ[28]	DDR3	I/O
K6	VSS	GND	
K7	SA_DQ[18]	DDR3	I/O
K8	SA_DQ[29]	DDR3	I/O
K9	VSS	GND	
K10	VTT0	REF	
K26	VTT1	REF	
K27	VSS	GND	
K28	PEG_TX[8]	PCIe	O
K29	PEG_TX#[8]	PCIe	O
K30	VSS	GND	
K31	PEG_TX[5]	PCIe	O
K32	PEG_TX#[5]	PCIe	O
K33	VSS	GND	
K34	VSS	GND	
K35	PEG_RX#[0]	PCIe	I
L1	VDDQ	REF	
L2	VSS	GND	

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
L3	SB_DQ[26]	DDR3	I/O
L4	SB_DQS#[3]	DDR3	I/O
L5	VSS	GND	
L6	SA_DQ[28]	DDR3	I/O
L7	SA_DQ[24]	DDR3	I/O
L8	VSS	GND	
L9	SA_DQ[27]	DDR3	I/O
L10	VTT0	REF	
L26	VCCPLL	REF	
L27	VCCPLL	REF	
L28	RSVD		
L29	VSS	GND	
L30	PEG_TX[3]	PCIe	O
L31	PEG_TX#[4]	PCIe	O
L32	VSS	GND	
L33	PEG_TX#[0]	PCIe	O
L34	PEG_TX[0]	PCIe	O
L35	VSS	GND	
M1	SB_DQ[27]	DDR3	I/O
M2	SB_CKE[1]	DDR3	O
M3	SB_CKE[0]	DDR3	O
M4	SB_DQ[30]	DDR3	I/O
M5	SB_DQS[3]	DDR3	I/O
M6	SA_DQ[25]	DDR3	I/O
M7	SA_DM[3]	DDR3	O
M8	SA_DQ[26]	DDR3	I/O
M9	SA_DQS[3]	DDR3	I/O
M10	VSS	GND	
M26	VCCPLL	REF	
M27	RSVD		
M28	PEG_TX[6]	PCIe	O
M29	PEG_TX#[6]	PCIe	O
M30	PEG_TX#[3]	PCIe	O
M31	PEG_TX[4]	PCIe	O
M32	PEG_TX[2]	PCIe	O
M33	PEG_TX#[2]	PCIe	O
M34	PEG_TX[1]	PCIe	O
M35	PEG_TX#[1]	PCIe	O
N1	SB_MA[15]	DDR3	O
N2	RSVD_TP		

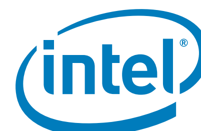


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
N3	RSVD_TP		
N4	VDDQ	REF	
N5	SB_DQ[31]	DDR3	I/O
N6	VSS	GND	
N7	VDDQ	REF	
N8	SA_DQ[30]	DDR3	I/O
N9	SA_DQS#[3]	DDR3	I/O
N10	VTT0	REF	
N26	VSS	GND	
N27	VSS	GND	
N28	VSS	GND	
N29	VSS	GND	
N30	VSS	GND	
N31	VSS	GND	
N32	VSS	GND	
N33	VSS	GND	
N34	VSS	GND	
N35	VSS	GND	
P1	VDDQ	REF	
P2	VSS	GND	
P3	SB_MA[11]	DDR3	O
P4	VSS	GND	
P5	SB_MA[14]	DDR3	O
P6	SA_CKE[1]	DDR3	O
P7	SA_CKE[0]	DDR3	O
P8	VSS	GND	
P9	SA_DQ[31]	DDR3	I/O
P10	VTT0	REF	
P26	VCC	REF	
P27	VCC	REF	
P28	VCC	REF	
P29	VCC	REF	
P30	VCC	REF	
P31	VCC	REF	
P32	VCC	REF	
P33	VCC	REF	
P34	VCC	REF	
P35	VCC	REF	
R1	SB_MA[4]	DDR3	O
R2	SB_MA[6]	DDR3	O

Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
R3	SB_MA[12]	DDR3	O
R4	SB_MA[8]	DDR3	O
R5	SB_MA[9]	DDR3	O
R6	SB_MA[7]	DDR3	O
R7	SB_BS[2]	DDR3	O
R8	RSVD_TP		
R9	RSVD_TP		
R10	VSS	GND	
R26	VCC	REF	
R27	VCC	REF	
R28	VCC	REF	
R29	VCC	REF	
R30	VCC	REF	
R31	VCC	REF	
R32	VCC	REF	
R33	VCC	REF	
R34	VCC	REF	
R35	VCC	REF	
T1	SA_MA[7]	DDR3	O
T2	SA_MA[11]	DDR3	O
T3	SA_MA[14]	DDR3	O
T4	VDDQ	REF	
T5	SB_MA[2]	DDR3	O
T6	VSS	GND	
T7	VDDQ	REF	
T8	SB_MA[5]	DDR3	O
T9	RSVD		
T10	VTT0	REF	
T26	VSS	GND	
T27	VSS	GND	
T28	VSS	GND	
T29	VSS	GND	
T30	VSS	GND	
T31	VSS	GND	
T32	VSS	GND	
T33	VSS	GND	
T34	VSS	GND	
T35	VSS	GND	
U1	VDDQ	REF	
U2	VSS	GND	

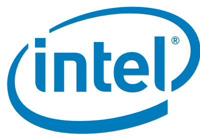
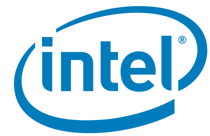


Table 46. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
U3	SA_MA[12]	DDR3	O
U4	VSS	GND	
U5	SB_MA[0]	DDR3	O
U6	SA_MA[9]	DDR3	O
U7	SA_BS[2]	DDR3	O
U8	VSS	GND	
U9	RSVD		
U10	VTT0	REF	
U26	VCC	REF	
U27	VCC	REF	
U28	VCC	REF	
U29	VCC	REF	
U30	VCC	REF	
U31	VCC	REF	
U32	VCC	REF	
U33	VCC	REF	
U34	VCC	REF	
U35	VCC	REF	
V1	SA_MA[4]	DDR3	O
V2	SB_MA[1]	DDR3	O
V3	SB_MA[3]	DDR3	O
V4	RSVD_TP		
V5	RSVD_TP		
V6	SB_CK#[1]	DDR3	O
V7	SB_CK[1]	DDR3	O
V8	SA_MA[6]	DDR3	O
V9	SA_MA[15]	DDR3	O
V10	VSS	GND	
V26	VCC	REF	
V27	VCC	REF	
V28	VCC	REF	
V29	VCC	REF	
V30	VCC	REF	
V31	VCC	REF	
V32	VCC	REF	
V33	VCC	REF	
V34	VCC	REF	
V35	VCC	REF	
W1	SA_MA[1]	DDR3	O
W2	RSVD_TP		

Table 46. rPGA988A Processor Pin List by Pin Number

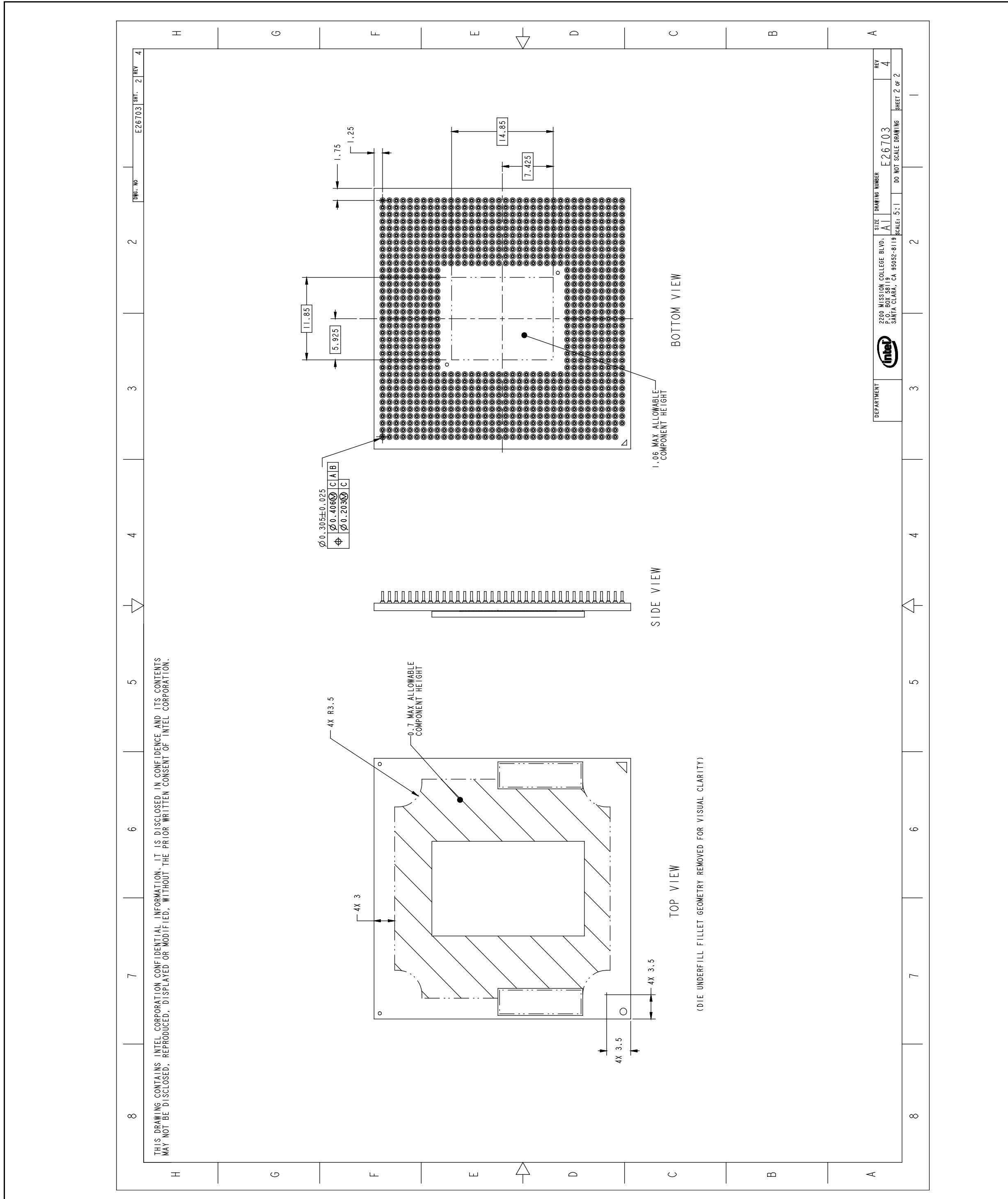
Pin Number	Pin Name	Buffer Type	Dir.
W3	RSVD_TP		
W4	VDDQ	REF	
W5	SB_BS[1]	DDR3	O
W6	VSS	GND	
W7	VDDQ	REF	
W8	SB_CK[0]	DDR3	O
W9	SB_CK#[0]	DDR3	O
W10	VTT0	REF	
W26	VSS	GND	
W27	VSS	GND	
W28	VSS	GND	
W29	VSS	GND	
W30	VSS	GND	
W31	VSS	GND	
W32	VSS	GND	
W33	VSS	GND	
W34	VSS	GND	
W35	VSS	GND	
Y1	VDDQ	REF	
Y2	VSS	GND	
Y3	SA_MA[0]	DDR3	O
Y4	VSS	GND	
Y5	SA_CK#[1]	DDR3	O
Y6	SA_CK[1]	DDR3	O
Y7	SB_RAS#	DDR3	O
Y8	VSS	GND	
Y9	SA_MA[8]	DDR3	O
Y10	VTT0	REF	
Y26	VCC	REF	
Y27	VCC	REF	
Y28	VCC	REF	
Y29	VCC	REF	
Y30	VCC	REF	
Y31	VCC	REF	
Y32	VCC	REF	
Y33	VCC	REF	
Y34	VCC	REF	
Y35	VCC	REF	



8.2 Package Mechanical Information

Figure 18. Intel Core i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series rPGA Mechanical Package (Sheet 1 of 2)

Figure 19. Intel Core i7-900 Mobile Processor Extreme Edition Series, Intel Core i7-800 and i7-700 Mobile Processor Series rPGA Mechanical Package (Sheet 2 of 2)



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