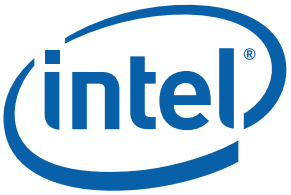

Intel® 5 Series Chipset and Intel® 3400 Series Chipset

Specification Update

February 2011

Notice: Intel® 5 Series Chipset and Intel® 3400 Series Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 322170-017

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Revision History

Revision	Description	Date
-001	• Initial Release	September 2009
-002	• Updated — Identification Information Markings — PCH Device and Revision Identification — 6-Errata: Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation • Added — Errata: 7-Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic, 8-Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum	January 7, 2010
-003	• Added — Errata: 9 - Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® ME, 10 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue, 11 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Transaction Priority Issue, 12 - Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports, 13 - Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports	January 13, 2010
-004	• Added — Errata: 14 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue, 15 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering	February 13, 2010
-005	• Added — Errata: 16 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Device May Slow or Hang, 17- Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Bulk/Control Transactions, 18- Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMIINITs, 19- Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug. — Specification Clarification: 1. GP_RST_SEL[95:0] Description Updated • Updated: — Intel®QS57 Chipset High Definition Audio Device ID Updated	March 10, 2010
-006	Added • Documentation Changes: 1. Correct Figure 8-2 S5 to S0 Timing Diagram • Updated Errata 17 Removed Bulk Transtion	April 14, 2010
-007	Added • Documentation Changes: 2. Update Table 3-1 to include SPI_CS0#. 3. Add Tj Mobile Thermal Junction Operating Temperature limits in Table 8-1. 4. Add sections 5.27.2.9 through 5.27.2.15 to section 5.27 PCH DisPlay Interface. 5. Remove Unit Interval DMI from Table 8-14	May 12, 2010
-008	Edited • Corrected typographical error in Documentation Changes, item #4.	May 17, 2010
-009	• Added — Errata: 20- Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK • Updated: — Errata: 11- Intel® 5 / 3400 Series Chipset Family USB Classic Device Removal Issue • Removed — Specification Clarification: 1; Documentation Changes: 1~5 that went into the updated datasheet 003	June 9, 2010

Revision	Description	Date
-010	• Added — Errata: 21 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection , 22 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit. • Updated: — Specification Clarification: 1- Host WOL Behavior Clarification. — Documentation Changes: 1- Correct Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*.	July 14, 2010
-011	• Updated: — Documentation Changes: 2 - Correct Table 8-8 DC Output Characteristics and Notes 1; 3 - Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers) ; 4 - Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)	August 11, 2010
-012	• Added — Errata: 23 - Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset. • Updated: — Specification Clarification: 2 - Display Port Clarification	September 8, 2010
-013	• Updated: — Errata: 21 - Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset	October 13, 2010
-014	• Added — Errata: 24- Intel® 5 Series Chipset and Intel® 3400 Series Chipset Family High-speed USB Device False Disconnect. — Specification Changes: 1 - SMLink0 Speed Change; 2 - VccVRM Min/Max Change — Specification Clarification: 3 - PIRQ Sharing; 4 - t205 Vcc Reference; 5 - Table 2-27 Power and Ground Signals — Documentation Changes: 5 - Correct 13.1.23 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0); 6 - Correct Table 2-28 Functional Strap Definitions; 7 - Correct Table 9-4 Memory Decode Ranges from Processor Perspective; 8 - Correct 10.1.43 OIC—Other Interrupt Control Register; 9 - Miscellaneous Typographical and Omission Error Corrections; 10 - Update Table 2-8 USB Interface Signals; 11 - Update Note 2 of Table 9-1 PCI Devices and Functions; 12 - Correct 14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2); 13 - Correct 15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5); 14 - Update Table 4-1 PCH System Clock Inputs; 15 - Update Table 2-20 Clock Interface Signals; 16 - Display Interface Updates; 17 - Correct Table 1-4. Intel® 5 Series Chipset Mobile SKUs; 18 - Correct Table 1-3. Intel® 5 Series Chipset Desktop SKUs	November 10, 2010
-015	• Added — Errata: 25- USB Isoch In Transfer Error Issue; 26- USB Full-Speed / Low-Speed Device Removal Issue; 27- USB Babble Detected with SW Overscheduling; 28- USB Low-Speed/Full-Speed EOP Issue; 29- USB PLL Control FSM Not Getting Reset on Global Reset; 30- Asynchronous Retries Prioritized Over Periodic Transfers; 31- Incorrect Data for LS or FS USB Periodic IN Transaction; 32- Intel® 5 Series and 3400 Series Chipset Family Delayed Periodic Traffic Timeout Issue. — Specification Clarification: 6- EHCI Function Numbers; 7- PCI Express* Root Port Function Numbers; 8- t212 Measurement Clarification; 9- Wake Event Causes Update; 10- SGPIO Reference Clock Speed. — Documentation Changes: 19- Controller Link Updates; 20- Miscellaneous Typographical Error Corrections II; 21- Remove note 11 on Table 3-3; 22- Remove VccpNAND on Table 8-3 and Table 8-4; 23- Section 8.2 Updates.	December 8, 2010
-016	• Update — Errata: 14- Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue; 21 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection • Added — Specification Clarification: 11- I^2C Block Read/Write Buffer — Documentation Changes: 24- TEMP_ALERT# Muxing; 25- Causes of Host and Global Resets Update; 26- GPIO18 Toggling Note; 27- Pre-fetch Based Pause Bit Definition; 28- Register Corrections; 29- Display BDF Register Additions; 30- Miscellaneous Typographical Error Corrections III	January 12, 2011
-017	• Update — Errata: 21 - Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA 6Gb/s Device Detection	February 16, 2011

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel ® 5 Series Chipset and Intel ® 3400 Series Chipset Datasheet	322169

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the PCH product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
1	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB Test J/Test K Output Drive Level
2	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB 2.0 Vhsoh
3	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA Signal Voltage Level
4	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection
5	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio Interface Intermittently Does Not Play Sound
6	X		Fixed	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation
7	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic
8	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum.
9	X		Fixed	Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® Management Engine
10	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue
11	X	X	No Fix	Intel® 5 / 3400 Series Chipset Family USB Classic Device Removal Issue
12	X	X	No Fix	Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports
13	X	X	No Fix	Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports
14	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue
15	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering
16	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Devices May Slow or Hang
17	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Control Transactions
18	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs
19	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug
20	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK
21	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA 6Gb/s Device Detection
22	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit
23	X	X	No Fix	Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset
24	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset Family High-speed USB Device False Disconnect
25	X	X	No Fix	USB Isoch In Transfer Error Issue
26	X	X	No Fix	USB Full-Speed / Low-Speed Device Removal Issue
27	X	X	No Fix	USB Babble Detected with SW Overscheduling
28	X	X	No Fix	USB Low-Speed/Full-Speed EOP Issue
29	X	X	No Fix	USB PLL Control FSM Not Getting Reset on Global Reset
30	X	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
31	X	X	No Fix	Incorrect Data for LS or FS USB Periodic IN Transaction
32	X	X	No Fix	Intel® 5 Series and 3400 Series Chipset Family Delayed Periodic Traffic Timeout Issue

Specification Changes

Spec Change Number	Stepping		SPECIFICATION CHANGES
	B2	B3	
1	X	X	SMLink0 Speed Change
2	X	X	VccVRM Min/Max Change

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
1	003	Host WOL Behavior Clarification
2	003	Display Port Clarification
3	003	PIRQ Sharing
4	003	t205 Vcc Reference
5	003	Table 2-27 Power and Ground Signals
6	003	EHCI Function Numbers
7	003	PCI Express* Root Port Function Numbers
8	003	t212 Measurement Clarification
9	003	Wake Event Causes Update
10	003	SGPIO Reference Clock Speed

Documentation Changes (Sheet 1 of 2)

No.	Document Revision	DOCUMENTATION CHANGES
1	003	Correct Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*
2	003	Correct Table 8-8 DC Output Characteristics and Note 1
3	003	Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)
4	003	Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)
5	003	Correct 13.1.23 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)
6	003	Correct Table 2-28 Functional Strap Definitions
7	003	Correct Table 9-4 Memory Decode Ranges from Processor Perspective
8	003	Correct 10.1.43 OIC—Other Interrupt Control Register
9	003	Miscellaneous Typographical and Omission Error Corrections
10	003	Update Table 2-8 USB Interface Signals
11	003	Update Note 2 of Table 9-1 PCI Devices and Functions
12	003	Correct 14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2)
13	003	Correct 15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5)
14	003	Update Table 4-1 PCH System Clock Inputs
15	003	Update Table 2-20 Clock Interface Signals
16	003	Display Interface Updates

Documentation Changes (Sheet 2 of 2)

No.	Document Revision	DOCUMENTATION CHANGES
17	003	Correct Table 1-4. Intel® 5 Series Chipset Mobile SKUs
18	003	Correct Table 1-3. Intel® 5 Series Chipset Desktop SKUs
19	003	Controller Link Updates
20	003	Miscellaneous Typographical Error Corrections II
21	003	Remove note 11 on Table 3-3
22	003	Remove VccpNAND on Table 8-3 and Table 8-4
23	003	Section 8.2 Updates

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Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	Notes
B2	SLGWN	82PM55	Intel® PM55 Chipset
B2	SLGWV	82P55	Intel® P55 Chipset
B2	SLGWX	3400	Intel® 3400 Chipset
B2	SLGWW	3420	Intel® 3420 Chipset
B3	SLGZQ	82QM57	Intel® QM57 Chipset
B3	SLGZR	82HM57	Intel® H57 Chipset
B3	SLGZS	82HM55	Intel® HM55 Chipset
B3	SLGZW	82Q57	Intel® Q57 Chipset
B3	SLGZL	82H57	Intel® H57 Chipset
B3	SLGZX	82H55	Intel® H55 Chipset
B3	SLH25	3520	Intel® 3420 Chipset
B3	SLGZY	3450	Intel® 3450 Chipset
B3	SLGZV	82QS57	Intel® QS57 Chipset
B3	SLH23	82PM55	Intel® PM55 Chipset
B3	SLH24	82P55	Intel® P55 Chipset

PCH Device and Revision Identification

The Revision ID (RID) is traditionally an 8-bit register located at the offset 08h in the PCI header of every PCI device and function. The assigned value is based on the product's stepping.

Intel ® 5 Series Chipset and Intel ® 3400 Series Chipset Device and Revision ID Table (Sheet 1 of 2)

Device Function	Description	Dev ID[1]	B2 Rev ID	B3 Rev ID	Comments
D31:F0	LPC	3B02h	05h	06h	Intel® P55 Chipset
		3B03h	05h	06h	Intel® PM55 Chipset
		3B06h	n/a	06h	Intel® H55 Chipset
		3B07h	n/a	06h	Intel® QM57 Chipset
		3B08h	n/a	06h	Intel® H57 Chipset
		3B09h	n/a	06h	Intel® HM55 Chipset
		3B0Ah	n/a	06h	Intel® Q57 Chipset
		3B0Bh	n/a	06h	Intel® HM57 Chipset
		3B0Fh	n/a	06h	Intel® QS57 Chipset
		3B12h	05h	n/a	Intel® 3400 Chipset
		3B14h	05h	06h	Intel® 3420 Chipset
		3B16h	n/a	06h	Intel® 3450 Chipset
D31:F2	SATA	3B20h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)
		3B21h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0 and 1)
		3B22h	05h	06h	Desktop: AHCI (Ports 0-5)
		3B23h	05h	06h	Desktop: AHCI (Ports 0, 1, 4 and 5)
		3B25h	05h	06h	Desktop RAID: 0/1/5/10
		3B28h	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0, 1, 4 and 5)
		3B29h	05h	06h	Mobile: AHCI (Ports 0, 1, 4 and 5)
		3B2Ch	05h	06h	Mobile: RAID: 0/1/5/10
		3B2Eh	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)
		3B2Fh	05h	06h	Mobile: AHCI (Ports 0-5)

Intel ® 5 Series Chipset and Intel ® 3400 Series Chipset Device and Revision ID Table (Sheet 2 of 2)

Device Function	Description	Dev ID[1]	B2 Rev ID	B3 Rev ID	Comments
D31:F5	SATA	3B26h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
		3B2Dh	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	3B30h	05h	06h	
D31:F6	Thermal	3B32h	05h	06h	
D30:F0	DMI to PCI Bridge	244Eh	A5h	A6h	Desktop
D30:F0	DMI to PCI Bridge	2448h	A5h	A6h	Mobile
D29:F0	USB EHCI #1	3B34h	05h	06h	
D26:F0	USB EHCI #2	3B3Ch	05h	06h	
D27:F0	Intel High Definition Audio	3B56h	05h	06h	
D27:F0	Intel® High Definition Audio	3B57h	05h	06h	Intel® QS57 Chipset Only
D28:F0	PCI Express* Port 1	3B42h	05h	06h	
D28:F1	PCI Express Port 2	3B44h	05h	06h	
D28:F2	PCI Express Port 3	3B46h	05h	06h	
D28:F3	PCI Express Port 4	3B48h	05h	06h	
D28:F4	PCI Express Port 5	3B4Ah	05h	06h	
D28:F5	PCI Express Port 6	3B4Ch	05h	06h	
D28:F6	PCI Express Port 7	3B4Eh	05h	06h	
D28:F7	PCI Express Port 8	3B50h	05h	06h	
D25:F0	LAN[3]	3B41h	05h	06h	
D22:F0	Intel MEI #1	3B64h	05h	06h	
D22:F1	Intel MEI #2	3B65h	05h	06h	
D22:F2	IDE-R	3B66h	05h	06h	
D22:F3	KT	3B67h	05h	06h	

NOTES:

1. The PCH contains two SATA controllers. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.
3. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 3B41h is used. Refer to the appropriate Intel GbE Physical Layer Transceiver (PHY) Datasheet for LAN Device IDs.

Errata

1. Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB Test J/Test K Output Drive Level

Problem: Pre-emphasis is not disabled on high-speed USB ports during Test J/Test K.

Implication: J and K DC voltage levels may exceed USB 2.0 V_{HSOH}-MAX and V_{HSOL}-MAX during Test J/Test K testing and may not meet the USB 2.0 specification.

Workaround: Clear bit 1 of the USB Initialization Registers [0-13] prior to enabling Test J/Test K mode using a memory editing tool. This bit must be set back to 1 for each port after Test J/Test K testing is complete.

Port	Offset: RCBA + Offset:
0	3500h
1	3504h
2	3508h
3	350Ch
4	3510h
5	3514h
6	3518h
7	351Ch
8	3520h
9	3524h
10	3528h
11	352Ch
12	3530h
13	3534h

Status: No Fix. For steppings affected, see the Summary Table of Changes.

2. Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB 2.0 V_{hsoh}

Problem: High-Speed USB 2.0 V_{hsoh} may not meet the USB 2.0 Specification.

- The maximum expected V_{hsoh} is 495 mV.

Implication: Some motherboards may exceed specification limits during USB-IF compliance testing.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

3. Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA Signal Voltage Level

Problem: The Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA 1.5 Gb/s & 3.0 Gb/s (Gen1i, Gen1m, Gen2i, and Gen2m) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 7.2.1 of the Serial ATA Specification, rev 2.5).

Implication: None Known.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

4. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection

Problem: Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection (SLPD) may not recognize, or may falsely detect, a SATA hot-plug event during a Partial or Slumber Link Power Management (LPM) state.

Implication: On Systems which enable LPM, when a SATA device attached to the Intel® 5 Series Chipset and Intel® 3400 Series Chipset is configured as External or hot-plug capable, one of the following symptoms may occur:

- Symptom #1: A hot-plug or External SATA device removal which is not detected results in the OS and Intel® Matrix Storage Manager/Intel® Rapid Storage Technology console falsely reporting the device present, or incorrectly identifying an eSATA device.
- Symptom#2:A false hot-plug removal detection may occur resulting in OS boot hang or ODD media playback hang

Workaround: A driver workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

5. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio Interface Intermittently Does Not Play Sound

Problem: The Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio controller logic may not be gated by DMI L1 entry.

Implication: Systems may intermittently not play sound on the Intel HD Audio interface Following a DMI L1 exit.

Workaround: BIOS workaround available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

6. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation

Problem: Full-Speed isochronous-out transactions with multi-frame packets may be truncated, in the presence of Full or Low-Speed USB asynchronous transactions.

- For this to occur, two devices, one performing Full-Speed isochronous-out transactions and one performing asynchronous transactions must be connected to the same USB controller (Ports 0-7 and 8-13).

Implication: In the case of a USB audio device this issue may result in no audible impact or audible artifacts such as pops and clicks.

Note:

- High-Speed and Low-Speed USB devices are not impacted by this issue.
- Only devices supporting Full-Speed isochronous-out transactions that Intel is aware of are audio devices, such as sound adapters, speakers, and headphones.
- Intel has only observed the issue when a Full-Speed audio devices and Full-Speed USB web camera are connected to the same USB controller.

Workaround: None.

Status: Fixed For steppings affected, see the Summary Table of Changes.

7. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic

Problem: When a single USB bulk device is active on an EHCI controller, and the device has pending control and bulk traffic the PCH may not be able to resolve which traffic type is a priority and the associated with the device may stall.

- The processor must be in C0 for an extended period of time such as when Cx states are disabled, or if system traffic prevents the system from leaving C0.

Implication: The USB device may appear unresponsive. If Cx states are enabled the device may recover a short time later.

Note: Intel has only observed this failure on a limited number of devices. Failure only occurs if software associated with a USB device programs the Nak Count Reload bits defined in the EHCI Specification for USB Rev 1.0 to 0.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

8. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum

Problem: When SYNC Escape by a SATA device occurs on a D2H FIS, the PCH does not set the PxIS.IFS bit to ‘1.’ This deviates from section 6.1.9 of the Rev 1.3 Serial ATA Advanced Host Controller Interface (AHCI).

Implication: There is no known observable impact. Instead of detecting the IFS bit, software will detect a timeout error caused by the SYNC escape and then respond.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

9. Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® ME

Problem: Some Intel P55, PM55, 3400, and 3420 based systems with Intel ME Ignition 6.0.0.1126 PV firmware may fail to correctly initialize the Intel ME subsystem during boot at colder temperatures.

Implication: Failures may occur during BIOS update. Systems fans may run continuously at full speed and the system may have increased power consumption.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: Fixed. For steppings affected, see the Summary Table of Changes.

10. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue

Problem: If the PCH encounters a Full-Speed or Low-Speed USB transaction with errors, the PCH may retry the transaction without considering if the transaction can finish before the end of the current frame.

Implication: The implication is dependant on the USB device. The PCH will attempt to recover per error handling specified in Section 4.5.2 of the USB Specification 2.0. The device may hang and require cycle to resume normal functionality.

Note: Intel has only observed this behavior on a limited number of USB devices. The implication only occurs if a USB device does not correctly respond to error handling as specified Section 4.5.2 of the USB Specification 2.0.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

11. Intel® 5 / 3400 Series Chipset Family USB Classic Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependant. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None

Status: No Fix. For steppings affected, see the Summary Table of Changes.

12. Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports

Problem: The Intel H55 Express Chipset and Intel 3420 Chipset support 6 ports on RMH #1 and may incorrectly report 8 USB ports in the bNbrPorts field of the RMH hub descriptor.

Implication: If AC power is removed while the system is in hibernate, when the system resumes new USB devices may not be detected, and all devices on RMH #1 may not function.

Note: AC power removal while a system is in S4 is not a common occurrence.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

13. Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports

Problem: The Intel HM55 Express Chipset supports 6 ports on RMH #1 and will incorrectly report 8 USB ports in the bNbrPorts field of the RMH hub descriptor.

Implication: There are no known functional implications due to this issue on production Intel HM55 chipsets.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

14. Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue

Problem: A read transaction that immediately follows a write transaction to the HPET register space may return an incorrect value.

Implication: Implication is dependent on the usage model as noted below:

- For the HPET TIMn_COMP Timer 0 Comparator Value Register and HPET MAIN_CNT—Main Counter Value Register the issue could result in the software receiving stale data. This may result in undetermined system behavior.

  Note: Timers [1:7] are not affected by this issue.

- For TIMERn_VAL_SET_CNF bit 6 in the TIMn_CONF—Timer n Configuration there is no known usage model for reading this bit and there are no known functional implications.
- A write to the High Precision Timer Configuration (HPTC) register followed by a read to HPET register space may return all 0xFFFF_FFFFh.

Workaround: A workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

15. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering

Problem: When USB full-speed/low-speed port staggering is enabled, the PCH may not wait for the bus to return to an idle state after an End of Packet (EOP) and may incorrectly acknowledge bus noise as a data packet.

Implication: Some full-speed/low-speed devices may fail to enumerate and function.

Note: This issue has been seen with a minimum number of devices on some motherboard ports with certain cable and trace lengths.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

16. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Devices May Slow or Hang

Problem: When the processor is in C0, and a single bulk High-Speed USB device is active the port associated with the active device may hang.

Implication: The implication is device driver dependant. Intel has observed some USB devices may have decreased performance, or the device may hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

17. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Control Transactions

Problem: If the USB control buffers in the PCH Rate Matching Hub(s) are saturated with pending transactions the buffers may not be serviced in round robin order.

Implication: Some low-speed endpoints may not receive their pending control transactions.

Note: This issue has only been observed in synthetic test environment. The implication will be Device, driver and operating system specific.

Workaround: None

Status: No Fix. For steppings affected, see the Summary Table of Changes.

18. Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs

Problem: Intel® 5 Series Chipset and Intel® 3400 Series Chipset may not detect an unsolicited COMINIT from a SATA device

Implication: The SATA device may not be properly detected and configured resulting in the device Not functioning as expected.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

19. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset may not detect the unplug of a SATA 3.0 Gb/s device on a hot-plug enabled SATA port.

Implication: Unplugged SATA device may temporarily appear to be available.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

20. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK

Problem: Following system power cycling or S3-S5 resume, if both HS and LS/FS devices are attached to the same controller, the host controller may not respond to a HS device ACK during a Get Descriptor request from the host SW to a USB HS port.

Implication: USB high-speed devices may not be detected after a power cycling or S3-S5 resume.

- Intel has only observed this failure on a limited number of platforms. On a failing platform, the issue occurs infrequently.
- Full-speed and low-speed USB devices are not impacted by this issue.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

21. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA 6Gb/s Device Detection

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset may not be able to complete SATA Out Of Band (OOB) signaling with SATA 6Gb/s devices and down-shift to SATA 3Gb/s speed.

Implication: Intel 5® Series Chipset and Intel® 3400 Series Chipset may not detect a SATA 6Gb/s device upon power up or resume form S3, S4 or S5 State, resulting in indeterminate system behavior.

Workaround: None

Status: No Fix. For steppings affected, see the Summary Table of Changes.

22. Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset PCI Express Ports may not exit the disable state when the Link Control Register “Link Disable” bit is set and PCIe Device Electrical Idle Exit is detected.

Implication: Port Specific Software Directed Hot Plug or Power Management support using the “Link Disable” bit may cause an Intel 5® Series Chipset and Intel® 3400 Series Chipset PCI Express Port to be stuck in the “Link Disable state” until a Host Reset with Power Cycling occurs.

Workaround: For Intel 5® Series Chipset and Intel® 3400 Series Chipset PCI Express Port Specific Software Directed Hot Plug or Power Management support, use PCI Power Management Control register $D3_{HOT}$ bits instead of Link Disable bit.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

23. Pixel Corruption Over Integrated LVDS Interface of Intel® 5 Series Chipset

Problem: Pixel corruption may be observed over integrated LVDS interface on Mobile Intel® 5 Series Platforms.

Implication: Display artifacts may be seen upon mode sets (resolution changes, screen rotation) and/or system boot on the platforms that use integrated LVDS.

Note: Visual artifacts observed in LVDS dual channel mode with panels supporting maximum native resolution of 1920 x1080 and higher.

Workaround: VBIOS and Intel® Graphics Media Accelerator driver change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

24. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Family High-speed USB Device False Disconnect

Problem: Intel 5® Series Chipset and Intel® 3400 Series Chipset may falsely detect a USB high-speed (HS) device has been disconnected.

False detection is dependent upon:

— HS USB devices with termination impedance at the high-end or greater than USB2.0 specification.

— And USB ports routed with high motherboard trace impedance.

Implication: HS USB device will appear to be disconnected and no longer accessible until a device reset, such as a hot plug, to resume normal functionality.

Note: This issue has only been observed on a limited number of HS USB devices. This issue does not affect full-speed or low-speed USB devices

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

25. USB Isoch In Transfer Error Issue

Problem: If a USB Full-Speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a micro-frame the PCH may see more than 189 bytes in the next micro-frame.

Implication: If the PCH sees more than 189 bytes for a micro-frame an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a micro-frame. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the micro-frame.

Workaround: None.

Status: No Plan to Fix.

26. USB Full-Speed / Low-Speed Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: No Plan to Fix.

27. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for Full-Speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: No Plan to Fix.

28. USB Low-Speed/Full-Speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending Low-Speed or Full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending Low-Speed or Full-Speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device is entered suspend and may start sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress

Workaround: None.

Status: No Plan to Fix.

29. USB PLL Control FSM not Getting Reset on Global Reset

Problem: Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB PLL may not lock if a Global Reset occurs early during a cold boot sequence.

Implication: USB interface would not be functional an additional cold boot would be necessary to recover.

Workaround: None.

Status: No Plan to Fix.

30. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes Full-Speed and Low-Speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: No Plan to Fix.

31. Incorrect Data for LS or FS USB Periodic IN Transaction

Problem: The Periodic Frame list entry in DRAM for a USB LS or FS Periodic IN transaction may incorrectly get some of its data from a prior Periodic IN transaction which was initiated very late into the preceding Micro-frame.

It is considered good practice for software to schedule Periodic Transactions at the start of a Micro-frame. However Periodic transactions may occur late into a Micro-frame due to the following cases outlined below:

- Asynchronous transaction starting near the end of the proceeding Micro-frame gets Asynchronously retried

Note: Transactions getting Asynchronous retried would only occur for ill behaved USB device or USB port with a signal integrity issue

- Or Two Periodic transactions are scheduled by software to occur in the same Micro-frame and the first needs to push the second Periodic IN transaction to the end of the Micro-frame boundary

Implication: The implication will be device, driver or operating system specific.

Note: This issue has only been observed in a synthetic test environment

Workaround: None.

Status: No Plan to Fix.

32. Intel® 5 Series and 3400 Series Chipset Family Delayed Periodic Traffic Timeout Issue

Problem: If an interrupt transaction is pushed to the x+4 micro-frame boundary due to asynchronous retries, the RMH may not wait for the interrupt transaction to timeout before starting the next transaction.

IF RMH TT reaches a discard boundary, a timeout may be ignored.

Implication: If the next transaction is intended for the same device targeted by the interrupt, the successful completion of that transaction is device dependent and cannot be guaranteed. The implication may differ depending on the nature of transaction: (only impacts TT – FS / LS).

- If the transaction is asynchronous and the device does not respond, it will eventually be retried with no impact.
- If the transaction is periodic and the device does not respond, the transfer may be dropped. A single dropped periodic transaction should not be noticeable by end user.
- NOTE: This issue has only been seen in a synthetic environment

Workaround: None.

Status: No Plan to Fix.

Specification Changes

1. SMLink0 Speed Change

a. The text of section 5.14.2.2 is updated as shown:

The PCH supports the Advanced TCO mode in which SMLink0 and SMLink1 are used in addition to the host SMBus. See Figured 5-6 for more details. In this mode, the Intel ME SMBus controllers must be enabled by soft strap in the flash descriptor. See *SPI Flash Programming Guide Application Note* for more detail.

SMLink0 is dedicated to integrated LAN use and when an Intel PHY 82579 is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of 300 KHz - 400 KHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled via a soft strap (See *SPI Flash Programming Guide Application Note* for more detail).

SMLink1 is dedicated to Embedded Controller (EC) or Baseboard Management Controller (BMC) use. In the case where a BMC is connected to SMLink1, the BMC communicates with Management Engine through Intel ME SMBus connected to SMLink1. The host and TCO slave communicated with BMC through SMBus.

b. SMlink0 clock timings when operating in fast mode are added Table 8-22:

Sym	Parameter	Min	Max	Unit	Notes	Figure
SMLink0 Clock (SML0CLK) (See note 15)						
f_{smb}	Operating Frequency	0	400	KHz		
t22_SML	High time	0.6	50	µs	2	8-18
t23_SML	Low time	1.3	—	µs		8-18
t24_SML	Rise time	—	300	ns		8-18
t25_SML	Fall time	—	300	ns		8-18

c. Note 13 is added to table 8-22 as “When SMLink0 is configured to run in Fast Mode via a soft strap, the operating frequency is in the range of 300 KHz-400 KHz.”

d. Table 8-26 is updated as follows:

Table 8-26 SMBus and SMLink Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t130	Bus Free Time Between Stop and Start Condition	4.7	—	µs		8-18
$t130_{SM\ LFM}$	Bus Free Time Between Stop and Start Condition	1.3	—	µs	5	8-18
t131	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0	—	µs		8-18
$t131_{SM\ LFM}$	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	0.6	—	µs	5	8-18
t132	Repeated Start Condition Setup Time	4.7	—	µs		8-18
$t132_{SM\ LFM}$	Repeated Start Condition Setup Time	0.6	—	µs	5	8-18
t133	Stop Condition Setup Time	4.0	—	µs		8-18
$t133_{SM\ LFM}$	Stop Condition Setup Time	0.6	—	µs	5	8-18
t134	Data Hold Time	0	—	ns	4	8-18
$t134_{SM\ LFM}$	Data Hold Time	0	—	ns	4, 5	8-18
t135	Data Setup Time	250	—	ns		8-18
$t135_{SM\ LFM}$	Data Setup Time	100	—	ns	5	8-18
t136	Device Time Out	25	35	ms	1	
t137	Cumulative Clock Low Extend Time (slave device)	—	25	ms	2	8-19
t138	Cumulative Clock Low Extend Time (master device)	—	10	ms	3	8-19

e. Note 5 is added to table 8-26 as “Timings with the SMLFM designator apply only to SMLink0 and only when SMLink0 is operating in Fast Mode.”

2. VccVRM Min / Max Change

a. Table 8-9 is changed as shown:

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VccVRM	Internal PLL and VRMs (1.5V for Mobile)	1.455	1.5	1.545	V	1, 3
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)	1.746	1.8	1.854	V	1, 3

b. Note 3 is added to table 8-9 as “Includes only DC tolerance. AC tolerance will be 2% in addition to this range.”

Specification Clarification

1. Host WOL Behavior Clarification

The following note add to Section 5.3.4.1.1 and 5.3.4.1.2

5.3.4.1.1 Advanced Power Management Wake Up

Note: APM wake up settings will be restored to NVM default by the PCH when LAN connected Device (PHY) power is turned off and subsequently restored. Some example host WOL flows are:

When system transitions to G3 after WOL is disabled from the BIOS, APM host WOL would get enabled.

Anytime power to the LAN Connected Device (PHY) is cycled while in S4/S5 after WOL is disabled from the BIOS, APM host WOL would get enabled. Anytime power to the LAN Connected Device (PHY) is cycled while in S3, APM host WOL configuration is lost.

5.3.4.1.2 ACPI Power Management Wake Up

Note: ACPI wake up settings are not preserved when the LAN Connected Device (PHY) power is turned off and subsequently restored. Some example host WOL flows are:

Anytime power to the LAN Connected Device (PHY) is cycled while in S3 or S4, ACPI host WOL configuration is lost.

2. DisplayPort Clarification

The following note add to Section 5.27.2.8

5.27.2.8 Display Port

Note: DisplayPort includes support for Dual-Mode operation, refer to the Platform Design Guide for more details on Dual-mode implementation.

3. PIRQ Sharing

A note is added to table 2-7 as “PIRQ Interrupts can only be shared if it is configured as level sensitive. They cannot be shared if configured as edge triggered.”

4. t205 Vcc Reference

Table 8-35 is changed as shown below:

Sym	Parameter	Min	Max	Units	Notes	Fig
t205	Vcc active to PWROK high	10	—	ms	5	8-2, 8-3

5. Table 2-27 Power and Ground Signals

Name	Description
DcpSusByp	**Decoupling:** 1.05 V Suspend well supply that is supplied internally by Internal VRs. This signal requires decoupling.

6. EHCI Function Numbers

The following note is added to table 9-1 and section 16.1:

Prior to BIOS initialization of the PCH USB subsystem, the EHCI controllers will appear as Function 7. After BIOS initialization, the EHCI controllers will be Function 0.

7. PCI Express* Root Port Function Numbers

a. The following note is added to table 9-1:

This table shows the default PCI Express Function Number-to-Root Port mapping. Function numbers for a given root port are assignable through the “Root Port Function Number and Hide for PCI Express Root Ports” register (RCBA+0404h).

b. The following note is added to the first paragraph of section 5.2 and section 19.1:

This section assumes the default PCI Express Function Number-to-Root Port mapping is used. Function numbers for a given root port are assignable through the “Root Port Function Number and Hide for PCI Express Root Ports” registers (RCBA+0404h).

8. t212 Measurement Clarification

The following note is added to table 8-35:

18. LAN_RST# high to SPI Soft-Start Read is an internal PCH timing. The timing cannot be measured externally and included here for general power sequencing reference.

9. Wake Event Causes Update

The following replaces table 5-27:

Table 5-27 Causes of Wake Events (Sheet 1 of 2)

Cause	How Enabled	Wake from S1, Sx	Wake from S1, Sx After Power Loss (Note 1)	Wake from “Reset” Types (Note 2)
RTC Alarm	Set RTC_EN bit in PM1_EN register.	Y	Y	
Power Button	Always enabled as Wake event.	Y	Y	Y
GPI[15:0]	GPE0_EN register ***Note:*** GPI’s that are in the core well are not capable of waking the system from sleep states when the core well is not powered.	Y		
GPIO27	Set GP27_EN in GPE0_EN Register.	Y	Y	Y
LAN	Will use PME#. Wake enable set with LAN logic.	Y	Y	

Table 5-27 Causes of Wake Events (Sheet 2 of 2)

Cause	How Enabled	Wake from S1, Sx	Wake from S1, Sx After Power Loss (Note 1)	Wake from "Reset" Types (Note 2)
RI#	Set RI_EN bit in GPE0_EN register.	Y	Y	
Intel® High Definition Audio	Event sets PME_B0_STS bit; PM_B0_EN must be enabled. Can not wake from S5 state if it was entered due to power failure or power button override.	Y	Y	
Primary PME#	PME_B0_EN bit in GPE0_EN register.	Y	Y	
Secondary PME#	Set PME_EN bit in GPE0_EN register.	Y	Y	
PCI_EXP_WAKE #	PCI_EXP_WAKE bit. (Note 3)	Y	Y	
SATA	Set PME_EN bit in GPE0_EN register. (Note 4)	S1	S1	
PCI_EXP PME Message	Must use the PCI Express* WAKE# pin rather than messages for wake from S3, S4, or S5.	S1	S1	
SMBALERT#	Always enabled as Wake event.	Y	Y	Y
SMBus Slave Wake Message (01h)	Wake/SMI# command always enabled as a Wake event. Note: SMBus Slave Message can wake the system from S1–S5, as well as from S5 due to Power Button Override.	Y	Y	Y
SMBus Host Notify message received	HOST_NOTIFY_WKEN bit SMBus Slave Command register. Reported in the SMB_WAK_STS bit in the GPEO_STS register.	Y	Y	Y
Intel® ME Non-Maskable Wake	Always enabled as a wake event.	Y	Y	Y
Integrated WOL Enable Override	WOL Enable Override bit (in Configuration Space).	Y	Y	Y

NOTES:

1. This column represents what the PCH would honor as wake events but there may be enabling dependencies on the device side which are not enabled after a power loss.
2. Reset Types include: Power Button override, Intel ME initiated power button override, Intel ME initiated host partition reset with power down, Intel ME Watchdog Timer, SMBus unconditional power down, Processor thermal trip, PCH catastrophic temperature event.
3. When the WAKE# pin is active and the PCI Express device is enabled to wake the system, the PCH will wake the platform.
4. SATA can only trigger a wake event in S1, but if PME is asserted prior to S3/S4/S5 entry and software does not clear the PME_B0_STS, a wake event would still result.

10. SGPIO Reference Clock Speed

SCLOCK Description in table 2-5 is updated as follows:

Name	Type	Description
SCLOCK/GPIO22	OD O	**SGPIO Reference Clock:** The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. The SCLOCK frequency supported is 32 kHz. If SGPIO interface is not used, this signal can be used as GPIO22.

11. I²C Block Read/Write Buffer

In section 5.20.1.1, the following note is added after the Block Read/Write description as shown:

The PCH contains a 32-byte buffer for read and write data which can be enabled by setting bit 1 of the Auxiliary Control register at offset 0Dh in I/O space, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the PCH, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

When operating in I²C mode (I2C_EN bit is set), the PCH will never use the 32-byte buffer for any block commands.

Documentation Changes

1. Correct Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*

The following changes applies to Table 5-58

Table 5-58 PCH supported Audio formats over HDMI and DisplayPort*

Audio Formats	HDMI	DisplayPort
AC-3 - Dolby Digital	Yes	No
Dolby* Digital Plus	Yes	No
DTS-HD*	Yes	No
LPCM, 192 KHz/24 bit, 8 Channel	Yes	Yes (two channel - upto 96 KHz 24 bit)
Dolby True HD, DTS HD Master Audio (Losses Blu-Ray Audio Format)	Yes	No

2. Correct Table 8-8 DC Output Characteristics and NOTES 1.

The following changes applies to Table 8-8

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL3}	Output Low Voltage	0	0.4	V	4 mA	
V_{OH3}	Output High Voltage	3.3 V - 0.5	—	V	-2 mA	Note 1, 7

NOTES:

1. The SERR#, PIRQ[H:A], SMBDATA, SMBCLK, SML[1:0]CLK, SML[1:0]DATA, SML[1:0] ALERT# and PWM[3:0] signal has an open-drain driver and SATALED# has an open-collector driver, and the VOH / IOH specification does not apply. This signal must have external pull up resistor.

3. Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Bit	Description
13	**Flash Descriptor Override Pin Strap Status (FDOPSS)—** RO. This bit reflects the value the Flash Descriptor Override Pin-Strap. 0 = The Flash Descriptor Override strap is set 1 = No override

4. Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Bit	Description
13	**Flash Descriptor Override Pin Strap Status (FDOPSS)—** RO. This bit reflects the value the Flash Descriptor Override Pin-Strap. 0 = The Flash Descriptor Override strap is set 1 = No override

5. Correct 13.1.23 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)

Bit	Description
15:2	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)—**R/W. **NOTE:** The PCH Does not provide decode down to the word or byte level

6. Correct Table 2-28 Functional Strap Definitions

Signal	Usage	When Sampled	Comment
SPI_MOSI	Reserved	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.

7. Correct Table 9-4 Memory Decode Ranges from Processor Perspective

Memory Range	Target	Dependency/Comments
FED4 0000h–FED4 BFFFh	TPM on LPC	

8. Correct 10.1.43 OIC—Other Interrupt Control Register

Bit	Description
11	Reserved

9. Miscellaneous Typographical and Omission Error Corrections

a. Section 10.1.67 MISCCTL—Miscellaneous Control Register RCBA+3590h is replaced as follows:

Bit	Description
31:2	Reserved.
1	**EHCI 2 USBR Enable** — R/W. When set, this bit enables support for the USB-r redirect device on the EHCI controller in Device 26. SW must complete programming the following registers before this bit is set: 1. Enable RMH 2. HCSPARAMS (N_CC, N_Ports)

Bit	Description
0	**EHCI 1 USBR Enable** — R/W. When set, this bit enables support for the USB-r redirect device on the EHCI controller in Device 29. SW must complete programming the following registers before this bit is set: 1. Enable RMH 2. HCSPARAMS (N_CC, N_Ports)

b. The SATA RAID controller Device IDs when the AIE bit is set are corrected in 14.1.33 as shown below. The Device IDs with the AIE bit cleared are also added to the Device and Revision ID table in section 2.28.

Bit	Description
7 (RAID Capable SKUs Only)	**Alternate ID Enable (AIE)** — R/WO. 0 = When in RAID mode the SATA Controller located at Device 31: Function 2 will report the following Device ID 2822h for Desktop or 282Ah for Mobile and the Microsoft Windows Vista* in-box version of the Intel® Rapid Storage Manager will load on the platform. 1 = When in RAID mode the SATA Controller located at Device 31: Function 2 will report the following Device ID 3B25h for Desktop or 3B2Ch for Mobile to prevent the Microsoft Windows Vista in-box version of the Intel® Rapid Storage Manager from loading on the platform and will require the user to perform an 'F6' installation of the appropriate Intel® Rapid Storage Manager. **NOTE:** This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST#. BIOS is required to reprogram the value of this bit after resuming from S3, S4 and S5.

c. Section 10.1.69 (USBOCM2 - Overcurrent MAP Register 2) is updated as follows:

Bit	Description
31:30	Reserved
29:24	**OC7 Mapping** Each bit position maps OC7# to a set of ports as follows: The OC7# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 29 28 27 26 25 24 **Port** 13 12 11 10 9 8
23:22	Reserved
21:16	**OC6 Mapping** Each bit position maps OC6# to a set of ports as follows: The OC6# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 21 20 19 18 17 16 **Port** 13 12 11 10 9 8
15:14	Reserved

Bit	Description
13:8	**OC5 Mapping** Each bit position maps OC5# to a set of ports as follows: The OC5# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 13 12 11 10 9 8 **Port** 13 12 11 10 9 8
7:6	Reserved
5:0	**OC4 Mapping** Each bit position maps OC4# to a set of ports as follows: The OC4# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 5 4 3 2 1 0 **Port** 13 12 11 10 9 8

d. D31:F1 references are changed to D31:F2 or D31:F5, where appropriate, throughout the document.

10. Update Table 2-8 USB Interface Signals

Name	Type	Description
OC0# / GPIO59 **OC1#** / GPIO40 **OC2#** / GPIO41 **OC3#** / GPIO42 **OC4#** / GPIO43 **OC5#** / GPIO9 **OC6#** / GPIO10 **OC7#** / GPIO14	I	**Overcurrent Indicators**: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. These signals can instead be used as GPIOs. **NOTES:** 1. OC# pins are not 5 V tolerant. 2. Depending on platform configuration, sharing of OC# pins may be required. 3. OC#[3:0] can only be used for EHCI controller #1 4. OC#[4:7] can only be used for EHCI controller #2

11. Update Note 2 of Table 9-1 PCI Devices and Functions

It is updated to “SATA controller 2 (D31:F5) is only visible when D31:F2 CC.SCC=01h.”

12. Correct 14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2)

Bit	Description
0	**Start/Stop Bus Master (START)** — R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit (D31:F2:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F2:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. ***Note:*** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then the PCH will not send DMAT to terminate the data transfer. SW intervention (such as, sending SRST) is required to reset the interface in this condition.

13. Correct 15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5)

Bit	Description
0	**Start/Stop Bus Master (START)** — R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit (D31:F5:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F5:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. ***Note:*** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then the PCH will not send DMAT to terminate the data transfer. SW intervention (such as, sending SRST) is required to reset the interface in this condition.

14. Update Table 4-1 PCH System Clock Inputs

Clock Domain	Frequency	Usage
CLKIN_BCLK_P, CLKIN_BCLK_N	133 MHz	133 MHz differential reference clock from a clock chip in Buffer-Through Mode.

15. Update Table 2-20 Clock Interface Signals

Name	Type	Description
CLKIN_BCLK_P, CLKIN_BCLK_N	I	133 MHz differential reference clock from a clock chip in Buffer-Through Mode.

16. Display Interface Updates

a. In section 1.2, Embedded DisplayPort is added to the list supported Analog and Digital Display ports.

b. The following two paragraphs are added to section 1.2.1:

PCH Display Interface

PCH integrates latest display technologies such as HDMI*, DisplayPort*, Embedded DisplayPort (eDP*), SDVO, and DVI along with legacy display technologies: Analog Port (VGA) and LVDS (mobile only). The Analog Port and LVDS Port are dedicated ports on the PCH and the Digital Ports B, C and D can be configured to drive HDMI, DVI, or DisplayPort. Digital Port B can also be configured as SDVO while Digital Port D can be configured as eDP. The HDMI interface supports the HDMI* 1.3C specification while the DisplayPort interface supports the DisplayPort* 1.1a specification. PCH supports High-bandwidth Digital Content Protection for high definition content playback over digital interfaces. PCH also integrates audio codecs for audio support over HDMI and DisplayPort interfaces.

PCH receives the display data over the Intel® FDI and transcodes the data as per the display technology protocol and sends the data through the display interface.

Intel® Flexible Display Interconnect (FDI)

Intel® FDI connects the display engine in the processor with the display interfaces on the PCH. The display data from the frame buffer is processed by the display engine and sent to the PCH where it is transcoded and driven out on the panel. Intel FDI involves two channels – A and B for display data transfer.

Intel® FDI supports maximum data rate of 2.7Gb/s per lane.

c. The following replaces section 5.27:

5.27 PCH Display Interfaces

The PCH integrates one Analog, LVDS (mobile only) and three Digital Ports B, C, and D. Each Digital Port can transmit data according to one or more protocols. Digital Port B, C and D can be configured to drive natively HDMI, DisplayPort or DVI. Digital Port B also supports Serial Digital Video Out (SDVO) that converts one protocol to another. Digital Port D can be configured to drive natively Embedded DisplayPort (eDP). Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The PCH's Analog Port uses an integrated 340.4 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.

The PCH SDVO port (configured through Digital Port B) is capable of driving a 200 MP/s (Megapixels/second) rate.

Each Digital Port is capable of driving a digital display up to 2560x1600 at 60 Hz using DisplayPort and 1920x1200 at 60 Hz using HDMI, DVI (with reduced blanking).

5.27.1 Analog Display Interface Characteristics

The Analog Port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair that is implemented using GPIO pins dedicated to the Analog Port. The intended target device is for a monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

Figure 5-14. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5V
	Control	Through GPIO interface

5.27.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the VGA monitor. The PCH's integrated 340.4 MHz RAMDAC supports resolutions up to 2048x1536 at 75 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

5.27.1.1.1 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support are included.

5.27.1.1.2 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

5.27.1.2 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug- and-play systems to be realized. Support for DDC 1 and 2 is implemented. The PCH uses the DDC_CLK and DDC_DATA signals to communicate with the analog monitor. The PCH will generate these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

5.27.2 Digital Display Interfaces

The PCH can drive a number of digital interfaces natively. The Digital Ports B, C, and/or D can be configured to drive HDMI, DVI, DisplayPort, and Embedded DisplayPort (port D only). The PCH provides a dedicated port for Digital Port LVDS (mobile only).

5.27.2.1 LVDS (Mobile only)

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics.

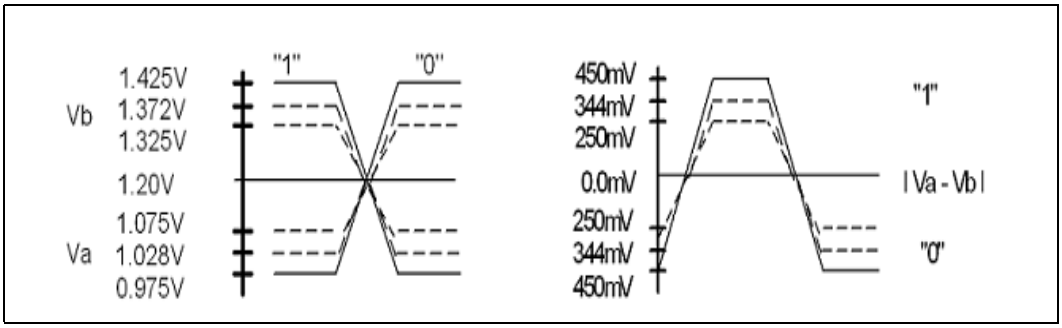
Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, each carry a portion of the data; thus, doubling the throughput to a maximum theoretical pixel rate of 224 MP/s.

There are two LVDS transmitter channels (Channel A and Channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each.

The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals.

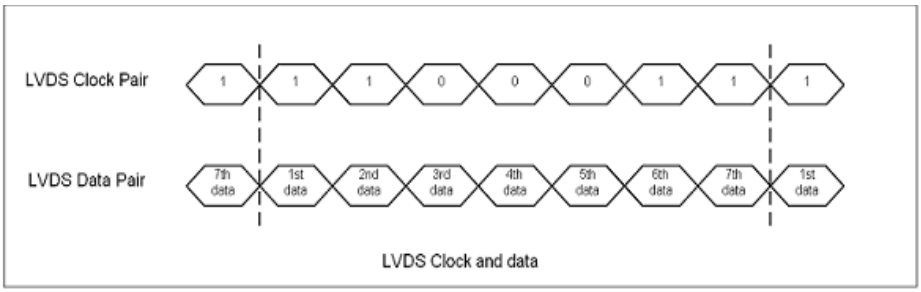
Figure 5-15 shows a pair of LVDS signals and swing voltage.

Figure 5-15. LVDS Signals and Swing Voltage



Logic values of 1s and 0s are represented by the differential voltage between the pair of signals. As shown in the Figure 5-16 a serial pattern of 1100011 represents one cycle of the clock.

Figure 5-16. LVDS Clock and Data Relationship



5.27.2.2 LVDS Pair States

The LVDS pairs can be put into one of five states:

- Active
- Powered down Hi-Z
- Powered down 0 V
- Common mode
- Send zeros

When in the active state, several data formats are supported. When in powered down state, the circuit enters a low power state and drives out 0 V or the buffer is the Hi-Z state on both the output pins for the entire channel. The common mode Hi-Z state is both pins of the pair set to the common mode voltage. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

The LVDS Port can be enabled/disabled using software. A disabled port enters a low power state. Once the port is enabled, individual driver pairs may be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0s output.

Individual pairs or sets of LVDS pairs can be selectively powered down when not being used. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

5.27.2.3 Single Channel versus Dual Channel Mode

In the single channel mode, only Channel-A is used. Channel-B cannot be used for single channel mode. In the dual channel mode, both Channel-A and Channel-B pins are used concurrently to drive one LVDS display.

In Single Channel mode, Channel A can take 18 bits of RGB pixel data, plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs; or 24 bits of RGB (plus 4 bits of timing control) output on four differential data pair outputs. A dual channel interface converts 36 or 48 bits of color information plus the 3 or 4 bits of timing control respectively and outputs it on six or eight sets of differential data outputs respectively.

Dual Channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out Channel-A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

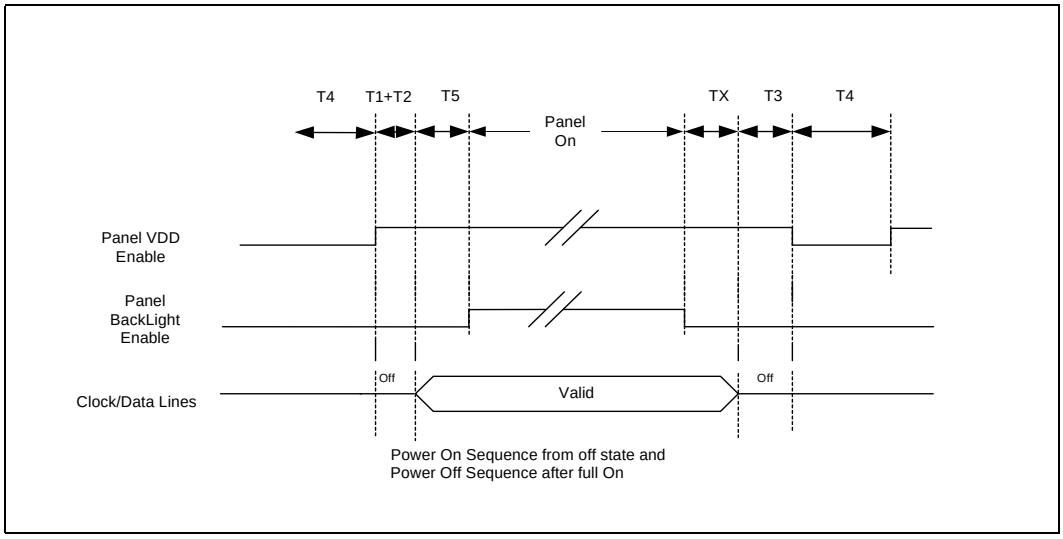
Note: Platforms using the PCH for integrated graphics support 24-bpp display panels of Type 1 only (compatible with VESA LVDS color mapping).

5.27.2.4 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. To meet the panel power timing specification requirements two signals, LFP_VDD_EN and LFP_BKLT_EN, are provided to control the timing sequencing function of the panel and the backlight power supplies.

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

Figure 5-17. Panel Power Sequencing



NOTE: Support for programming parameters TX and T1 through T5 using software is provided.

5.27.2.5 LVDS DDC

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then 'locked' into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA.

The LVDS DDC helps to reads the panel timing parameters or panel EDID.

5.27.2.6 High-Definition Multimedia Interface

The High-Definition Multimedia Interface (HDMI) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the PCH and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

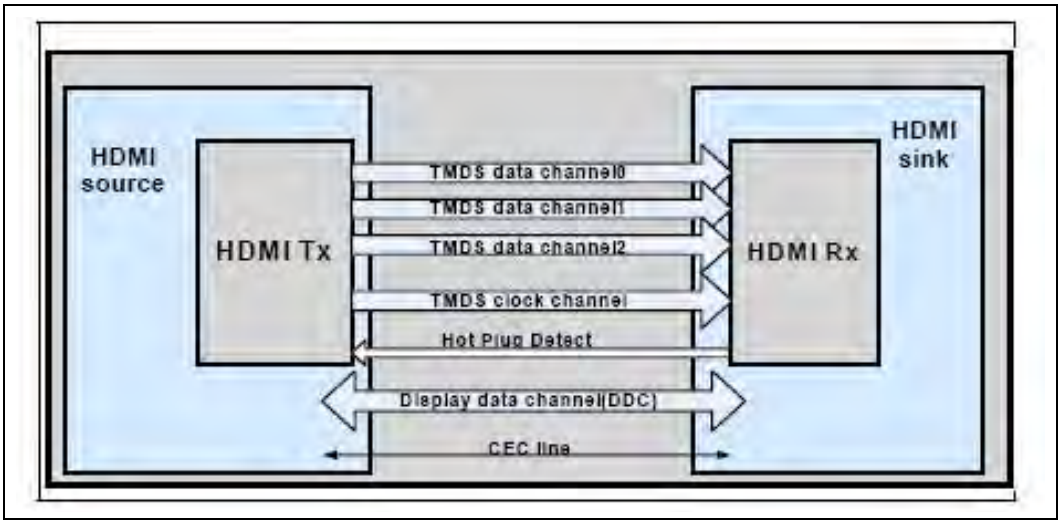
HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) (not supported by the PCH). As shown in Figure 5-18, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

PCH HDMI interface is designed as per High-Definition Multimedia Interface Specifica-

tion 1.4a. The PCH supports High-Definition Multimedia Interface Compliance Test Specification 1.4a.

Figure 5-18. HDMI Overview



5.27.2.7 Digital Video Interface (DVI)

The PCH Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver which is similar to the HDMI protocol but the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals is connected along with the digital data and clock signals from one of the Digital Ports. When a system has support for a DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

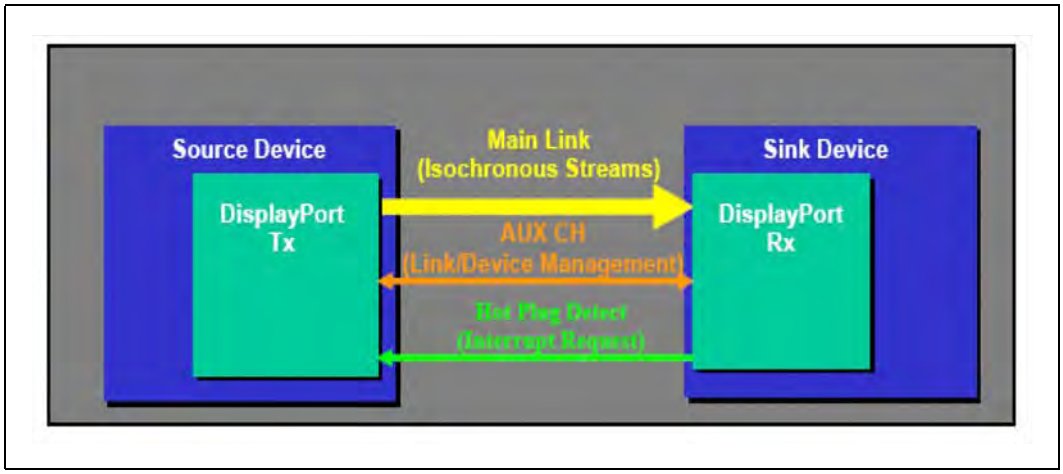
5.27.2.8 DisplayPort*

DisplayPort is a digital communication interface that utilizes differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A DisplayPort consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a uni-directional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

PCH is designed as per VESA DisplayPort Standard Version 1.1a. The PCH supports VESA DisplayPort* PHY Compliance Test Specification 1.1 and VESA DisplayPort* Link Layer Compliance Test Specification 1.1.

Figure 5-19. DisplayPort Overview



5.27.2.9 Embedded DisplayPort

Embedded DisplayPort (eDP*) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PC's. eDP is supported only on Digital Port D. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

The eDP support on desktop PCH is possible because of the addition of the panel power sequencing pins: L_VDD, L_BKLT_EN and L_BLKT_CTRL. The eDP on the PCH can be configured for 2 or 4 lanes.

PCH supports Embedded DisplayPort* (eDP*) Standard Version 1.1.

5.27.2.10 DisplayPort Aux Channel

A bi-directional AC coupled AUX channel interface replaces the I^2C for EDID read, link management and device control. I^2C-to-Aux bridges are required to connect legacy display devices.

5.27.2.11 DisplayPort Hot-Plug Detect (HPD)

The PCH supports HPD for Hot-Plug sink events on the HDMI and DisplayPort interface.

5.27.2.12 Integrated Audio over HDMI and DisplayPort

DisplayPort and HDMI interfaces on PCH support audio. The below table shows the supported audio technologies on the PCH.

Table 5-58. PCH supported Audio formats over HDMI and DisplayPort*

Audio Formats	HDMI	DisplayPort
AC-3 - Dolby* Digital	Yes	No
Dolby Digital Plus	Yes	No
DTS-HD*	Yes	No
LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes (two channel - up to 96 kHz 24 bit)
Dolby TrueHD, DTS-HD Master Audio* (Losses Blu-ray Disc* Audio Format)	Yes	No

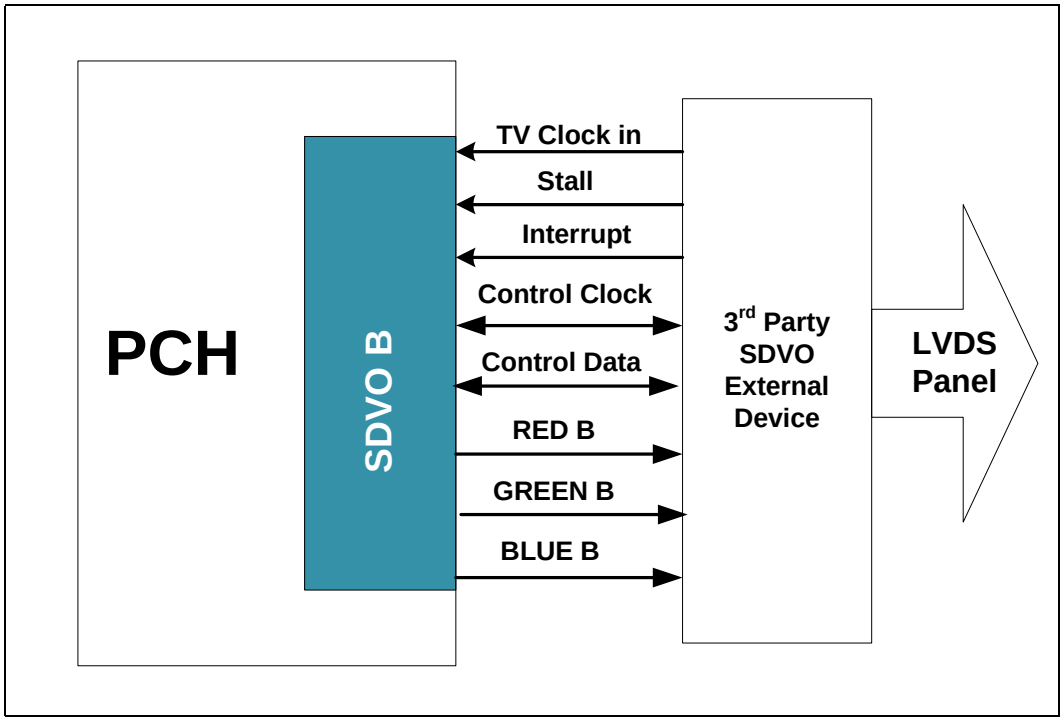
PCH adds support for Silent stream. Silent stream is a integrated audio feature that enables short audio streams such as system events to be heard over the HDMI and DisplayPort monitors. PCH supports silent streams over the HDMI and DisplayPort interfaces at 48 kHz, 96 kHz, and 192 kHz sampling rates.

5.27.2.13 Serial Digital Video Out (SDVO)

Serial Digital Video Out (SDVO) supports SDVO-LVDS only on the PCH. Though the SDVO electrical interface is based on the PCI Express interface, the protocol and timings are completely unique. The PCH utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

SDVO is supported only on Digital Port B of the PCH.

Figure 5-20. SDVO Conceptual Block Diagram



5.27.2.14 Control Bus

Communication to SDVO registers and if utilized, ADD2 PROMs and monitor DDCs, are accomplished by using the SDVOCTRLDATA and SDVOCTRLCLK signals through the SDVO device. These signals run up to 400 kHz and connect directly to the SDVO device.

The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device data sheets for level shifting requirements of these signals.

5.27.3 Mapping of Digital Display Interface Signals

Table 5-59. PCH Digital Port Pin Mapping

Port Description	DisplayPort* Signals	HDMI* Signals	SDVO Signals	PCH Display Port Pin details
Port B	DPB_LANE3	TMDSB_CLK	SDVOB_CLK	DDPB_[3]P
	DPB_LANE3#	TMDSB_CLKB	SDVOB_CLK#	DDPB_[3]N
	DPB_LANE2	TMDSB_DATA0	SDVOB_BLUE	DDPB_[2]P
	DPB_LANE2#	TMDSB_DATA0B	SDVOB_BLUE#	DDPB_[2]N
	DPB_LANE1	TMDSB_DATA1	SDVOB_GREEN	DDPB_[1]P
	DPB_LANE1#	TMDSB_DATA1B	SDVOB_GREEN#	DDPB_[1]N
	DPB_LANE0	TMDSB_DATA2	SDVOB_RED	DDPB_[0]P
	DPB_LANE0#	TMDSB_DATA2B	SDVOB_RED*	DDPB_[0]N
	DPB_HPD	TMDSB_HPD		DDPB_HPD
	DPB_AUX			DDPB_AUXP
	DPB_AUXB			DDPB_AUXN
Port C	DPC_LANE3	TMDSC_CLK		DDPC_[3]P
	DPC_LANE3#	TMDSC_CLKB		DDPC_[3]N
	DPC_LANE2	TMDSC_DATA0		DDPC_[2]P
	DPC_LANE2#	TMDSC_DATA0B		DDPC_[2]N
	DPC_LANE1	TMDSC_DATA1		DDPC_[1]P
	DPC_LANE1#	TMDSC_DATA1B		DDPC_[1]N
	DPC_LANE0	TMDSC_DATA2		DDPC_[0]P
	DPC_LANE0#	TMDSC_DATA2B		DDPC_[0]N
	DPC_HPD	TMDSC_HPD		DDPC_HPD
	DPC_AUX			DDPC_AUXP
	DPC_AUXC			DDPC_AUXN
Port D	DPD_LANE3	TMDSD_CLK		DDPD_[3]P
	DPD_LANE3#	TMDSD_CLKB		DDPD_[3]N
	DPD_LANE2	TMDSD_DATA0		DDPD_[2]P
	DPD_LANE2#	TMDSD_DATA0B		DDPD_[2]N
	DPD_LANE1	TMDSD_DATA1		DDPD_[1]P
	DPD_LANE1#	TMDSD_DATA1B		DDPD_[1]N
	DPD_LANE0	TMDSD_DATA2		DDPD_[0]P
	DPD_LANE0#	TMDSD_DATA2B		DDPD_[0]N
	DPD_HPD	TMDSD_HPD		DDPD_HPD
	DPD_AUX			DDPD_AUXP
	DPD_AUXD			DDPD_AUXN

5.27.4 Multiple Display Configurations

Microsoft Windows* XP, Windows Vista* and Windows* 7 operating systems supports multiple displays. PCH has two pipes which send the display data out through the ports. Two display pipes enables the PCH to support two different images on different display devices.

- **Single Display** is a mode with one display port activated to display the output to one display device.
- **Intel® Dual Display Clone** is a mode with two display ports activated to display the same output to two different display devices with the same color depth setting, but potentially different refresh rates and resolution settings.
- **Extended Desktop** is a mode with two display ports activated used to display two different outputs to two different display devices with potentially different color depth, refresh rate, and resolution settings.

Table 5-61 describes the valid interoperability between display technologies.

Table 5-60. Display Co-Existence Table

Display	Not Attached	DAC / VGA	Integrated LVDS	Integrated DisplayPort*	HDMI*/DVI	eDP*
Not Attached	X	S	S	S	S	S
DAC / VGA	S	X	S[1], C, E	A	A	S[1], C, E
Integrated LVDS	S	S[1], C, E	X	S[1], C, E	S[1], C, E	X
Integrated DisplayPort	S	A	S[1], C, E	A	A	S[1], C, E
HDMI/DVI	S	A	S[1], C, E	A	X	S[1], C, E
SDVO LVDS	S	S[1], C, E	X	S[1], C, E	S[1], C, E	X
eDP	S	S[1], C, E	X	S[1], C, E	S[1], C, E	X

- A = Single Pipe Single Display, Intel® Dual Display Clone (Only 24-bpp), or Extended Desktop Mode
- C = Clone Mode
- E = Extended Desktop Mode
- S = Single Pipe Single Display
- S[1] = Single Pipe Single Display With One Display Device Disabled
- X = Unsupported/Not Applicable

5.27.5 High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor and TV's). The PCH supports HDCP 1.4 for content protection over wired displays (HDMI, DVI and DisplayPort).

The HDCP 1.4 keys are integrated into the PCH and customers are not required to physically configure or handle the keys.

5.27.6 Intel® Flexible Display Interconnect

Intel® FDI connects the display engine in the processor with the display interfaces on the PCH. The display data from the frame buffer is processed in the display engine of the processor and sent to the PCH over the Intel FDI where it is transcoded as per the display protocol and driven to the display monitor.

Intel FDI has two channels A and B. Each channel has 4 lanes and total combined is 8 lanes to transfer the data from the processor to the PCH. Depending on the data bandwidth the interface is dynamically configured as x1, x2 or x4 lanes. Intel FDI supports lane reversal and lane polarity reversal.

17. Correct Table 1-4. Intel® 5 Series Chipset Mobile SKUs

Feature Set	SKU Name(s)				
	QM57	HM57	PM55	HM55	QS57
HDMI/DVI/VGA/SDVO/DisplayPort/eDP	Yes	Yes	No	Yes	Yes

18. Correct Table 1-3. Intel® 5 Series Chipset Desktop SKUs

Feature Set	SKU Name(s)				
	Q57	H57	H55	P55	**B55**
HDMI/DVI/VGA/SDVO/DisplayPort/eDP	Yes	Yes	Yes	No	Yes

19. Controller Link Updates

a. Controller Link is supported on all platforms. References to “Mobile Only” are removed throughout the document.

b. Controller Link signal names are updated as follows throughout the document:

CL_RST# corrected to CL_RST1#

CL_CLK corrected to CL_CLK1

CL_DATA corrected to CL_DATA1

c. AC timings are added in Section 8.6:

Table 8-35 Controller Link Receive Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t190	Single bit time	13	—	ns		8-30
t191	Single clock period	15	—	ns		8-30
t192	Rise time/Fall time	0.11	3.5	V/ns	1	8-31
t193	Setup time before CL_CLK1	0.9	—	ns		8-30
t194	Hold time after CL_CLK1	0.9	—	ns		8-30
V_{IL_AC}	Input low voltage (AC)		CL_Vref - 0.08	V	2	
V_{IH_AC}	Input high voltage (AC)	CL_Vref +0.08		V	2	

NOTES:
1. Measured from (CL_Vref - 50mV to CL_Vref + 50mV) at the receiving device side. No test load is required for this measurement as the receiving device fulfills this purpose.
2. CL_Vref = 0.12*(VccSus3_3).

d. The following figures are added to section 8.9:

Figure 8-30 Controller Link Receive Timings

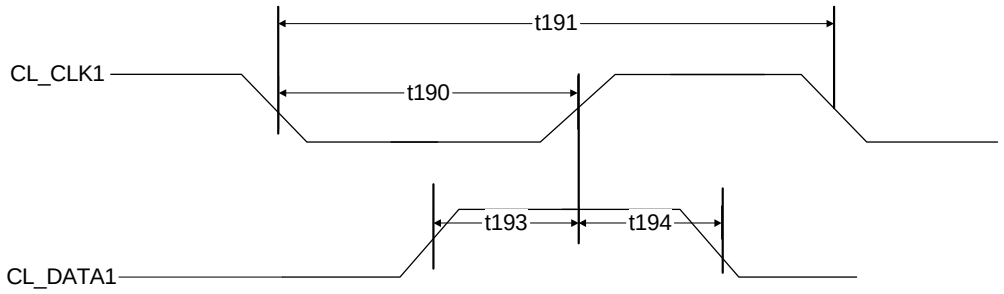
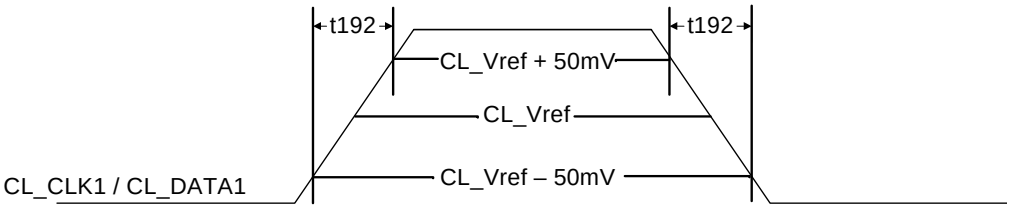


Figure 8-31 Controller Link Receive Slew Rate



e. CL_RST0# references are changed to CL_RST1#

f. Controller Link signals are added to table 3-3:

Signal Name	Power Plane	During Reset[1]	Immediately after Reset[1]	S0/S1	S3	S4/S5
Controller Link						
CL_CLK1[6]	Suspend	High/Low[15]	High/Low[15]	Defined	Defined	Defined
CL_DATA1[6]	Suspend	High/Low[15]	High/Low[15]	Defined	Defined	Defined
CL_RST1#[6]	Suspend	Low	High	High	High	High

g. Note 15 is added to table 3-3 as follows:

15. Controller Link Clock and Data buffers use internal pull-up and pull-down resistors to drive a logical 1 or a 0.

h. Link Controller references are changed to Controller Link.

20. Miscellaneous Typographical Error Corrections II

a. Default values for section 23.5.14 SID—Subsystem ID Register (D22:F2) and section 23.9.11 SID—Subsystem ID Register (D22:F3) are corrected from 0000h to 8086h.

b. ACPI 3.0b references are changed to ACPI 4.0a throughout the document.

c. Mobile Only / Desktop Only tags are removed from bits 27:26 of section 10.1.64 CG—Clock Gating (RCBA+341Ch) as shown:

Bit	Description
27	**SATA Port 3 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 3 Dynamic Clock Gating is Disabled 1 = SATA Port 3 Dynamic Clock Gating is Enabled ***Note:*** This bit may be Reserved depending on if port is available in the given SKU. See Section 1.3 for details if port is available.
26	**SATA Port 2 Dynamic Clock Gate Enable** — R/W. 0 = SATA Port 2 Dynamic Clock Gating is Disabled 1 = SATA Port 2 Dynamic Clock Gating is Enabled ***Note:*** This bit may be Reserved depending on if port is available in the given SKU. See Section 1.3 for details if port is available.

21. Remove note 11 on Table 3-3

~~11. PMSYNCH is low in C6/C7 states only~~

22. Remove VccpNAND on Table 8-3 and Table 8-4

Table 8-3 Measured I_{CC} (Desktop Only)

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
~~VccpNAND~~	~~1.8~~	~~.0055~~	~~.0055~~	~~.0022~~	~~.0022~~	~~0~~	~~0~~	—

Table 8-4 Measured I_{CC} (Mobile Only)

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
~~VccpNAND~~	~~1.8~~	~~.0055~~	~~.0055~~	~~.0022~~	~~.0022~~			—

23. Section 8.2 Updates

The title of section 8.2 is changed as below.

8.2 Absolute Maximum and Minimum Ratings

The following paragraphs are added to section 8.2:

Table 8-2 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the PCH/ICHx contains protective circuitry to resist damage from Electro - Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

24. TEMP_ALERT# Muxing

TEMP_ALERT# functionality is muxed on SATA5GP/GPIO49. Figure 2-1, table 2-5, table 3-4, table 3-5, table 6-61 and table 6-62, SATA5GP/GPIO49 are updated to show SATA5GP/GPIO49/TEMP_ALERT#.

25. Causes of Host and Global Resets Update

PROCPWRGD-to CPURST# Violation is removed from table 5-35.

26. GPIO18 Toggling Note

Note 7 of table 2-25 is modified as shown:

7. GPIO18 will toggle at a frequency of approximately 1 Hz when the signal is programmed as a GPIO (when configured as an output) by BIOS.

27. Pre-fetch Based Pause Bit Definition

The Pre-fetch Based Pause control bit is redefined as Pre-fetch Based Pause Enable with the following description:

Bit	Description
4	**Pre-fetch Based Pause Enable** — R/W. 0 = Pre-fetch Based Pause is disabled. 1 = Pre-fetch Based Pause is enabled.

28. Register Corrections

a. Bit 2 of section 22.1.3 CMD—Command (D31:F6) is changed as shown:

Bit	Description
2	**BME (Bus Master Enable)** — R/W. 0 = Function disabled as bus master. 1 = Function enabled as bus master.

b. Section 22.2.12 PTA—PCH Temperature Adjust (TBARB+14h) is changed as shown:

Bit	Description
15:8	**PCH Slope** — R/W. This field contains the PCH slope for calculating PCH temperature. The bits are locked by AE.bit7 (offset 3Fh). **NOTE:** When thermal reporting is enabled, BIOS must write 80h into this field.
7:0	**Offset**— R/W. This field contains the PCH offset for calculating PCH temperature. The bits are locked by AE.bit7 (offset 3Fh). **NOTE:** When thermal reporting is enabled, BIOS must write 8Ch into this field.

29. Display BDF Register Additions

Bit 0 of section 10.1.66 FD2—Function Disable 2 (RCBA+3428h) is changed as shown (Reserved bits are also corrected to show bits 31:5 instead of 31:0):

Bit	Description
31:5	Reserved

30. Miscellaneous Typographical Error Corrections III

a. TRST# is removed from tables 3-4 and 3-5.

b. SATAGP[5:0] is corrected to SATA[5:0]GP in table 8-5.

c. Port numbers are corrected in section 10.1.15 RPFN—Root Port Function Number and Hide for PCI Express* Root Ports (RCBA+0404h) as shown:

Bit	Description
30:28	**Root Port 8 Function Number (RP8FN)** — R/WO. These bits set the function number for PCI Express Root Port 8. This root port function number must be a unique value from the other root port function numbers
26:24	**Root Port 7 Function Number (RP7FN)** — R/WO. These bits set the function number for PCI Express Root Port 7. This root port function number must be a unique value from the other root port function numbers

d. Occurrences of SMBASE are changed to SMB_BASE throughout the document.

e. In section 5.14.1.2, “TCO_STS” is changed to “TCO2_STS”.

f. In section 13.9.3, “TCO_STS” is changed to “TCO1_STS”.

g. Occurrences of PCH_PWROK are corrected to PWROK.

h. Occurrences of “e-SATA” are corrected to eSATA.