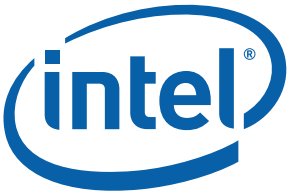

Intel® 6 Series Chipset and Intel® C200 Series Chipset

Specification Update

May 2011

Notice: Intel® 6 Series Chipset and Intel® C200 Series Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 324646-006

Contents

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Revision History

Revision	Description	Date
001	• Initial Release	January 2011
002	• Updated Top Markings • Updated for B3 Rev ID • Added Errata # 14: SATA Ports 2-5 Issue	February 2011
003	• Updated Top Markings • Updated PCH Device and Revision Identification	February 2011
004	• Added Intel® Q65 Chipset to Top Markings and PCH Device and Revision Identification • Added Specification Change #1: Intel Q65 SKU Addition	April 2011
005	• Added Intel® C200 Series Chipet to Top Markings, PCH Device and Revision Identification, and Errata.	April 2011
006	• Added Intel® Z68 Chipet to Top Markings and PCH Device and Revision Identification.	May 2011

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 6 Series Chipset and Intel® C200 Series Chipset Datasheet	324645-004

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the PCH product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
1	X	X	No Fix	USB Isoch In Transfer Error Issue
2	X	X	No Fix	USB Full-Speed / Low-Speed Device Removal Issue
3	X	X	No Fix	USB Babble Detected with SW Overscheduling
4	X	X	No Fix	USB Low-Speed/Full-Speed EOP Issue
5	X	X	No Fix	USB PLL Control FSM Not Getting Reset on Global Reset
6	X	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
7	X	X	No Fix	USB FS/LS Incorrect Number of Retries
8	X	X	No Fix	Incorrect Data for LS or FS USB Periodic IN Transaction
9	X	X	No Fix	HDMI 222 MHz Electrical Compliance Testing Failures
10	X	X	No Fix	SATA Signal Voltage Level Violation
11	X	X	No Fix	SATA Differential Return Loss Violations
12	X	X	No Fix	USB V_{HSOH} Maximum Violation
13	X	X	No Fix	Delayed Periodic Traffic Timeout Issue
14	X		Fixed	SATA Ports 2-5 Issue

Specification Changes

Spec Change Number	Stepping		SPECIFICATION CHANGES
	B2	B3	
			There are no specification changes in this revision of the specificaiton update.

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
		There are no specification clarifications in this revision of the specificaiton update.

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
		There are no documentation changes in this revision of the specificaiton update.

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Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	Notes
B2	SLH82	BD82H67	Intel® H67 Chipset
B2	SLH84	BD82P67	Intel® P67 Chipset
B2	SLH9C	BD82HM67	Intel® HM67 Chipset
B2	SLH9D	BD82HM65	Intel® HM65 Chipset
B3	SLJ4D	BD82Q67	Intel® Q67 Chipset
B3	SLJ4E	BD82Q65	Intel® Q65 Chipset
B3	SLJ4A	BD82B65	Intel® B65 Chipset
B3	SLJ4F	BD82Z68	Intel® Z68 Chipset
B3	SLJ49	BD82H67	Intel® H67 Chipset
B3	SLJ4C	BD82P67	Intel® P67 Chipset
B3	SLJ4B	BD82H61	Intel® H61 Chipset
B3	SLJ4J	BD82C202	Intel® C202 Chipset
B3	SLJ4H	BD82C204	Intel® C204 Chipset
B3	SLJ4G	BD82C206	Intel® C206 Chipset
B3	SLJ4M	BD82QM67	Intel® QM67 Chipset
B3	SLJ4L	BD82UM67	Intel® UM67Chipset
B3	SLJ4N	BD82HM67	Intel® HM67 Chipset
B3	SLJ4P	BD82HM65	Intel® HM65 Chipset
B3	SLJ4K	BD82QS67	Intel® QS67 Chipset

PCH Device and Revision Identification

The Revision ID (RID) is an 8-bit register located at the offset 08h in the PCI header of every PCI device and function. The assigned value is based on the product's stepping.

PCH Device and Revision ID Table (Sheet 1 of 3)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D31:F0	LPC	1C4Eh		05h	Intel® Q67 Chipset
		1C4Ch		05h	Intel® Q65 Chipset
		1C50h		05h	Intel® B65 Chipset
		1C4Ah	04h	05h	Intel® H67 Chipset
		1C44h		05h	Intel® Z68 Chipset
		1C46h	04h	05h	Intel® P67 Chipset
		1C5Ch		05h	Intel® H61 Chipset
		1C52h		05h	Intel® C202 Chipset
		1C54h		05h	Intel® C204 Chipset
		1C56h		05h	Intel® C206 Chipset
		1C4Fh		05h	Intel® QM67 Chipset
		1C47h		05h	Intel® UM67Chipset
		1C4Bh	04h	05h	Intel® HM67 Chipset
		1C49h	04h	05h	Intel® HM65 Chipset
		1C4Dh		05h	Intel® QS67 Chipset
D31:F2	SATA[1]	1C00h	04h	05h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0-3)
		1C02h	04h	05h	Desktop: AHCI (Ports 0-5)
		2822h[2]	04h	05h	Desktop (all RAID-capable SKUs): RAID 0/1/5/10 (Ports 0-5) (AIE bit = 0)
		1C04h[2]	04h	05h	Desktop (all RAID-capable SKUs): RAID 0/1/5/10 (Ports 0-5) (AIE bit = 1)
		1C01h	04h	05h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0-3)
		1C03h	04h	05h	Mobile: AHCI (Ports 0-5)
		282Ah[2]	04h	05h	Mobile: RAID 0/1/5/10 (Ports 0-5) (AIE bit = 0)
		1C05h[2]	04h	05h	Mobile: RAID 0/1/5/10 (Ports 0-5) (AIE bit = 1)
D31:F5	SATA[1,3]	1C08h	04h	05h	Desktop: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
		1C09h	04h	05h	Mobile: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	1C22h	04h	05h	

PCH Device and Revision ID Table (Sheet 2 of 3)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D31:F6	Thermal	1C24h	04h	05h	
D30:F0	DMI to PCI Bridge	1C25h	04h	05h	Desktop (When D30:F0:4Ch:bit 29 = 1)
		244Eh	A4h	A5h	Desktop (When D30:F0:4Ch:bit 29 = 0)
		1C25h	04h	05h	Mobile (When D30:F0:4Ch:bit 29 = 1)
		2448h	A4h	A5h	Mobile (When D30:F0:4Ch:bit 29 = 0)
D29:F0	USB EHCI #1	1C26h	04h	05h	
D26:F0	USB EHCI #2	1C2Dh	04h	05h	
D27:F0	Intel® High Definition Audio	1C20h	04h	05h	
D28:F0	PCI Express* Port 1	1C10h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1= 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F1	PCI Express Port 2	1C12h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F2	PCI Express Port 3	1C14h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F3	PCI Express Port 4	1C16h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F4	PCI Express Port 5	1C18h	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)

PCH Device and Revision ID Table (Sheet 3 of 3)

Device Function	Description	Dev ID	B2 Rev ID	B3 Rev ID	Comments
D28:F5	PCI Express Port 6	1C1Ah	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F6	PCI Express Port 7	1C1Ch	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D28:F7	PCI Express Port 8	1C1Eh	B4h	B5h	Desktop and Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 0)
		244Eh	B4h	B5h	Desktop (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
		2448h	B4h	B5h	Mobile (When D28:F0/F1/F2/F3/F4/F5/ F6/F7:ECh:bit 1 = 1)
D25:F0	LAN	1C33h[4]	04h	05h	
D22:F0	Intel® ME Interface #1	1C3Ah	04h	05h	
D22:F1	Intel ME Interface #2	1C3Bh	04h	05h	
D22:F2	IDE-R	1C3Ch	04h	05h	
D22:F3	KT	1C3Dh	04h	05h	

NOTES:

1. PCH contains two SATA controllers. The SATA Device ID is dependent upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. The SATA RAID Controller Device ID is dependent upon the AIE bit setting (bit 7 of D31:F2:Offset 9Ch).
3. SATA Controller 2 (D31:F5) is only visible when D31:F2 CC.SCC =01h
4. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 1C33h is used. Refer to the appropriate Intel® GbE physical layer Transceiver (PHY) datasheet for LAN Device IDs.
5. This table shows the default PCI Express Function Number-to-Root Port mapping. Function numbers for a given root port are assignable through the “Root Port Function Number and Hide for PCI Express Root Ports” register (RCBA+0404h).

Errata

1. USB Isoch In Transfer Error Issue

Problem: If a USB Full-Speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a micro-frame the PCH may see more than 189 bytes in the next micro-frame.

Implication: If the PCH sees more than 189 bytes for a micro-frame an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a micro-frame. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the micro-frame.

Workaround: None.

Status: No Plan to Fix.

2. USB Full-Speed / Low-Speed Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: No Plan to Fix.

3. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for Full-Speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: No Plan to Fix.

4. USB Low-Speed/Full-Speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending Low-Speed or Full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending Low-Speed or Full-Speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device entered suspend and may starting sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress

Workaround: None.

Status: No Plan to Fix.

5. USB PLL Control FSM not Getting Reset on Global Reset

Problem: Intel® 6 Series Chipset and Intel® C200 Series Chipset USB PLL may not lock if a Global Reset occurs early during a cold boot sequence.

Implication: USB interface would not be functional an additional cold boot would be necessary to recover.

Workaround: None.

Status: No Plan to Fix.

6. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes Full-Speed and Low-Speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: No Plan to Fix.

7. USB FS/LS Incorrect Number of Retries

Problem: A USB Low-Speed Transaction may be retried more than three times, and a USB Full-Speed transaction may be retried less than three times if all of the following conditions are met:

- A USB Low-Speed transaction with errors, or the first retry of the transaction occurs near the end of a micro-frame, and there is not enough time to complete another retry of the Low-Speed transaction in the same micro-frame
- There is pending USB Full-Speed traffic and there is enough time left in the micro-frame to complete one or more attempts of the Full-Speed transaction
- Both the Low-Speed and Full-Speed transactions must be asynchronous (Bulk/Control) and must have the same direction either in or out

Note: Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of 3 times if it continues to fail.

Implication:

- For Low-Speed transactions the extra retry(s) allow a transaction additional chance(s) to recover regardless of if the Full-Speed transaction has errors or not.
- If the Full-Speed transactions also have errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: None.

Status: No Plan to Fix.

8. Incorrect Data for LS or FS USB Periodic IN Transaction

Problem: The Periodic Frame list entry in DRAM for a USB LS or FS Periodic IN transaction may incorrectly get some of its data from a prior Periodic IN transaction which was initiated very late into the preceding Micro-frame.

It is considered good practice for software to schedule Periodic Transactions at the start of a Micro-frame. However Periodic transactions may occur late into a Micro-frame due to the following cases outlined below:

- Asynchronous transaction starting near the end of the proceeding Micro-frame gets Asynchronously retried

Note: Transactions getting Asynchronous retried would only occur for ill behaved USB device or USB port with a signal integrity issue

- Or Two Periodic transactions are scheduled by software to occur in the same Micro-frame and the first needs to push the second Periodic IN transaction to the end of the Micro-frame boundary

Implication: The implication will be device, driver or operating system specific.

Note: This issue has only been observed in a synthetic test environment

Workaround: None.

Status: No Plan to Fix.

9. HDMI 222 MHz Electrical Compliance Testing Failures

Problem: HDMI 222 MHz electrical compliance testing may show eye diagram and jitter test failures on Intel 6 Series Chipsets and Intel C200 Series Chipset.

Implication: No functional or visual failures have been observed by Intel. HDMI electrical compliance failures may be seen at 222 MHz Deep Color Mode. This issue does not prevent HDMI with Deep Color Logo certification as no failures have been seen with 74.25 MHz Deep Color Mode (720P 60 Hz or 1080P 30 Hz) as required HDMI Compliance Test Specification.

Workaround: None.

Status: No Plan to Fix.

10. SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.1 of the Serial ATA specification, rev 3.0. This issue applies to Gen 1 (1.5 Gb/s) and Gen 2 (3.0 Gb/s).

Implication: None known.

Workaround: None.

Status: No Plan to Fix.

11. SATA Differential Return Loss Violations

Problem: The Intel 6 Series Chipset and Intel C200 Series Chipset SATA buffer capacitance may be higher than expected.

Implication: There are no known functional failures. This may cause a violation of the SATA-IO compliance test for Receiver or Transmitter Differential Return Loss.

Workaround: None.

Note: Intel has obtained a waiver for the SATA-IO building block status.

Status: No Plan to Fix.

12. USB V_{HSOH} Maximum Violation

Problem: Intel 6 Series Chipset and Intel C200 Series Chipset High-Speed USB 2.0 V_{HSOH} may exceed the USB 2.0 specification.

- The maximum expected V_{HSOH} is 440 mV.

Implication: There are no known functional failures.

Note: USB-IF does not require testing of V_{HSOH} for USB Logo Certification.

Workaround: None.

Status: No Plan to Fix.

13. Delayed Periodic Traffic Timeout Issue

Problem: If a periodic interrupt transaction is pushed out to the x+4 micro-frame boundary, the RMH may not wait for the transaction to timeout before starting the next transaction.

Implication: If the next Full-Speed or Low-Speed transaction is intended for the same device targeted by the periodic interrupt, the successful completion of that transaction is device dependent and cannot be guaranteed. The implication may differ depending on the nature of the transaction:

- If the transaction is asynchronous and the device does not respond, it will eventually be retried with no impact.
- If the transaction is periodic and the device does not respond, the transfer may be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment.

Workaround: None.

Status: No Plan to Fix.

14. SATA Ports 2-5 Issue

Problem: Due to a circuit design issue on Intel 6 Series Chipset and Intel C200 Series Chipset, electrical lifetime wear out may affect clock distribution for SATA ports 2-5. This may manifest itself as a functional issue on SATA ports 2-5 over time.

- The electrical lifetime wear out may result in device oxide degradation which over time can cause drain to gate leakage current.
- This issue has time, temperature and voltage sensitivities.

Implication: The increased leakage current may result in an unstable clock and potentially functional issues on SATA ports 2-5 in the form of receive errors, transmit errors, and unrecognized drives.

- Data saved or stored prior to functional issues on a SATA device will be retrievable if connected to a working SATA port.

- SATA ports 0-1 are not affected by this design issue as they have separate clock generation circuitry.

Workaround: Intel has worked with board and system manufacturers to identify and implement solutions for affected systems.

- Use only SATA ports 0-1.
- Use an add-in PCIe SATA bridge solution.

Status: Closed.

- This issue has been resolved with a silicon stepping for all Intel 6 Series Chipsets and and Intel C200 Series Chipsets incorporating a minor metal layer change.
- The fix does not impact the designed functionality and electrical specifications of the Intel 6 Series Chipset and Intel C200 Series Chipset.

Specification Changes

There are no specificaiton changes in this revision of the specification update.

Specification Clarification

There are no specification clarifications in this revision of the specification update.

Documentation Changes

There are no documentation changes in this revision of the specification update.