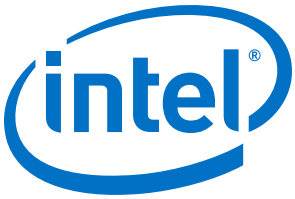
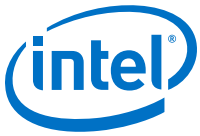


Intel® Xeon® Processor E3-1125C with Intel® Communications Chipset 8910 Development Kit

User Guide

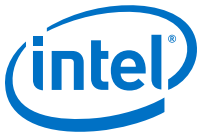
October 2012

Order No.: 328009-001US



Contents

Figures

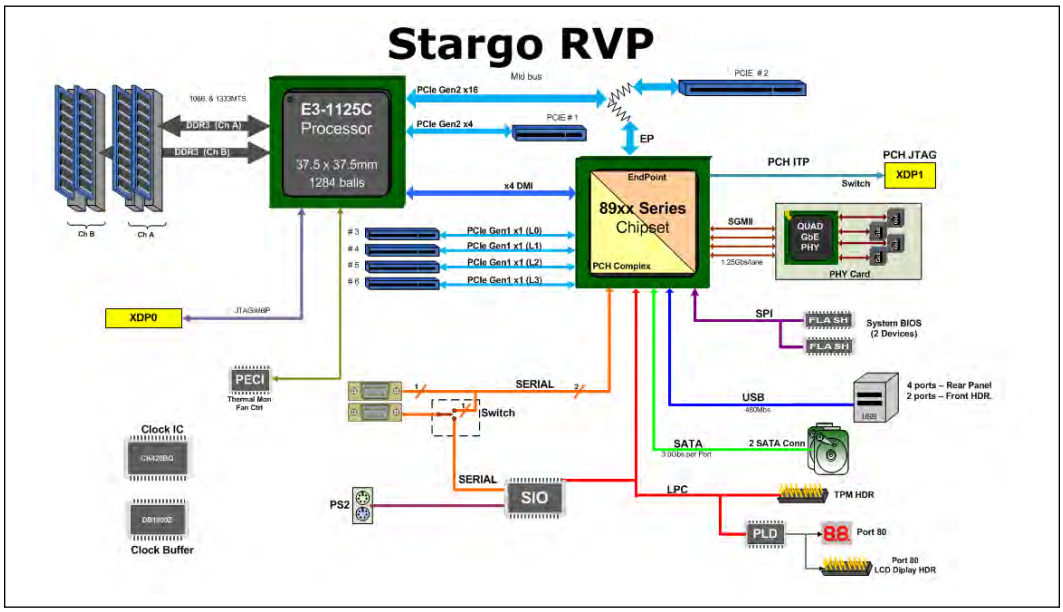


Tables

1.0 Introduction

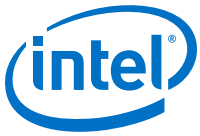
The Intel® Xeon® Processor E3-1125C with Intel® Communications Chipset 8910 Development Kit (CRB) hardware design is based on the Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure connected to the Intel® Communications Chipset 89xx Series. The CRB design supports one Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure using a device down topology . The processor supports up to two DDR3 channels and up to 20 PCI Express* Gen 2 lanes, as shown below.

Figure 1. Reference Board Overview



Unless otherwise stated references to the "CRB" or "customer reference board" refer to the Intel® Xeon® Processor E3-1125C with Intel® Communications Chipset 8910 Development Kit. Unless otherwise stated references to the “processor” and "CPU" throughout this document refer to the Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure. Unless otherwise stated references to the “chipset,” “Platform Controller Hub,” or “PCH” refer to the Intel® Communications Chipset 89xx Series.

The CRB schematics are the primary source for details about the CRB. This user guide is a supplement to the schematics. Component reference designators in this user's guide are based on the CRB schematics and are defined by their type and board-mapped location. They end with a numerical index. The board-mapped locations are sectioned on a grid pattern: 1 through 9 horizontally, and A through K vertically. The bottom side of the board has a similar grid pattern but with different call-outs. See the grid call-outs along the edges of the board. U6D1, for example, is an IC (U), is on the top of the board at cross section 6D, and is the first indexed component (1) of that type in that area.



1.1 Warnings and Cautions

Caution: Ensure a safe and static-free work environment before removing any components from their anti-static packaging. The CRB is susceptible to electrostatic discharge, which may cause failure or unpredictable operation.

Caution: Connecting the wrong cable or reversing a cable may damage the board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to the board.

Caution: The power supply cord is the main disconnect device to the main power (AC power). The socket outlet should be installed near the equipment and should be readily accessible. To avoid shock, ensure that the power cord is connected to a properly wired and grounded receptacle. Do not connect/disconnect any cables or perform installation/maintenance of the boards during an electrical storm. Ensure that any equipment to which this CRB will be attached is also connected to properly wired and grounded receptacles.

Ensure that setting up the power supply is the final step performed in the process of assembly.

Once the board is set up, plug the power cable into the back of the power supply, leaving the switch in the OFF position, then plug the cord into the power source and switch on the power supply.

Caution: Items marked as "Reserved" in this users guide and in the CRB schematics are not supported. Changing settings related to these items could lead to unknown behavior on the CRB.

1.2 Kit Contents

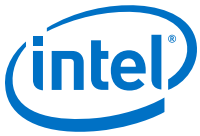
Feature	Description
CRB board	PCB assembled with a BGA device down for the Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure and device down for Intel® Communications Chipset 89xx Series with a passive heatsink.
Processor	Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure
Processor heatsink	Active heatsink
Chipset	Intel® Communications Chipset 8910
Memory	Two Micron 1-GB DDR3, UDIMMs (ECC) (different DIMM type may be provided)
SPI flash	Two-socketed SPI flash (4 MB each) for BIOS, PCH ME Ignition FW, and platform data
Power supply	625 W ATX power supply
Video card	x1 PCIe* graphics card
Hard drive	Western Digital 3.5 inch-solid state drive: 160 GB SATA II
Disk drive	LITE ON DVD-RW/CD-RW SATA disk
	continued...

Feature	Description
GbE PHY plug-in cards	• Intel® Ethernet Server Adapter X520-T2, Dual-port 10G Bast T NIC • Intel® Ethernet Server Adapter X520-SR2, Dual-port SFP+ SR Optics
Stand	Acrylic stand for board plus pads
Additional peripherals	8 x Standoffs and 16 x screws

1.3 Features Summary

Feature	Description
Form factor	12-layer custom ATX (~12 x ~12 inches) board
Processor	Supports Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure.
Bus speed	Intel® DMI2 2.5GT/s: • Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure: Gen2 protocol at Gen2 speed. • Intel® Communications Chipset 89xx Series: Gen2 protocol at Gen1 speed.
Processor VR	IMVP 7.0
Memory	Total of four DIMM connectors: • Up to two channels per processor • Up to two DIMMs / channel • Supports 1066/1333 MHz DDR3 Unregistered 240-pin DIMMs. • Up to 32 GB of system memory • Support for single-rank and dual-rank DIMMs • Support for 1 Gb, 2 Gb, and 4 Gb technologies/densities
PCI Express	Total of six slots: • One x16 slot connected to processor Intel® Communications Chipset 89xx Series Endpoint) • One x8 slot on processor (4 active lanes) • Four x8 slots from PCH (2.5 GT/s Max) (1 active lane in each) *Note: PCI Express* Base Specification, Rev. 1.0a*
PCI Express hot-plug	Not supported.
Chipset	BGA soldered down Intel® Communications Chipset 89xx Series
Serial ATA	Two SATA-II ports with AHCI support *Note:* Windows XP should be booted in IDE mode only
USB*	Total of six connections (USB 2.0 ports (RMH/EHCI configuration): • 4x USB ports on rear panel • 2x USB connector ports (10 pin header)
Video	PCI Express* video controller. Connected to PCH PCI Express x1 controller
LAN support	PHY Card plug in cards over HMZD connection: One Acre Quad PHY Module (I347)
LPC	Low Pin Count (LPC) Bus I/O Controller: One (TPM) header
Other I/Os	PS/2* keyboard and mouse ports Two Serial ports (One dedicated to PCH, second is shared between PCH and SIO)

continued...



Feature	Description
Clocking	CK420 for delivery of differential clocks to Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure and Intel® Communications Chipset 89xx Series DB1900 clock buffer for additional 100-MHz differential clocks
BIOS	Two 16-pin SOIC SPI Socket for Flash support. Populated with 4-MB devices (one device for BIOS and the other for ME FW, GbE etc.) Support for Advanced Configuration and Power Interface (ACPI), plug-and-play, SMBIOS
Hardware subsystem	Supports S0, S3, S4, and S5 sleep states. Fan support: • CPU fan connector (full speed only) • PCH fan connector (full speed only) Debug: • ITP-XDP0 connector for CPU • ITP-XDP1 connector for PCH

1.4 Related Documents

Always use the latest versions as references for the CRB. Contact your field representative for publication access.

Document	URL (Document Number)
Intel® Xeon® and Intel® Core™ Processors For Communications Infrastructure Datasheet	327405
Intel® Communications Chipset 89xx Series Datasheet	327879
Intel® Communications Chipset 89xx Series Specification Update	328000
Intel® Xeon® and Intel® Core™ Processors For Communications Infrastructure Thermal/Mechanical Design Guide	327397
Intel® Communications Chipset 89xx Series Thermal/Mechanical Design Guide	328012
JEDEC Memory Specification	http://www.jedec.org
PCI Express* Base Specification, Rev. 2.0	http://www.pcisig.com/specifications/
PCI Express* Base Specification, Revision 1.1	http://www.pcisig.com/specifications/
PCI Express* Card Electromechanical Specification, Revision 1.1	http://www.pcisig.com/specifications/
PCI Local Bus Specification, Rev. 2.3	http://www.pcisig.com/specifications/
PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.1	http://www.pcisig.com/specifications/
PCI Power Management Specification, Revision 1.1	http://www.pcisig.com/specifications/
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
Low Pin Count Interface Specification, Revision 1.1 (LPC)	Contact your Intel representative for the latest version of this item.
Universal Serial Bus Revision 2.0 Specification (USB)	http://www.usb.org

continued...

Document	URL (Document Number)
Advanced Configuration and Power Interface, Version 2.0 (ACPI)	http://www.acpi.info/spec.htm
Universal Host Controller Interface, revision 1.1 (UHCI)	Contact your Intel representative for the latest version of this item.
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	Contact your Intel representative for the latest version of this item.
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
Serial ATA II: Extensions to Serial ATA 1.0, Revision 1.0a	http://www.serialata.org
IEEE 802.3 Fast Ethernet	http://standards.ieee.org
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
IA-PC HPET (High Precision Event Timers) Specification, Revision 0.98a	Contact your Intel representative for the latest version of this item.
Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test	Intel appnote AP-728
Front Panel I/O Connectivity Design Guide	http://www.formfactors.org/DeveloperResources.asp
SSI Specification	http://ssiforum.org/specifications.aspx
ATX Specification Rev 2.02	http://www.formfactors.org/formfactor.asp
Socket B Design Guidelines	Contact your Intel representative for the latest version of this item.

1.5 Processors and Chipset

The CRB is designed to support the following processor and chipset. Use only the processor and chipset in the table. The use of unsupported components can damage the CRB board, the processor, and the power supply.

In this document, "processor" and "CPU" refers to the processor in the following table.

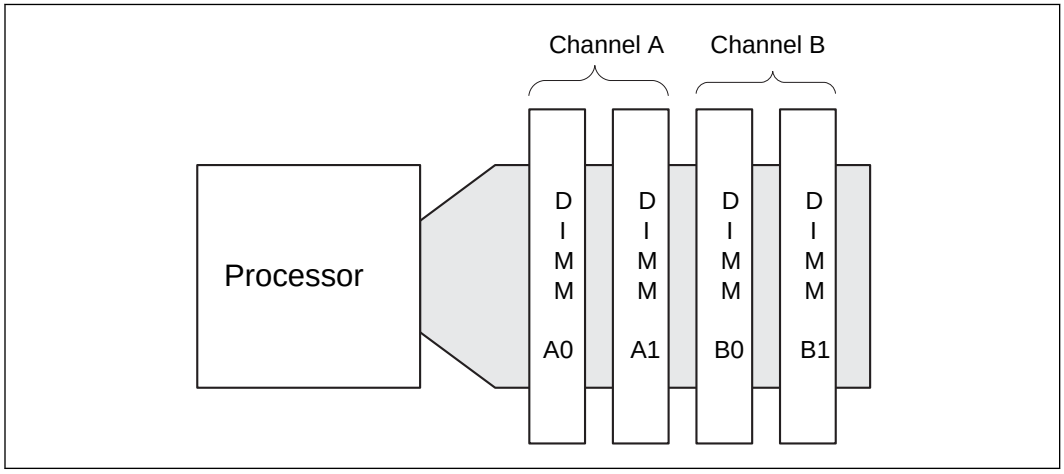
Table 1. Supported Processor and Chipset

Ref Des Location	Description	
U6G1	CPU / processor	Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure
U2G1	Chipset	Intel® Communications Chipset 8910

1.6 Memory Sub-System

The CRB supports a DDR3-based memory subsystem that includes support for up to two channels per processor and two DIMMs per channel (2 DIMM/CH). See the following figure.

Figure 2. CRB 2 DIMM/CH DDR3 Topology



1.6.1 Supported Memory

The CRB supports DDR3-1066 and DDR3-1333 memory technologies.

The processor has a two-channel memory interface. Each channel consists of 64 data and 8 ECC bits. The CRB supports unbuffered ECC/non-ECC DDDR3 DIMMs.

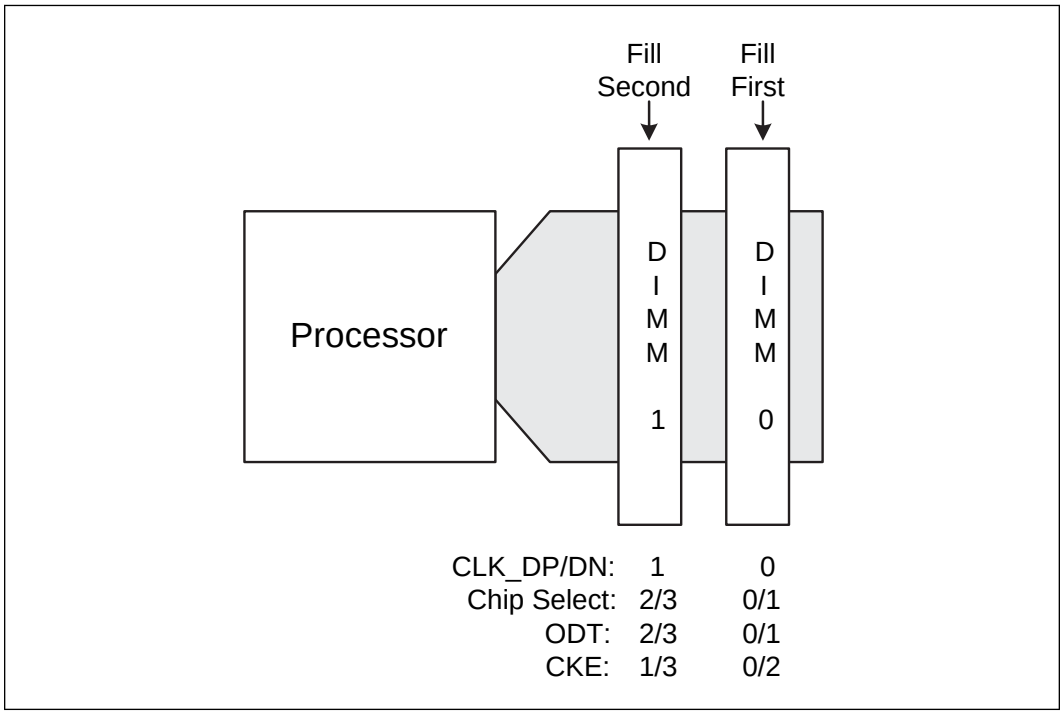
1.6.1.1 Population Requirements

- All DIMMs must be DDR3 Unbuffered DIMMs.
- Unbuffered DIMMs can be ECC or non-ECC.
- Mixing of ECC and non-ECC DIMMs is not allowed.
- A maximum of 4 logical ranks per channel is allowed.
- DIMMs with different timing parameters can be installed on different slots within the same channel, but only timings that support the slowest DIMM will be applied to all. As a consequence, faster DIMMs will be operated at timings supported by the slowest DIMM populated. The same interface frequency (DDR3-1066 or DDR3-1333) will be applied to all DIMMs on all channels on the platform.
- When single and dual rank DIMMs are populated for 2DPC, always populate the higher number rank DIMM first (starting from the farthest slot), for example, first dual rank and last single rank.

1.6.1.2 DIMM Population for Two Slots per Channel

For two slot per channel configurations, the CRB requires DIMMs within a channel to be populated starting with the DIMMs farthest from the processor in a “fill-farthest” approach.

Figure 3. DIMM Population Within a Channel for Two Slots per Channel



All allowed DIMM population configurations for two slots per channel are shown in the following table.

Table 2. UDIMM Population Configurations Within a Channel for Two Slots per Channel

Configuration Number	POR Speed	1N or 2N	DIMM0	DIMM1
1	DDR3-1333 & 1066	1N	Empty	Single-rank
2	DDR3-1333 & 1066	1N	Empty	Dual-rank
3	DDR3-1333 & 1066	2N	Single-rank	Single-rank
4	DDR3-1333 & 1066	2N	Single-rank	Dual-rank
5	DDR3-1333 & 1066	2N	Dual-rank	Dual-rank

1.7 Thermal and Mechanical Components

Table 3. Thermal and Mechanical Components

Name	Description
Standard Processor Thermal Solution Mounting	The CRB supports full power processor thermal solution mounting provisions as delineated in the processor's Thermal/Mechanical Design Guidelines.
Processor Fan	The CRB provides fan headers for the processors that includes 12V.
Heatsink	The CRB supports heatsink mounting requirements.

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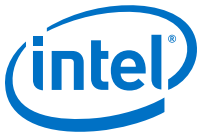

Name	Description
Active Heatsink	The CRB provides mounting provisions and a fan header for an active thermal solution.
Fan Headers	The CRB provides one fan header.
Solder Down Anchors	The CRB provides solder down anchors for the CRB and chipset. This includes active heatsink mounting holes.

Heatsinks

The processor and CRB use an active heatsink design with a built-in fan, and the PCH uses a passive heatsink. The active heatsink is powered by the platform. For details on the processor and PCH heatsink, see the Thermal/Mechanical Design Guidelines. The passive heatsink for the Intel® Communications Chipset 89xx Series requires no power.

Physical and Mechanical Board Specifications

The CRB is approximately 12 inches long by 12 inches wide. It provides non-plated mounting holes with top and bottom ground rings and requires users to use the acrylic stand provided to avoid shorts.

1.8 Real Time Clock (RTC), CMOS SRAM, and Battery

A coin-cell battery (B1B1 type CR2032) powers the real-time clock (RTC) and CMOS memory. The battery has an estimated life of three years when it is not plugged into a wall socket. When the platform is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSTBY applied.

If the battery and AC power fail, then at boot-up the system will prompt you to either load optimized defaults or enter the BIOS and manually adjust the BIOS settings.

1.9 On-Board Peripheral Components

Table 4. On-Board Peripheral Components

Ref Des Location	Description	
U5F1/U3E1	Clock Generator / Clock Buffer	CK420 Clock Generator/ DB1900 Clock Buffer
U3A2	SuperI/O*	The SIO (WPCD376I) is driven by the PCH Low Pin Count (LPC) bus.
U2K1/U2K2	SPI Flash	16 MB socket with footprint for 8-pin devices (primary boot, Intel® Communications Chipset 89xx Series FW storage, BIOS etc.)
S6A1	Power Button	System power button
S7A1	Reset Button	System reset button
U1K1	Port 80 Logic Device	Altera* EPM570_100P
DS2K1/DS2K2	Port 80 Code Display	Two digit, 7-segment LED character displays

continued...

Ref Des Location	Description	
B1B1	Battery	3 V Lithium CR2032 coin battery for real time clock (RTC) and CMOS memory backup
U9A1	RS232 Transceiver	Two 28-pin connectors to handle all modem control signals
U9A2		

1.10 On-Board I/O Connectors

Table 5. On-Board I/O Connectors

Ref Des Location	Description	
J1D1, J1D2	PHY Card Connector	HMZD connector for PHY add-in card
J1G1	Serial ATA Port 0	Two SATA 2 interface connectors. SATA ports 4 and 5 are referenced as SATA ports 0 and 1 respectively.
J1F6	Serial ATA Port 1	
J1E3	USB Port 4 and 5 Header	10-pin (pin 9 is omitted as a plug-in key), dual-row header that routes two USB ports to an external USB connector. In conjunction with the rear panel USB ports there are a total of six USB ports.
J1A7	Front Panel Header	10-pin (pin 10 is omitted as a plug-in key), dual-row header that provides connection for: • Power Switch • Reset Switch • Power-on LED • HD Status LED
J8D1	CPU Fan Header	Four-wire CPU fan header.
J3J1	PCH Fan Header	Three-wire PCH fan header.
J5B3	AUX Fan Header	Three-wire header with no fan speed control.
J1H2	LPC Header	20-pin card header for the TPM / LPC bus.
J1J1	LCD Data	16-pin header, not populated, for LCD port 80 output
J2J2	PCH In-Circuit SPI Programming Header	10-pin header for use with DediProg* SF100 in-circuit program tool. Used to update PCH SPI device without removing it from its socket.
J5A1	XDP0 Connector CPU	Top-side 60-pin connector for ITP-XDP processor debug. XDP is the Extended Debug Port used for component debugging and testing.
J6D2	XDP1 Connector PCH	Top-side 60-pin connector for the ITP-XDP PCH debug. XDP is the Extended Debug Port used for component debugging and testing.

1.11 Expansion I/O Slots

Table 6. Expansion I/O Slots

Ref Des Location	Description		Notes
J5B1	PCI Express* Slot 1	Processor	The PCI Express ports comply with *PCI Express* Base Specification, Rev. 2.0a*.

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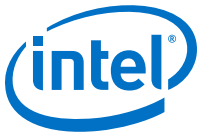

Ref Des Location	Description		Notes
J4B1	PCI Express Slot 2		
J4B2	PCI Express Slot 3	PCH Root Complex (2.5 GT/s Max)	The PCI Express Ports comply with *PCI Express* Base Specification, Rev. 1.0a*. All PCI Express slots (3, 4, 5, 6) employ physical x8 connectors regardless of whether they are x1, x4, or x8. This enables use of x8 cards even if the actual bandwidth and functionality is less.
J3B1	PCI Express Slot 4		
J2B2	PCI Express Slot 5		
J2B1	PCI Express Slot 6		
PCI Express Hot-Plug is not supported.			

1.12 PCH EndPoint PCIe Configuration

This section provides details on how to configure the PCIe for the supported Intel® Communications Chipset 89xx Series SKU.

Table 7. Intel® Communications Chipset 89xx Series SKUs

Intel® Communications Chipset 89xx Series SKU	PCIe Width
#3	x8

The PCH EndPoint can operate as a x4, x8, or x16 depending on the SKU and population of the headers below.

Table 8. Intel® Xeon® Processor E3-1125C PCIe Port0 Configuration

J6F6 CFG<6> Bit	J6E4 CFG<5> Bit	Intel® Xeon® Processor E3-1125C Port Bifurication
1	1	x16
1	0	x8 & x8
0	1	Reserved
0	0	x8, x4 & x4

The Intel® Communications Chipset 89xx Series EndPoint also supports lane reversal. Lane Reversal and Polarity Inversion must be done at a port level on the processor part (as outlined below).

Table 9. Intel® Xeon® Processor E3-1125C PCIe Lane Reversal

	Jumper
PCIe x16 - Lane Reversal	J6E5 - Closed
PCIe x16 - No Lane Reversal (Default)	J6E5 - Open
PCIe x4 - Lane Reversal	J6E6 - Closed
PCIe x4 - No Lane Reversal (Default)	J6E6 - Open

In addition to the above headers, additional headers affect the PCIe training at boot-up.

Table 10. Intel® Xeon® Processor E3-1125C with Intel® Communications Chipset 8910 Development Kit PCIe Configuration

Header	Description
J6E2	J6E2 must be Open for the PCH with BIOS V35 or later.
J3F2 Keep EP in Reset	Jumper must be Closed (inserted). Removing the jumper (Open) will keep EP in Reset (Low-true signal forced Low).

Figure 4. Intel® Xeon® Processor E3-1125C with Intel® Communications Chipset 8910 Development Kit PCIe Headers

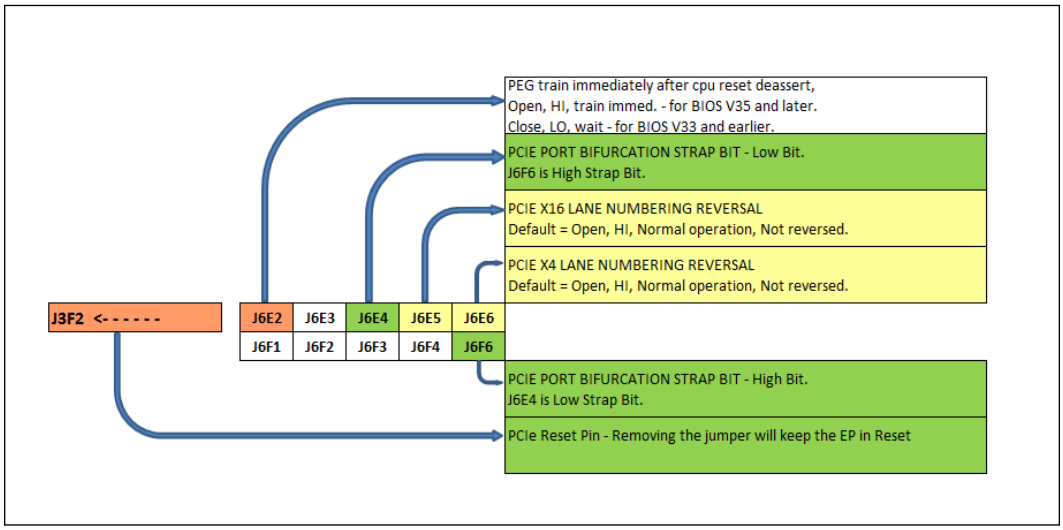

Table 11. Intel® Xeon® Processor E3-1125C with Intel® Communications Chipset 8910 Development Kit Default Header Configuration

SKU	J6F6	J6E4	J6E2	J3F2	J6E5	J6E6	Description
#1	Closed	Closed	Open	Closed	Closed	X	Bifur = X4 (0,0), Lane Reverse
#2	Closed	Closed	Open	Closed	Closed	X	Bifur = X4 (0,0), Lane Reverse
#3	Closed	Open	Open	Closed	Closed	X	Bifur = X8 & X8 (1,0), Lane Reverse
#4	Open	Open	Open	Closed	Closed	X	Bifur = X16 (1,1), Lane Reverse

1.13 Rear Panel I/O Connectors

Table 12. Rear Panel I/O Connectors

Ref Des Location	Description	
J8A1	USB Ports 0-3 Connector	The rear panel connector provides a quad-stacked USB 2.0 ports. Additionally, on board there is a header to allow connection to a front panel header. There are three USB modes: • RMH • UHCI • EHCI

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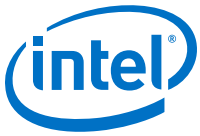


Ref Des Location	Description	
		See the *Intel® Communications Chipset 89xx Series Datasheet* for details on USB operating modes.
J9A2	PS/2 Keyboard and Mouse Connectors	The side panel provides two stacked circular DIN PS/2 connectors. Turn off power before a keyboard or mouse is connected or disconnected. • Keyboard connector on bottom (nearest board) • Mouse connector on top
J9A3	Serial COM Port Connector	The rear panel provides a dual-stack serial COM port. • RS232E 9-pin male D-sub dual port connector • Only outbound serial port traffic is available

1.14 On-Board Power Connectors

Table 13. On-Board Power Connectors

Ref Des Location	Description	
J4K4	SSI 24-pin power connector	Provides 12 V (+12V2), -12 V, 5 V, 3.3 V, 5 VSB voltages from the external power supply.
J5K2	SSI 8-pin power connector	Provides 12 V (+12V1) voltages from the external power supply that feed the CPU.
J9D1	SSI 8-pin power connector	Provides 12 V (+12V1) voltages from the external power supply that feed the DIMMs.

1.15 Watch Dog Timer (WDT)

The PCH has a safeguard watchdog timer to help prevent processor from thermal overload. During the power-up sequence, the PCH asserts CPUPWRGD. If the processor reset handshake is not completed within 10 ms of assertion, the PCH will power cycle the system to re-attempt the boot. It is critical to avoid having the processor powered and held in reset for an extended time.

The PCH watchdog timer will cause the CRB to power cycle if something does not allow the processor reset handshake to be completed with 10 ms of CPUPWRGD assertion.

1.16 Sleep States and Soft Off

ACPI 1.0, 2.0, 3.0 APM compliant.

- S0, S3, S4, and S5 sleep states
- Soft off capability (S5)
  - — Operating system dependent
  - — Requires a complete OS boot when the system wakes

1.17 Wake Events

- Power switch
- Wake on LAN (WoL) from GbE (PCH EndPoint/connector) or PCIe port

1.18 Fan Power Connections

- One processor fan connector
- One PCH fan connector
- One 3-wire auxiliary fan connector

1.19 On-Board Switches

The CRB has the following momentary push-button switches to provide state control:

- System power button (S6A1)
- System reset button (S7A1)

1.20 Supported Operating Systems

The CRB is validated with the following operating systems:

- Microsoft* Windows Embedded Standard 7 SP1 (32-bit and 64-bit)
- Windows Server 2008 R2 with SP1 (64-bit)
- FreeBSD* 8.2 (32-bit and 64-bit)
- Fedora* 16 (32-bitt and 64-bit)

Operating systems must be obtained by the customer. They are not distributed with the CRB kit.

1.21 BIOS Features

The BIOS has an AMI* core with the following components:

Table 14. Supported BIOS Features

BIOS Component	Description
PCI 2.3	The BIOS is compliant with the PCI Local Bus Specification, Rev. 2.3.
Serial ATA boot	The BIOS supports booting from a Serial ATA hard drive.
CD-ROM boot	The BIOS supports booting from a Serial ATA CD-ROM.
USB boot	The BIOS supports booting from a USB boot device.
Floppy boot	The BIOS supports booting from a floppy drive
PCI Express	The BIOS initializes and supports PCI Express cards that are plugged into the CRB.
USB	The BIOS supports the USB 1.1 and USB 2.0 interfaces.
CMOS Header	The BIOS supports recognizing the clear CMOS header.
ECC support	The BIOS detects and supports ECC memory.
Watchdog Timer (WDT)	The BIOS provides watch dog timer support.
APIC and ACPI Control	The ability to enable and disable APIC and ACPI is present in the BIOS. Control is also required for OS plug-and-play features. The BIOS supports the following ACPI states:

continued...

BIOS Component	Description
	• G0 (S0) - Working • G1 (S3) - Sleeping [Suspend to RAM] • G2 (S5) - Soft Off The BIOS supports C0, C1, C1E and C2 states.
Patch Update Mechanism	The Patch Update Mechanism is used to upgrade and/or install micro-code patches into BIOS is supported (BIOS Recovery Strap is located at J5A3 on the board).

1.22 ACPI

ACPI gives the OS direct control over the power management and plug-and-play functions of the platform. ACPI requires an OS that provides full ACPI support.

Under ACPI, the OS directs all system and device power state transitions by managing devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The OS uses information from applications and user settings to put the system as a whole into a low-power state.

Table 15. Effects of Pressing the Power Button

If the system is in this state...	...and the power switch is pressed for	...the system enters this state
Off (ACPI G2/G5 - soft off)	Less than four seconds	Power-on (ACPI G0 - working state)
On (ACPI G0 - working state)	Less than four seconds	Soft-off/Standby (ACPI G1 - sleeping state)
On (ACPI G0 - working state)	More than four seconds	Fail Safe Power-off (ACPI G2/G5 - soft off)
Sleep (ACPI G1 - sleeping state)	Less than four seconds	Wake-up (ACPI G0 - working state)
Sleep (ACPI G1 - sleeping state)	More than four seconds	Power-off (ACPI G2/G5 - soft off)

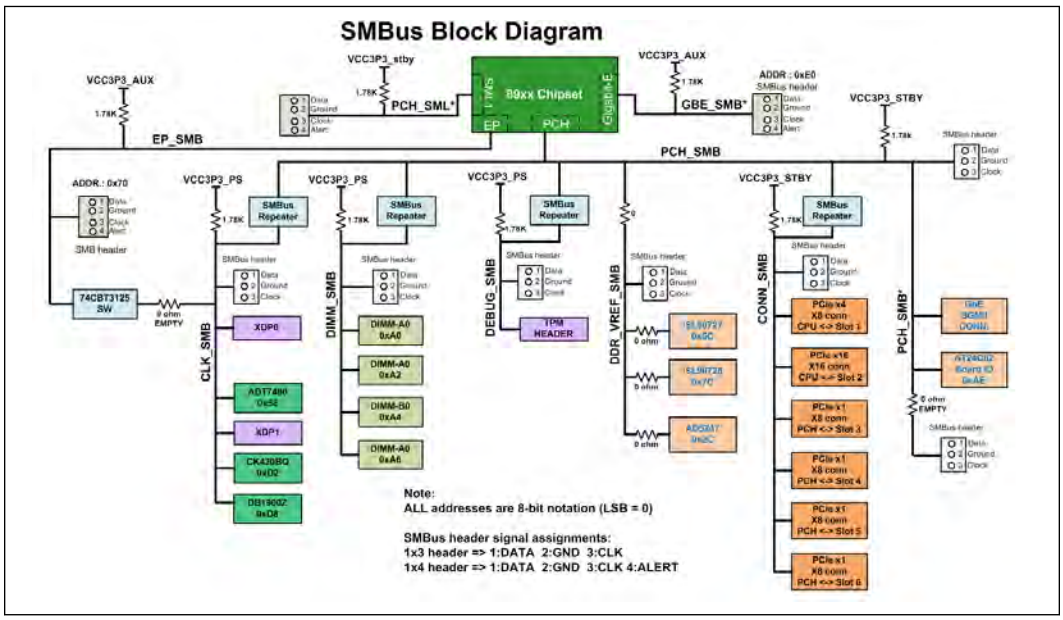
1.23 Debug Ports

The CRB provides an XDP for the processor (XDP0 - J5A1) and an XDP for the PCH (XDP1 - J6D2).

1.24 SMBus

The following figure provides a summary of the SMBus structure and address information supplemental to the CRB schematics.

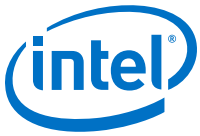
Figure 5. SMBus Block Diagram



1.25 DDR3 VREF Control Circuit

The ISL90728 chip for Channel B responds to SMBus address 0x7C. the ISL90727 chip for Channel A responds to SMBus address 0x5C. These digital potentiometer chips both reside in the DIMM_VREF_SMB segment of the CRB SMBus.

The CRB schematics show the digital potentiometers connected in parallel with 12.1 KΩ / 12.1 KΩ 1% resistor voltage dividers. This must be considered if calculating the resulting VREF voltage for particular settings of the potentiometer.



2.0 CRB Setup

2.1 CRB Configuration Setting Notes

Before powering on your board, review this guide, particularly this section.

The CRB schematics provide the ultimate definition of all HW configuration settings and options. See the schematics Table of Contents for relevant pages.

The primary source for CRB board configuration and setup are header jumpers. The critical jumper settings are defined in the schematics and are identified in this document. Additionally the soft strapping options are available in the *Intel® Communications Chipset 89xx Series Datasheet* and the *Intel® Xeon® and Intel® Core™ Processors For Communications Infrastructure External Design Specification*.

Configuration jumpers can be changed without a rework, but you might need to change jumper settings to perform specific functions. The processor and PCH strap settings, and JTAG, SMBus, and other configurations may be changed through jumper settings.

Note: The CRB is shipped with jumpers in place and is ready to boot.

Note: The CRB went through a series of burn-in tests before it was shipped.

An additional source for CRB configuration and setup options is via board-level stuffing resistors. These settings may be visible via the CRB schematics. These stuffing resistor settings should not be altered unless directed to do so by Intel; changes require a board rework.

The processor straps start being latched when PLTRST#/CPUPWRGD are asserted by the PCH. The latch in the processor closes approximately 250 ns after the de-asserting edge of PLTRST#.

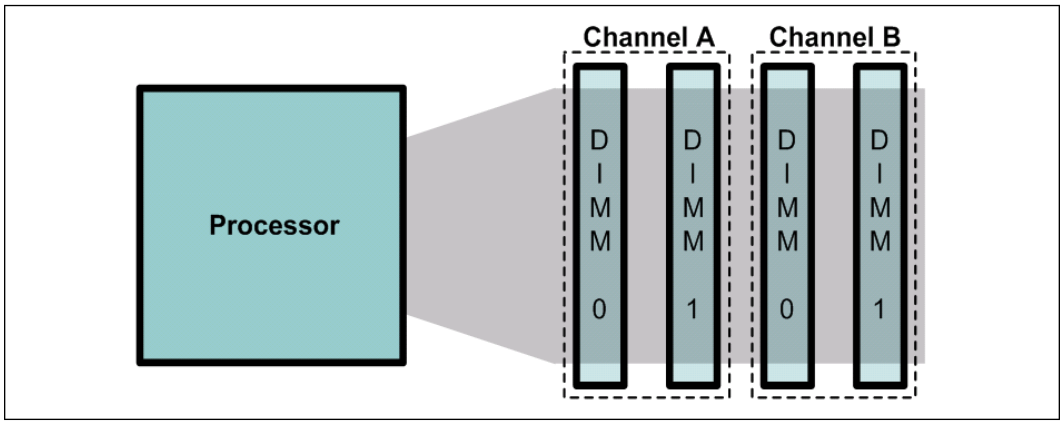
The PCH Functional Straps are used for static configuration. These straps are sampled either at the rising edge of RSMRST# or PWROK, depending on the strap. These straps select the required configurations and then revert to their normal pin usage.

Caution: The following precautions will help promote safe and proper operation of the CRB:

- Before connecting power, make sure the CRB is mounted on the provided stand-offs to avoid accidental shorts.
- The CRB is susceptible to damage by electrostatic discharge (ESD) that may result in platform failure or unpredictable operation. Make sure you are in a static-free work environment before removing components from their anti-static packaging.
- Connecting the wrong cable, or reversing a cable, may damage the CRB or a device being connected. Since the CRB is not in a protective chassis, use care when connecting cables to the platform.

2.2 Memory Module Plug-in

Figure 6. Memory Sockets



Note: See Memory Sub-System on page 10 for memory specific information.

1. Beginning with Channel A - DIMM1, line up the DIMM with the slot and make sure that the end clips are moved outward to the open position.
2. Gently push the DIMM into the socket until you hear or feel the end clips lock into the side of the DIMM.
3. Continue adding memory in accordance with Memory Sub-System on page 10.

2.3 Peripheral Setup

2.3.1 Connect SATA Cables

There are two Serial ATA (SATA) connectors on the CRB. Connect the cables to the appropriate drive sequentially starting from SATA Port 0 through Port 1.

Note: Intel recommends using SATA Port 0 as the boot drive (Port 4 in the Intel® Communications Chipset 89xx Series documentation).

2.3.2 Expansion Connectors

If necessary, connect PCI Express* add-in cards, possibly including the video card, in the appropriate Slot 1 through Slot 6 PCI Express slots.

- Slot 1 is a x4 link with a x8 connector. Some systems may not support Slot 1 or may have issues training with Slot 1. If you encounter issues with Slot 1, try a different slot.
- Slot 2 is a x8 link with a x16 connector (option for x16 link muxed with the Intel® Communications Chipset 89xx Series End-Point). Some systems may have issues training with Slot 2. If you encounter issues with Slot 2, try a different slot.
- Slots 3, 4, 5, and 6 are x1 link widths with x8 connectors.

- Intel recommends that you install the Matrox* video card in slot 3, and you connect the bottom DVI port to the monitor's VGA connection with a DVI-to-VGA adapter.

2.3.3 Rear Panel Connectors

- Connect a USB or PS/2 keyboard and/or mouse to the rear panel connectors.
- If using the video graphics card, connect the monitor to the PCIe x1 graphics card.

2.3.4 SPI Boot Devices

The BIOS is located on the SPI flash bootable devices. The CRB supports two SPI flash devices (SPI0 & SPI1) with the Descriptor, Soft-strap and ME residing on SPI0, and the BIOS residing on SPI1. The in-circuit Dediprog tool provides a way to program the flash memories. See Miscellaneous Jumper Settings on page 38.

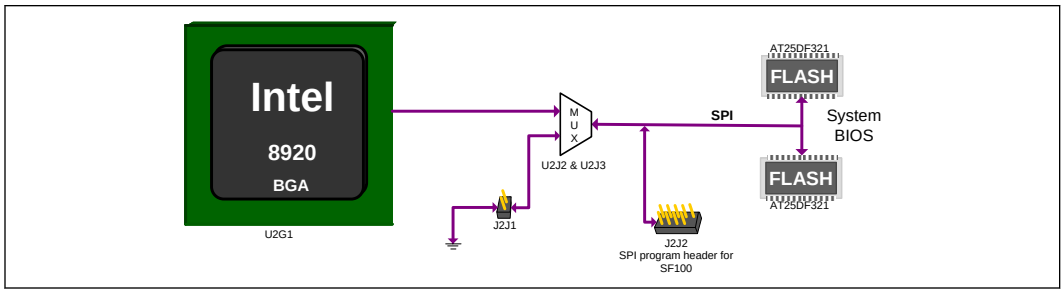
Normal Operation Mode (Default)

- When power is applied to the CRB, the switches used (U2J2 and U2J3) will automatically connect the PCH SPI signals to the SPI flash device.
- For the switch to function correctly in Normal Operation Mode, jumper J3J3 and J3J4, and the SPI program header (J2J2) for Dediprog SF100 must be empty.

Programming Mode

See Dediprog: SPI Flash Memory Programming on page 28.

Figure 7. SPI In-Circuit Programming

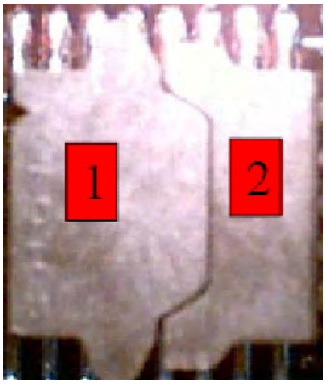


Note: The SPI bus includes MISO, MOSI, CLK, and CS signals.

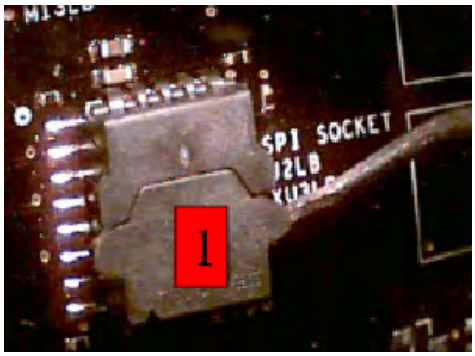
Note: The shunt must be removed from J2J1 to disable U2J2 and U2J3.

2.3.4.1 SPI Flash Memory Installation

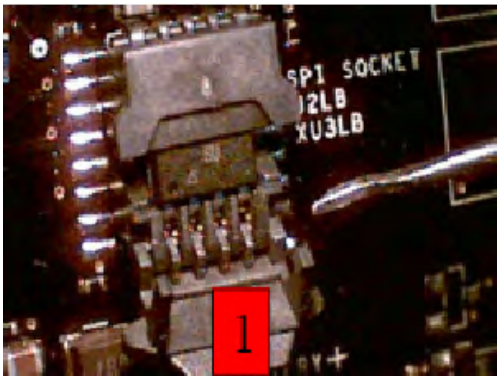
Prerequisites: Doors identified prior to install or removal of Flash device.



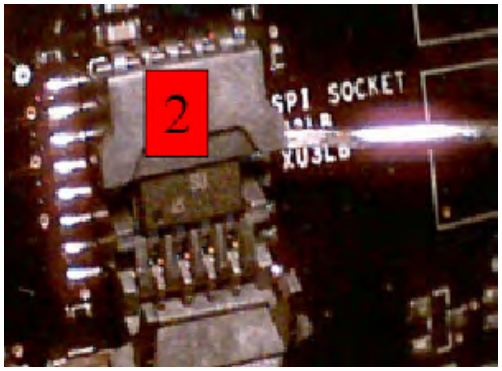
1. The #1 door shown below must be opened first to avoid damage to the socket. Door 1 is identified by the lip that is pointed out. Use a pick to gently push up from under the lip of Door 1.



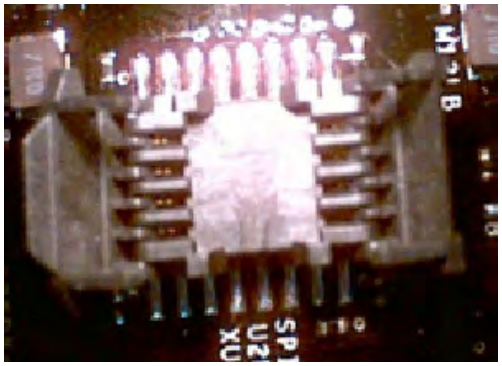
This is what it looks like with door 1 opened: (Note: SPI flash should be preinstalled)



2. Follow the same steps to open door 2.

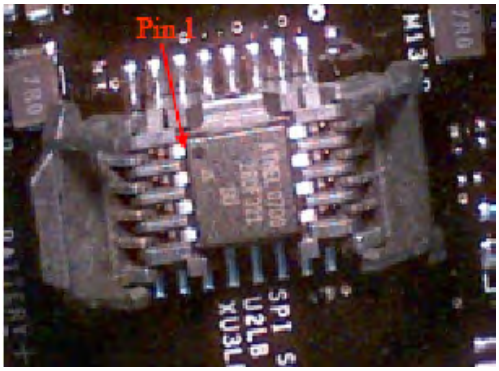


3. With socket doors open, the SOIC8 package can be installed.

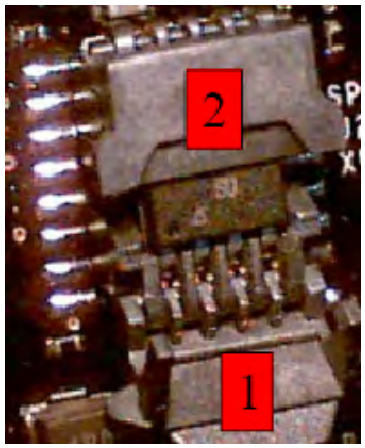


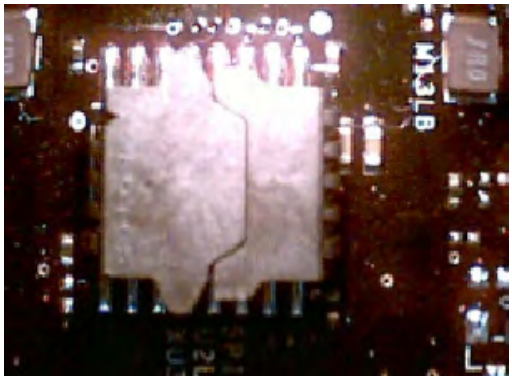
4. Align SOIC with guide slots. It is not necessary to apply pressure.

5. Align the pin 1 indicator on the IC with the pin 1 dot on the board silkscreen.



6. Gently close door 2, and then door 1.



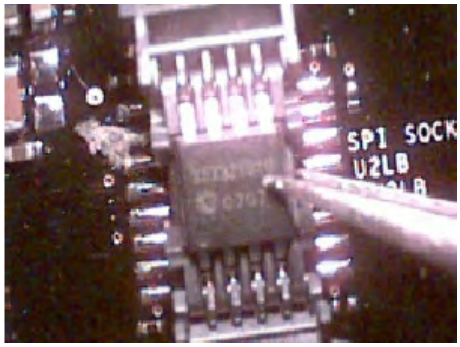


Note: Pressure will be applied with socket doors closed to ensure contact between the socket and the flash memory device.

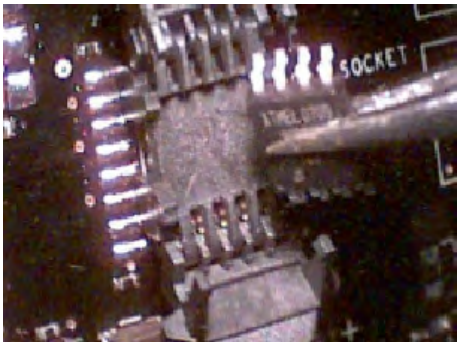
2.3.4.2 SPI Flash Memory Removal

1. Follow the steps from SPI Flash Memory Installation on page 23 to open the doors.

2. Use tweezers to gently remove the device from the socket.



3. Gently close the socket doors to avoid damage.



2.3.4.3 Dediprog: SPI Flash Memory Programming

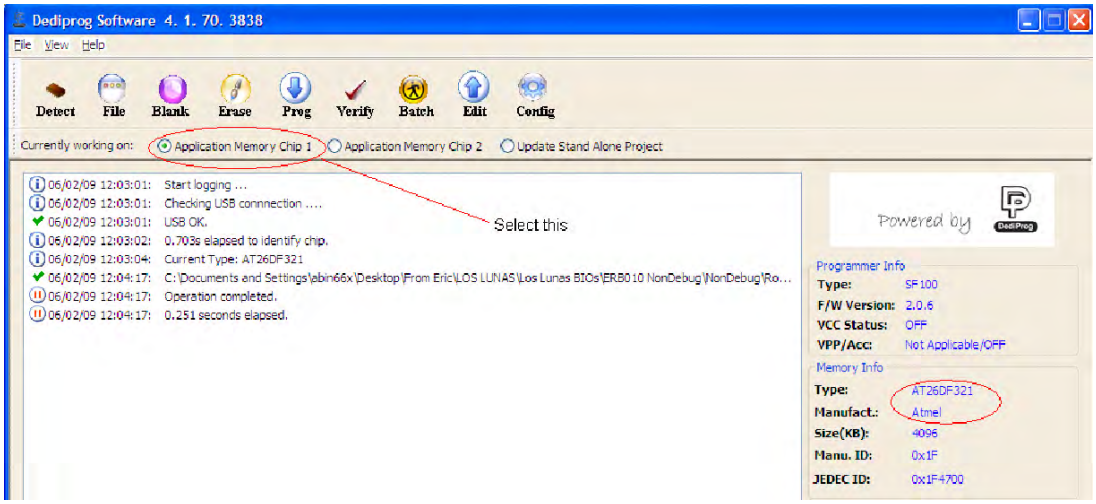
The Flash Programming Tool (FPT) is an MS-DOS* program that is included in the Intel® ME Ignition Firmware kit and allows for updating the PCH SPI device. Refer to the kit documentation for additional details on the FPT tool.

Note: Flash Descriptor Security Override strap (GPIO33, jumper J1G4) must be populated.

SPI Flash can be reprogrammed using the Dediprog device (SF100). You will need to purchase an additional converter (10 pin) from the Dediprog website http://www.dediprog.com/product.php?UID=99

Even though the SPI flash can be programmed with or without power on the board, it is best to do it with the board powered down.

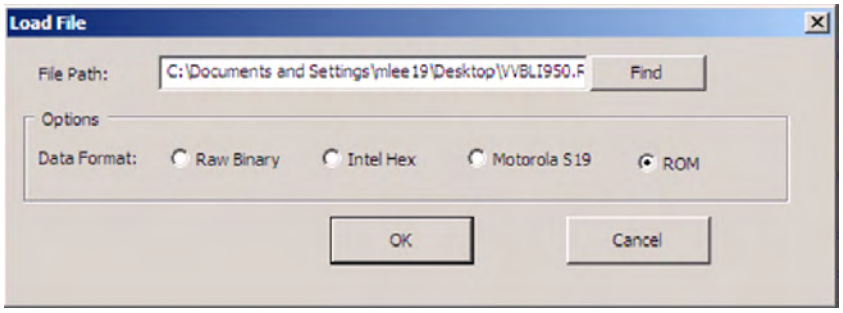
1. Disconnect the Intel® Communications Chipset 89xx Series SPI interface to SPI flash by removing the shunt from SPI_PROG jumper (J2J1) to program either SPI0 or SPI1.
2. Connect Dediprog to Dediprog connector header (J2J2), ensuring orientation is correct. Use the 10-pin header, which has a rainbow of colors. Pin 1 of the header (square pad) is connected to the brown strap of the cable.
3. Remove SPI WR protection jumpers J3J3 and J3J4 (if populated).
4. Launch the Dediprog software. Ensure that the program detects the correct type of flash device (for example, AT25DF321).



Note: The SPI can be damaged if programmed with a different algorithm. It is a good practice to restart the program when a different board is used. Verify that the "Application Memory Chip" is selected (SPI0, Application Memory Chip1 or SPI1, Application Memory Chip2).

The Dediprog software is a free download from: http://www.dediprog.com/SPI-flash-in-circuit-programming/SF100

5. Click **Erase** to blank the SPI.
6. Use **Blank** to verify the SPI has been erased.
7. After the blank check has been completed without any problem, click **File** to locate and open the file. If the suffix is .ROM, select **Data Format: ROM**. if the suffix is .BIN, select **Data Format: Raw Binary**. Click **OK.**



You need to program chip 1 and chip 2. Repeat steps 5 through 7 for Chip 1 and 2, using the following files:

- Application Memory Chip 1: `Rom00_4M_ST.bin`
- Application Memory Chip 2: `Rom01_4M.bin`

Note: See the File Descriptions section of the BIOS release notes to verify BIOS version and file names.

8. Need offset? At the main window, the file size is shown at the bottom right. For this example, the file size is 1 Mbytes or 8 Mbits. The AT25DF321 is 32 Mbits or 4 Mbytes. An offset may be needed, depending on the image size.

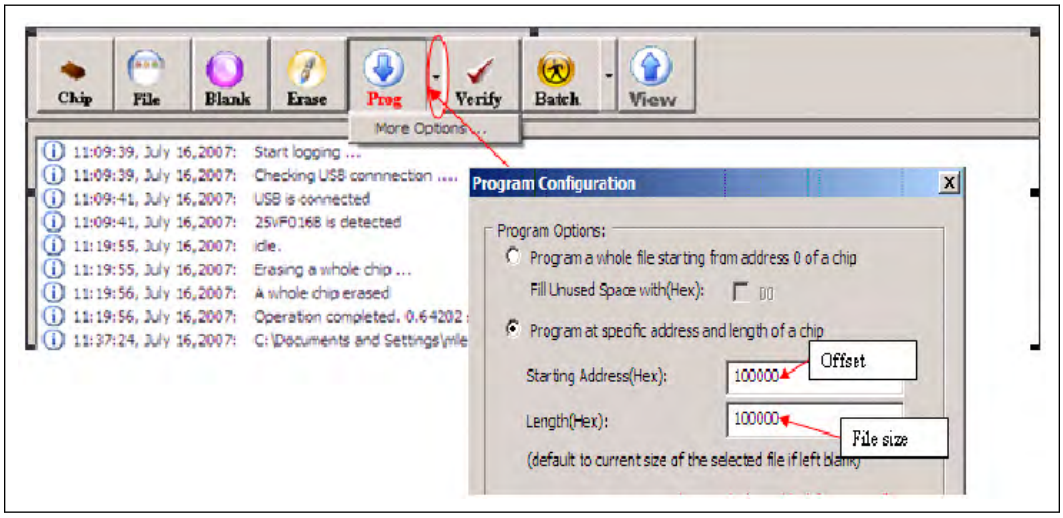
   Refer to the Dediprog Help for details.

Figure 8. Dediprog: SPI Flash Offset

	1 Mbytes Image	2 Mbytes Image	4 Mbytes Image
16 Mbits SPI	0x100000 offset	0x0 offset	N/A
32 Mbits SPI	0x300000 offset	0x200000 offset	0x0 offset

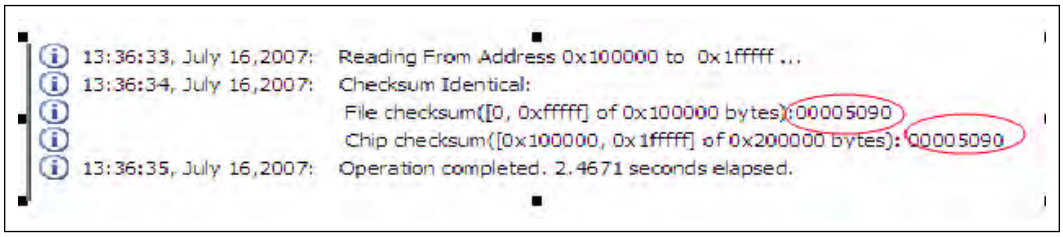
9. Check Offset Setting: Click the arrow next to **Prog**, then **More Options**. Always check the offset setting because the program saved the last used setting. Fill in the Starting Address and Length (file size). If no offset required, select the option for Program a whole file.

Figure 9. Offset Setting

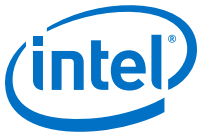


10. Program & Verify: Click **Prog** after save the Offset and File size. Finally, click **Verify** to verify the SPI. Make sure the checksum matches.

Figure 10. Offset Verification



11. Done: Disconnect the Dediprog cable before booting the system.



2.3.4.4 GbE EEPROM Devices

The system is designed to accept configuration EEPROM either from the CRB platform or from the PHY card. If there is no PHY card in the socket, the EEPROM (U1E2) from the CRB platform will be used. If the PHY card is plugged is, the EEPROM from the PHY-card will be used.

For guidelines on GbE EEPROM insertion and removal, see SPI Flash Memory Installation on page 23 and SPI Flash Memory Removal on page 27.

2.3.5 Connect Power

Caution: Do not force the power plugs into the connector; they should connect easily when plugged in correctly. Plugging them in incorrectly will result in severe damage to the CRB.

1. Insert the main 24-pin baseboard power plug into the motherboard's J4K4 SSI 24-pin power connector making sure that the plug clip lines up with the clip lock, and the connector pins fit easily into their appropriate slots.
2. Insert the 8-pin power plug into the motherboard's J5K2 SSI 8-pin power connector, making sure that the plug clip lines up with the clip lock, and the connector pins fit easily into their appropriate slots.
3. Insert the 4-pin power plug into the motherboard's J9D1 SSI 4-pin power connector, making sure that the plug clip lines up with the clip lock, and the connector pins fit easily into their appropriate slots.
4. Plug in any remaining peripheral power connectors (e.g., for hard drives and disc drives).
5. Plug the AC power cable into the back of the power supply. Plug the cord into the wall after the board is set up.

2.4 Turning On and Resetting the Board

The CRB board has two momentary push buttons. One push button is the power-on button, labeled "POWER," and the other button is the reset button, labeled "RESET."

Note: The power button is also used to wake a system that is in a sleep state.

3.0 Overview of BIOS Features

3.1 Introduction

The BIOS is stored in the SPI device on the PCH SPI bus. If SPI flash programming is necessary, contact your Intel technical representative about the SPI programming details.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The BIOS Setup program can be used to view and change the BIOS settings for the CRB. The BIOS Setup program is accessed by pressing the <F2> or <Delete> key after the POST test and memory test begin and before the operating system begins to boot.

3.1.1 PCI Auto-Configuration

The BIOS automatically configures PCI devices. Currently on the CRB, there are six PCI Express add-in card connectors. Auto-configuration lets a user insert or remove PCI Express cards without having to manually configure the system. When a user turns on the system after adding an add-in card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to AVAILABLE in setup are considered to be available for use by the add-in card.

3.2 System Management BIOS (SMBIOS)

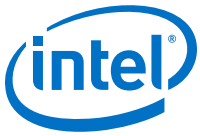
SMBIOS is a Desktop Management Interface (DMI)-compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level.
- Fixed-system data, such as peripherals, serial numbers, and asset tags.
- Resource data, such as memory size, cache size, and processor clock frequency.
- Dynamic data, such as event detection and error logging.

3.3 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support may be used to access the BIOS Setup program and to install an operating system that supports USB.



Legacy USB support operates as follows:

1. When applying power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS, allowing the use of a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system.

After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, follow the operating system's installation instructions.

3.4 Language Support

The BIOS Setup program and help messages are supported in US English.

3.5 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, USB device, or a network. The default setting is for the floppy to be the first and the hard drive to be the second.

3.5.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system attempts to boot from the next defined drive.

3.5.2 Network Boot

A network can be selected as a boot device using a network add-in card plugged into an add-in card slot. This selection allows booting from a network add-in card with a remote boot ROM installed.

In order to boot from the LAN, enter the BIOS, and select LAN boot as your first boot device.

3.5.3 USB Boot

In order to boot from a USB device, enter the BIOS, and select USB boot as your first boot device. The USB device should be set as the first priority device under Removable devices, and the USB device should be selected as the priority device in the Boot Priority menu.

Have the USB device plugged in when changing this BIOS setting.

3.5.4 Changing the Boot Device

Pressing the <Delete> key during POST causes the BIOS menu to be displayed. Using your arrow keys, move to <BOOT>, arrow down to <Boot Device Priority>, and then select the device you would like to boot first and second.

Note: Follow the instructions on the right side of the BIOS screen to navigate and change BIOS settings.

3.5.5 Serial Console Redirection

The pre-boot firmware supports redirection of both video and keyboard via a serial port. When console redirection is enabled, the remote console terminal sends keystrokes to the development board pre-boot firmware and the preboot firmware redirects the video to the console terminal.

As an option, the development board can be operated without a keyboard or video and can run entirely via the remote serial console. This includes accessing the pre-boot firmware setup menu.

Console redirection ends when operating system boot up begins. After boot up begins, the operating system is responsible for continuing the redirection.

Pre-boot firmware console redirection is text only. Graphical data, such as logos, are not redirected.

Table 2 shows the default settings of the serial console redirection.

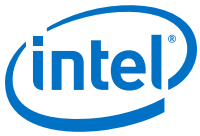
Table 16. Serial Console Redirection Default Settings

Parameter	Default
Port Number	COM 1
Baud Rate	115200
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None

3.6 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.



- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt is displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A–Z, a–z, and 0–9. Passwords may be up to 16 characters in length.

3.7 Boot Flow

When booting from a Global Reset, the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 starting at address 0x10 (for the PCH B0 Silicon). The descriptor fetch is triggered by either the assertion of MEPWROK or de-assertion of LAN_RST#; whichever occurs first. If the signature is present and valid, the PCH will boot in Descriptor Mode which is a requirement of the CRB. It will load up the descriptor into corresponding registers within the PCH.

With a valid descriptor, the PCH will look to the BBS0 and BBS1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from SPI flash (default boot destination on the CRB).

Once the BIOS destination is determined, the PCH will determine the location of BIOS on the SPI device through the base address that is defined in the SPI flash descriptor.

Appendix A Technical Reference

Detailed memory information for addressable memory and memory maps are in the *Intel® Communications Chipset 89xx Series Datasheet* and in the *Intel® Xeon® and Intel® Core™ Processors For Communications Infrastructure Datasheet*.

Caution: Do not move jumpers when the power is on. Always turn off the power and unplug the power cord before changing a jumper setting. Otherwise, the CRB may be damaged.

Caution: Only the back panel and PS/2 connectors have over-current protection. The other internal connectors are not over-current protected. Use caution with these connectors to avoid an over-current event.

A.1 CMOS Battery Replacement

With the board shut down and with the power supply disconnected, remove the 3 V coin battery (B1B1) and replace it with a new battery. Dispose of used batteries according to the vendor's instructions.

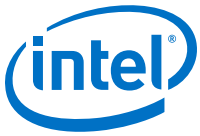
Caution: There is a risk of explosion if the lithium battery is replaced with an incorrect battery type.

CMOS batteries rarely fail, but an indication of battery failure is when you must restore your BIOS settings and system time after unplugging the system and plugging it in again. With a failed battery, this occurs every time power is removed from the power supply.

A.2 Clearing CMOS Memory

1. ***Caution:*** Do not move jumpers when the power is on. Always turn off the power and unplug the power cord before changing a jumper setting. Otherwise, the CRB may be damaged.

   With the system shut down, unplug the power supply and/or turn the power supply to the off position to remove all sources of power to the board.
2. Remove jumper J1J5 from pins 1 and 2 and place it on pins 2 and 3.
3. Leave the jumper in place for approximately 20 seconds.
4. Remove the jumper from pins 2 and 3 and return it to pins 1 and 2.
5. Make sure the CMOS is cleared. if not, make sure power is removed from platform and leave the jumper on pins 2 and 3 for a longer duration. The board should display a setup prompt before booting, asking you to choose to either use defaults or enter the BIOS.



A.3 Processor Straps - Jumper Settings

Table 17. Processor Straps - Jumper Settings

Jumper Name	Ref Des Location	Color	Default Setting	Description		
CFG[2] PCIe x16 Lane Reversal	J6E5	Blue	Open	Open: Normal Operation Closed: Lane Reversed		
CFG[3] PCIe x4 Lane Reversal	J6E6	Blue	Open	Open: Normal Operation Closed: Lane Reversed		
CFG[5] CFG[6] PCIe Port Bifurication	J6E4 J6F6	Blue	Closed Open	**J6E4**	**J6F6**	**Operation**
				Open	Open	x16 operation
				Closed	Open	x8 & x8 (default)
				Open	Closed	RESERVED
				Closed	Closed	x8, x4 & x4
CFG[7]	J6E2	Blue	Closed	Reserved		

A.4 PCH Straps - Jumper Settings

Table 18. PCH Straps - Jumper/Resistor Settings

Jumper Name	Ref Des Location	Color	Default Setting	Description		
INTRUDER Protection (INTRUDER_N)	J1J2	Black	Open	Open: Normal Closed: Disable Power		
No Reboot (NRBOOTS)	J1H1	Blue	Open	Open: Normal Closed: No Reboot		
Boot Device Select (BBS0)	J1H3 J1H4	Blue	Headers Unpopulated	**J1H3**	**J1H4**	**Operation**
				Open	Open	SPI (default)
				Open	Closed	Reserved
				Closed	Open	Reserved
				Closed	Closed	Reserved
CMOS Reset	J1J5	Blue	Shunt [1-2]	1-2: Normal 2-3: Reset (hold for 20 seconds)		
Secondary RTC Reset	J1J4	Blue	Shunt [1-2]	1-2: Normal 2-3: Reset (hold for 20 seconds)		
DMI TX Voltage (GPIO17)	J1G7	Blue	Pull Up Open	Open: Sets the DMI termination voltage to Vcc/2 Closed: Sets the DMI termination voltage to Vcc		

continued...

Jumper Name	Ref Des Location	Color	Default Setting	Description
Core Oscillator Power Strap (GPIO30)	J1H6	Blue	Closed	Open: VCC1P0_STBY (external) Closed: SFI Out (internal)
Flash Sec Descriptor Override Low (GP33)	J1G4	Blue	Open	Open: Normal Closed: Security Override
DMI Mode (GPIO53)	R2G37(PU)	N/A	Pull Up	Pull Up: DC Coupling Pull Down: AC Coupling
Top Block Swap (GPIO55)	R2G46(PU)	N/A	Pull Up	Pull Up: Normal Pull Down: Swap Top Block (BIOS)
BIOS Recovery Strap (PCH_GP46)	J5A3	Blue	Open	Open: Normal Mode Closed: BIOS Recovery Mode

A.5 Miscellaneous Jumper Settings

Table 19. Miscellaneous Jumper/Resistor Settings

Jumper Name	Ref Des Location	Color	Default Setting	Description
EP JTAG Enable	J6D1	Black	Open	3-pin header for Endpoint JTAG enable/ disable Shunt 1-2: PCH JTAG only Shunt 2-3: EP JTAG only Open: PCH & EP JTAG
GPIO25 DDR3 Voltage Select	J9C2	Black	Open	Open: VDD1P5_DDR is 1.5V (default) Closed: VDD1P5_DDR is 1.35V
PCH WDT Enable	J4A1	Black	Open	When closed, this header enables the board to reset the board when the WDT times out
CPU Fan Override (CPU_FAN_CTRL)	J7D1	Black	Open	Open: Manual Control Full Speed Closed: PWM Control
PCH Fan Override (PWM2_PCHFAN)	J3J2	Black	Shunt [1-2]	Open: PWM Control Closed: Full Speed
VTT_SA_VID Select (VTT_SA_CPU_VID0)	J6K2	Black	Shunt [2-3]	Shunt [1-2]: 0.8V Shunt [2-3]: 0.89V
THRMTRIP Clear	J6E1	Black	Shunt [1-2]	Open: Clear THRMTRIP LED Closed: Normal
Serial Port Selection (Port 1)	J3A3	Black	Open	Open: SIO Serial <-> Serial Port #1 Closed: Intel® Communications Chipset 89xx Series (Serial Port #2) <-> Serial Port #1
SIO Enable (LPC_FRAME_SIO_N)	J3A2	Black	Shunt [1-2]	Open: Disable SIO Closed: Enable SIO

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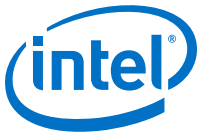


Jumper Name	Ref Des Location	Color	Default Setting	Description
SPI In Circuit Programming Mode	J2J1	Black	Shunt [1-2]	Open: SPI Programming Mode Closed: Normal Operation
SPI CS0_PU Enable (SPI_PROG_CS0_N)	J3K1	EMPTY	Open	Open: CS0 PU Disable Closed: CS0 PU Enabled
SPI CS1_PU Enable (SPI_PROG_CS01_N)	J2K1	EMPTY	Open	Open: CS1 PU Disable Closed: CS1 PU Enabled
SPI0 Flash Write Protect	J3J3	Black	Open	Open: Allow Writes Closed: Write Protect SPI0
SPI1 Flash Write Protect	J3J4	Black	Open	Open: Allow Writes Closed: Write Protect SPI1
Main Power Mode	J4K1	Black	Shunt [1-2] Shunt [3-4]	4-pin header 5V power supply voltage select Shunt 1-2/3-4: VCC5_PS_STBY Open: VCC5_PS
PS_ON Override	J5F1	Black	Shunt [1-2]	Open: Main Off/Stby only Shunt 1-2: Normal operation Shunt 2-3: Main power operation Open: MAIN OFF/ STBY Only
BRD ID EEPROM Write Protect (FRUID_WR)	J1A4	Black	Shunt [1-2]	Open: Write Enable Closed: Write protected
GbE EEPROM Write Protect	J1E1	Black	Shunt [1-2]	Shunt 1-2: Write Protected Open: Allow writes
CPU System Agent Voltage Selection (VTT_SA_CPU0)	J6K1	Black	Shunt [2-3]	Shunt 1-2: VID0 forced high (VOUT = 0.5 (1 + RFS/ROFS)) Shunt 2-3: VID0 forced low (VOUT = 0.55 (1 + RFS/ROFS))
CPU System Agent Vsref Selection	J6K2	Black	Shunt [2-3]	Shunt 1-2: VTT_SA VID0 pin pulled high (SNB) Shunt 2-3: VTT_SA VID0 pin pulled high (IVB)
DMI Voltage CPU_SNB_IVB_N	J8K4	Black	Shunt [2-3]	Shunt 1-2: 1.0V (Ivy Bridge processor) Shunt 2-3: 1.05V (2nd Generation Intel® Core™ Mobile Processor)

Table 20. Reserved Headers

Ref Des	Colour	Default Setting[1]
J1F8	Blue	Open
J1G2	Red	Open
J1G3	Red	Open
J1G5	Blue	Open
J1G6	Red	Open
J2H1	Black	Open
J3E1	Black	Open

continued...

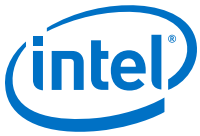
Ref Des	Colour	Default Setting[1]
J3F1	Black	Open
J3G1	Black	Open
J3H1	Black	Open
J4G1	Black	Open
J5A4	Red	Open
J6A1	Red	Open
J6A2	Black	Open
J6E3	Blue	Open
J6E7	Red	Open
J6F1	Blue	Open
J6F2	Blue	Open
J6F3	Blue	Open
J6F5	Red	Open
J6F7	Red	Open
J6F8	Black	Open
J8C1	Black	Open
J8C2	Black	Open
J8D2	Red	Open
J8D3	Red	Open
J8D4	Red	Open

1. The headers below are implemented primarily for board debug purposes. Please ensure that these are correctly populated to ensure board operation.

A.6 SMBus Headers

Table 21. SMBus Headers

Jumper Name	Ref Des Location	Default Setting	Description
EP_SMBus Header	J3D1	Open	Header for the PCH Endpoint Header
GBE_SMBus Header	J4J1	Open	GbE SMBus Header
PCH_SMLink1 Header	J4J2	Open	PCH SMLink Header
SMBus PCH - PCIe Slot Header	J5B2	Open	Header on PCIe SMBus
SMBus PCH - DDR VREF Header	J7D2	Open	Header on DDR VREF SMBus
SMBus PCH - LPC/TPM Header	J1B2	Open	Header on LPC/TPM SMBus
SMBus PCH - DIMM Header	J7E3	Open	Header on DIMM SMBus
SMBus PCH - Clock Header	J5A2	Open	Header on Clock SMBus



A.7 Voltage Measurement Headers

Table 22. Voltage Measurement Headers

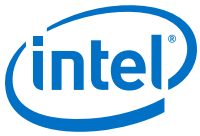
Jumper Name	Ref Des Location	Default Setting [1]	Description
VCC5_PS	J5K1	Open	5.0V input voltage measurement
VCC3P3_PS	J9B2	Open	3.3V input voltage measurement
VCC12_PS	J4K3	Open	12V input measurement
VCC5_PS_STBY	J4K2	Open	5.0V standby voltage measurement
VCC5_AUX	J9B1	Open	5.0V aux voltage measurement
VCC3P3_AUX	J1A1	Open	3.3V AUX voltage measurement
VCC5_SW	J4J3	Open	5.0V switch voltage measurement
VCC3P3_STBY	J9C1	Open	3.3V standby voltage
VTT_SA_CPU	J6K3	Open	System Agent(0.8V-0.89V) voltage measurement
VCC1P8_CPU	J8K3	Open	1.8V CPU voltage measurement
VDD1P5_DDR	J9E1	Open	DDR3 (1.5V) voltage measurement
VTT_CPU	J7K2	Open	CPU VTT (1.05V) voltage measurement
VCC_CORE_CPU	J6K4	Open	VCC core (0.8V-1.3V) voltage measurement
VCC1P0_PCH	J1A5	Open	1.0V PCH voltage measurement
VCC1P0_STBY	J1A2	Open	1.0V standby voltage measurement
VCC1P0_AUX	J1A6	Open	1.0V aux voltage measurement
VCC1P8_AUX	J3A1	Open	1.8V aux voltage measurement
VCC1P8_STBY	J1A3	Open	1.8V standby voltage measurement
VCC1P8_PCH	J1H5	Open	1.8V PCH voltage measurement
VCCDMI_PCH	J3H1	Open	1.05V DMI voltage measurement
VCC1P05_AUX	J3E1	Open	1.05V aux voltage measurement
1. Do not short pin headers to ground. Doing so may damage the board.			

A.8 LED Indicators

Table 23. LED Indicators

LED Name	Ref Des Location	"ON" Color	Description (LED "ON" State)
12 V Voltage	DS4K3	Green	VCC12_PS voltage present
5 V Main Voltage	DS5K1	Green	VCC5_PS voltage present
5 V Main Standby Voltage	DS4K2	Green	VCC5_PS_STBY voltage present
5 V Aux Power	DS9B1	Green	VCC5_AUX voltage present
			continued...

LED Name	Ref Des Location	"ON" Color	Description (LED "ON" State)
5V SW Power	DS4K1	Green	VCC5_SW voltage present
3.3V Voltage	DS9C1	Green	VCC3P3_PS voltage present
3.3 V Standby Voltage	DS9C2	Green	VCC3P3_STBY voltage present
3.3 V Aux Power	DS1A1	Green	VCC3P3_AUX voltage present
1.8V PCH Voltage	DS1H1	Green	VCC1P8 voltage present
1.8V PCH STBY Voltage	DS1A3	Green	VCC1P8 STBY voltage present
1.8V PCH AUX Voltage	DS3A1	Green	VCC1P8 AUX voltage present
1.05V PCH AUX Voltage	DS3E1	Green	VCC1P05_PCH voltage present
1.0V PCH Voltage	DS1A4	Green	VCC1P0_PCH voltage present
1.0V PCH STBY Voltage	DS1A2	Green	VCC1P0_STBY voltage present
1.0V PCH AUX Voltage	DS1A5	Green	VCC1P0_AUX voltage present
PCH DMI Voltage	DS3H1	Green	VCCDMI_PCH voltage present
CPU VTT Power	DS7K1	Green	VTT_CPU voltage present
CPU VTT_SA Power	DS6K1	Green	VTT_SA System Agent voltage present
CPU 1.8_CPU	DS8K1	Green	VCC1P8_CPU voltage present
CPU Core Power	DS6K2	Green	VCCP_CORE_CPU voltage present
CPU DDR3 Power	DS9E1	Green	VDD1P5_DDR voltage present
System Power OK	DS1E1	Green	SYS_PWROK signal is active
PCH Power OK	DS1F1	Green	PCH_PWROK signal is active
Sleep S3	DS1F3	Yellow	PCH_S3_N signal is active
Sleep S4	DS1F2	Yellow	PCH_S4_N signal is active
Sleep S5	DS1F5	Yellow	PCH_S5_N signal is active
Resume Reset	DS1F4	Red	RSMRST signal is active
Platform Reset	DS6A1	Red	PLTRST_N signal is active
SATA Hard Drive Active	DS1B1	Green	SATA_HD_LED_N signal is active
LAN Link Status GBE_LED[3:0]	DS2E1 DS2E2 DS2E3 DS2E4	Yellow Green Yellow Green	The controller implements one output driver per port intended for driving external LED circuits. LED outputs can be individually configured to select the particular event, state, or activity, which is indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus non-blinking (steady-state) indication.
CPU CATTERR	DS5F3	Red	CPU_CATERR output signal is active
PROCHOT#	DS6B1	Yellow	CPU Processor Hot output signal is active
CPU RESET#	DS5F2	Red	CPU Reset signal is active
CPU THERMTRIP#	DS5F1	Red	The CPU Thermal Trip output signal is active
PCH Wake	DS2F1	Green	PCH Wake Signal is active
WDT Time-out	DS2E5	Yellow	PCH WDT_TOUT is active



A.9 Power Supply Connectors

The power supply connectors conform to the SSI EPS12V specification.

Table 24. 24-pin Main Power Connector Pins (Top-View)

Signal Name	Pin		Pin	Signal Name
+3.3 V	13		1	+3.3 V
-12 V	14		2	+3.3 V
GND	15		3	GND
PS_ON	16		4	+5 V
GND	17		5	GND
GND	18		6	+5 V
GND	19		7	GND
RSVD	20		8	PWR_OK
+5 V	21		9	+5 V Standby (5VSB)
+5 V	22		10	+12 V (+12V2)
+5 V	23		11	+12 V (+12V2)
GND	24		12	+3.3 V

Table 25. 8-pin Processor Power Connector Pins (Top-View)

Signal Name	Pin		Pin	Signal Name
+12 V (+12V1)	5		1	GND
+12 V (+12V1)	6		2	GND
+12 V (+12V1)	7		3	GND
+12 V (+12V1)	8		4	GND

Table 26. 4-pin DDR Power Connector Pins (Top-View)

Signal Name	Pin		Pin	Signal Name
+12 V (+12V1)	3		1	GND
+12 V (+12V1)	4		2	GND

A.10 Front Panel Connector

Table 27. 9-pin Front Panel Connector Pins (Top-View)

Description	Signal Name	Pin		Pin	Signal Name	Description
PU resistor (5V) for hard drive LED	FP_VCC_HDLED	1		2	FP_LED_GRN_N	ATX power on indicator LED
Hard drive LED driver output	FP_HD_LED_N	3		4	FP_LED_YLW_N	User defined LED driver output (GP27)

continued...

Description	Signal Name	Pin		Pin	Signal Name	Description
GND	FP_PD1	5		6	FP_PWR_BTN_N	Power button
Reset button	FP_RST_BTN_N	7		8	FP_PD2	GND
5V supply (VCCV_PS)		9			NC	

A.11 Memory Resources

Detailed memory information for addressable memory and memory maps are in the *Intel® Communications Chipset 89xx Series Datasheet* and in the *Intel® Xeon® and Intel® Core™ Processors For Communications Infrastructure External Design Specification*

A.12 Interrupts

Interrupts can be routed through the I/O xAPIC, which supports 24 interrupts. The I/O xAPIC is supported by Microsoft OS's.

Table 28. I/O xAPIC Interrupt Mapping [1]

IRQ [2]	Via SERIRQ	Via PCI Message	System Resource
0	No	No	Cascade from 8259 #1
1	Yes	Yes	
2	No	No	8254 Counter 0, HPET #0 (legacy mode)
3	Yes	Yes	
4	Yes	Yes	
5	Yes	Yes	
6	Yes	Yes	
7	Yes	Yes	
8	No	No	Real-time clock, HPET #1 (legacy mode)
9	Yes	Yes	Option for SCI, TCO
10	Yes	Yes	Option for SCI, TCO
11	Yes	Yes	HPET #2, option for SCI, TCO [3]
12	Yes	Yes	HPET #3 [4]
13	No	No	FERR# logic
14	Yes	Yes	SATA
15	Yes	Yes	SATA
16	PIRQA#	Yes	Internal devices are routable.
17	PIRQB#		
18	PIRQC#		
19	PIRQD#		

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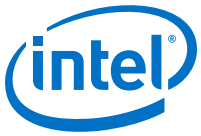

IRQ [2]	Via SERIRQ	Via PCI Message	System Resource
20	N/A	Yes	Option for SCI, TCO, HPET #0, 1, 2, 3. Other internal devices are routable.
21	N/A		
22	N/A		
23	N/A		

1. PIRQ is not externally routed rather they are used to reference internally routed PCIe* interrupts.
2. When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources, while interrupts 16 through 23 receive active-low internal interrupt sources
3. If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of HPET #2. The hardware does not prevent sharing of IRQ 11.
4. If IRQ 12 is used for HPET #3, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of HPET #3. The hardware does not prevent sharing of IRQ 12.

Table 29. PCH GPIO Mapping

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
BMBUSY# /GPI0	I/O	GPI	1	I	CORE		CORE Bus Master Busy. This signal is used to support the C3 state. It indicates that a bus master device is busy. When this signal is asserted, the BM_STS bit will be set. If this signal goes active in a C3 state, it is treated as a break event. This signal is internally synchronized using the PCICLK and a two-stage synchronizer. It does not need to meet any particular setup or hold time. This signal can also be used as GPIO Port 0.
GPIO1	I/O	GPI	1	I	CORE		General Purpose I/O Port 1. Not Multiplexed.
GPIO2 [1]	I/O	GPI	1	I	CORE		General Purpose I/O Port 2. Not Multiplexed.
GPIO3 [1]	I/O	GPI	1	I	CORE		General Purpose I/O Port 3. Not Multiplexed.
GPIO4 [1]	I/O	GPI	1	I	CORE		General Purpose I/O Port 4. Not Multiplexed.
GPIO5 [1]	I/O	GPI	1	I	CORE		General Purpose I/O Port 5. Not Multiplexed.
GPIO6	I/O	GPI	1	I	CORE		General Purpose I/O Port 6. Not Multiplexed.
GPIO7	I/O	GPI	1	I	CORE		General Purpose I/O Port 1. Not Multiplexed.
GPIO8	I/O	GPO	1	O (High)	SUS	Weak Internal pull-up for strap	General Purpose I/O Port 8. Not Multiplexed. This signal has a weak internal pull-up and must not be pulled low at boot up
GPIO9 [2]	I/O	Native	1	I	SUS		General Purpose I/O Port 9. Not Multiplexed [3]

continued...

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
GPIO10 [2]	I/O	Native	1	I	SUS		General Purpose I/O Port 9. Not Multiplexed [3]
MST_SMBALERT#/ GPIO11 [2]	I/O	MST_SMBALERT#	1	I	SUS	External pull-up required	SUS SMBus Alert. This signal is used to wake the system or generate SMI#. External pull-up resistor to VCCSUS3P3 is required. Resistor value should be calculated based on the bus load, see the Platform Design Guide. This signal can also be configured to GPIO Port 11.
GPIO12	I/O	Native	1	O (Low)	SUS		General Purpose I/O Port 12. Not Multiplexed. [3]
GPIO13 [4]	I/O	GPI	1	I	SUS	Weak internal pull-down	General Purpose I/O Port 13. Not Multiplexed
GPIO14	I/O	Native	1	I	SUS		General Purpose I/O Port 14. Not Multiplexed [3]
GPIO15	I/O	GPO	1	O (Low)	SUS		General Purpose I/O Port 15. Not Multiplexed
SATA4_GP /GPIO16	I/O	GPI	1	I	CORE		Serial ATA 4 General Purpose. This is an input pin which can be configured as an interlock switch corresponding to SATA Port 4. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO port 16
GPIO17	I/O	GPI	1	I	CORE	Platform Dependent	General Purpose I/O Port 17. Not Multiplexed. This signal strapping sets the DMI termination voltage.
GPIO18	I/O	Native	1	I	CORE		General Purpose I/O Port 18. Not Multiplexed [3]
GPIO19	I/O	GPI	1	I	CORE		General Purpose I/O Port 19. Not Multiplexed.
GPIO20	I/O	Native	1	I	CORE		General Purpose I/O Port 20. Not Multiplexed.
GPIO21	I/O	GPI	1	I	CORE		General Purpose I/O Port 21. Not Multiplexed.
SCLOCK/ GPIO22	I/O	GPI	1	I	CORE		SGPIO Reference Clock. The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. If SCLOCK interface is not used, this signal can be used as a GPIO Port 22.
LDRQ1#/ GPIO23	I/O	LDRQ1#	1	I	CORE		LPC Serial DMA/Master Request Input Bit 1. Used by LPC devices, such as Super I/O chips, to request DMA or bus master access. This signal is typically connected

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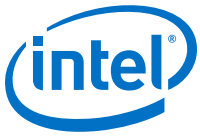

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
							to external Super I/O device. An internal pull-up resistor is provided on these signals. If LDRQ1# interface is not used, this signal can be used as a GPIO Port 23.
GPIO24	I/O	GPO	1	O (Low)	SUS		General Purpose I/O Port 24. Not Multiplexed
GPIO25	I/O	Native	1	I	SUS		General Purpose I/O Port 25. Not Multiplexed [3]
GPIO26	I/O	Native	1	I	SUS		General Purpose I/O Port 26. Not Multiplexed [3]
GPIO27	I/O	GPO	1	O (Low)	SUS		General Purpose I/O Port 27. Not Multiplexed
GPIO28	I/O	GPI	1	I	SUS		General Purpose I/O Port 28. Not Multiplexed
GPIO30	I/O	GPI	1	I	SUS	Internal pull-down	General Purpose I/O Port 30. Not Multiplexed
GPIO31 [5]	I/O	GPI	1	I	SUS		General Purpose I/O Port 31. Not Multiplexed
GPIO32 [4]	I/O	Native	1	O (High)	CORE		General Purpose I/O Port 32. Not Multiplexed [3]
GPIO33 [4]	I/O	GPO	1	O (High)	CORE	Weak internal pull-up	General Purpose I/O Port 33. Not Multiplexed Flash Descriptor Security Overwrite. This signal is used to set the security override strap on the PCH. If sampled low, the Flash Descriptor Security will be overridden. If high, the security measures defined in the Flash Descriptor will be in effect. This strap should only be enabled (pulled low) in manufacturing environments using an external pull-down resistor. GPIO33 0 Enable (Pull-Down Required) 1 Disable (Default) When the Security Overwrite is enabled, it allows permission to every master to read and write to the entire Flash Components including areas outside the defined regions.
GPIO34	I/O	GPI	1	I	CORE		General Purpose I/O Port 34. Not Multiplexed
GPIO35	I/O	GPO	1	O (Low)	CORE		General Purpose I/O Port 35. Not Multiplexed
GPIO36	I/O	GPI	1	I	CORE		General Purpose I/O Port 36. Not Multiplexed
ADR/ GPIO37	I/O	GPI	1	I	CORE		General Purpose I/O Port 37. Can be used for ADR (Asynchronous DRAM Refresh) trigger on platform. Only supported if processor supports ADR. HARDWARE activation mechanism that

continued...

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
							triggers memory controller of CPU to put SDRAM into self-refresh mode. Activation of ADR flushes contents of some write data buffers to the DIMM before self refresh entry.
SLOAD/ GPIO38	I/O	GPI	1	I	CORE		SATA Serial GPIO Load. The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SLOAD interface is not used, this signal can be used as a GPIO Port 38.
SDATAOUT0/ GPIO39	I/O	GPI	1	I	CORE		SATA Serial GPIO Data Out 0. Driven by the controller to indicate the drive status in the following sequence: drive 4, 5...4,5... If SDATAOUT0 interface is not used, this signal can be used as a GPIO Port 39.
OC1#/ GPIO40 [2]	I/O	OC1#	1	I	SUS		Overcurrent Indicators. These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[3:0]# may optionally be used as GPIO Ports [42,41,40,59]. *Note:* 1. OC# pins are 3.3V and NOT 5V tolerant 2. OC# pins must be shared between ports 3. OC#[3:0] can only be used for EHCI controller #1
OC2#/ GPIO41 [2]	I/O	OC2#	1	I	SUS		Overcurrent Indicators. These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[3:0]# may optionally be used as GPIO Ports [42,41,40,59]. *Note:* 1. OC# pins are 3.3V and NOT 5V tolerant 2. OC# pins must be shared between ports 3. OC#[3:0] can only be used for EHCI controller #1
OC3#/ GPIO42 [2]	I/O	OC3#	1	I	SUS		Overcurrent Indicators. These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[3:0]# may optionally be used as GPIO Ports [42,41,40,59]. *Note:* 1. OC# pins are 3.3V and NOT 5V tolerant 2. OC# pins must be shared between ports

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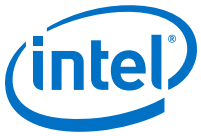

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
							3. OC#[3:0] can only be used for EHCI controller #1
GPIO43 [2]	I/O	Native	1	I	SUS		General Purpose I/O Port 43. Not Multiplexed [3]
GPIO44	I/O	Native	1	I	SUS		General Purpose I/O Port 44. Not Multiplexed [3]
GPIO45	I/O	Native	1	I	SUS		General Purpose I/O Port 45. Not Multiplexed [3]
GPIO46	I/O	Native	1	I	SUS		General Purpose I/O Port 46. Not Multiplexed [3]
GPIO47	I/O	Native	1	I	SUS		General Purpose I/O Port 47. Not Multiplexed [3]
SDATAOUT1/ GPIO48	I/O	GPI	1	I	CORE		SATA Serial GPIO Data Out 1. Driven by the controller to indicate the drive status in the following sequence: drive 4, 5...4,5... If SDATAOUT1 interface is not used, this signal can be used as a GPIO Port 48.
SATA5_GP/ TEMP_ALERT#/ GPIO49	I/O	GPI	1	I	CORE		Serial ATA 5 General Purpose. This is an input pin which can be configured as an interlock switch corresponding to SATA Port 5. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. Temperature Alert. Used as an alert (active low) to indicate to the external controller (such as, EC or SIO) that temperatures are out of range for the PCH or Memory Controller or the processor core. If interlock switches or Temp Alert are not required, this pin can be configured as GPIO Port 49.
GPIO50 [2]	I/O	Native	1	I	CORE		General Purpose I/O Port 50. Not Multiplexed [3]
BBS1/ GPIO51	I/O	BBS1	1	O (High)	CORE	Weak internal pull-up	BIOS Boot Strap 1. **BBS1** / **BBS0**: 0/0 Not valid; 0/1 Not valid; 1/0 Not valid; 1/1 SPI boot If BBS1 interface is not used, the signals can be used as GPIO Port 51. [3]
GPIO52 [2]	I/O	Native	1	I	CORE		General Purpose I/O Port 52. Not Multiplexed.

continued...

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
GPIO53	I/O	Native	1	O (High)	CORE	Platform Dependant. Weak internal pull-up	General Purpose I/O Port 53. Not Multiplexed. [3] External platform dependent. DMI Coupling Strap. 0 AC Coupling (Pull-Down Required) 1 DC Coupling (Default)
GPIO54 [2]	I/O	Native	1	I	CORE		General Purpose I/O Port 54. Not Multiplexed [3]
GPIO55	I/O	Native	1	O (High)	CORE	Weak internal pull-up	General Purpose I/O Port 55. Not Multiplexed. [3] Strap for BIOS Boot-Block Update Scheme. This mode allows the PCH to swap the Top-Block in the SPI (the boot block) with another location. GPIO55 0 Enable Top-Block Swap (Pull-down required) 1 Disable Top-Block Swap (Default) The internal pull-up is disabled after PLTRST# deasserts. If the signal is sampled low, this indicates that the system is strapped to the "Top-Block Swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Software will not be able to clear the Top-Swap bit until the system is rebooted without GPIO55 being pulled down.
GPIO56	I/O	Native	1	I	SUS		General Purpose I/O Port 56. Not Multiplexed. [3]
GPIO57	I/O	GPI	1	I	SUS		General Purpose I/O Port 57. Not Multiplexed.
SML1CLK/ GPIO58	I/O	SML1CLK	1	I	SUS	When SMBUS: External pull-up required	System Management Link 1 Clock. SMBus link to external BMC. External pull-up resistor to VCCSUS3P3 is required. Resistor value should be calculated based on the bus load, refer to the Platform Design Guide. If SML1CLK interface is not used, the signals can be used as GPIO Port 58.
OC0#/ GPIO59 [2]	I/O	OC0#	1	I	SUS		Overcurrent Indicators. These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[3:0]# may optionally be used as GPIO Ports [42,41,40,59]. OC# pins are 3.3V and NOT 5 V tolerant. OC# pins must be shared between ports OC#[3:0] can only be used for EHCI controller #1

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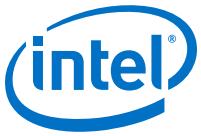
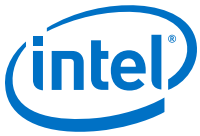


Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
GPIO60	I/O	Native	1	I	SUS		General Purpose I/O Port 60. Not Multiplexed. [3]
SUS_STAT#/ GPIO61	I/O	SUS_STAT#	1	O (High)	SUS		Suspend Status: This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. If SUS_STAT# interface is not used, this signal can be used as a GPIO Port 61.
SUS_CLK/ GPIO62	I/O	SUS_CLK	1	O (Low)	SUS		Suspend Clock. This clock is an output of the RTC generator circuit. It is used by other chips for refresh clock. If SUS_CLK interface is not used, the signals can be used as GPIO Port 62.
SLP_S5#/ GPIO63	I/O	SLP_S5#	1	O (High)	SUS		S5 Sleep Control. SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states. If SLP_S5# interface is not used, the signals can be used as GPIO Port 63.
GPIO72 [4]	I/O	Native	1	I	SUS		General Purpose I/O Port 72. Not Multiplexed. [3]
GPIO73	I/O	Native	1	I	SUS		General Purpose I/O Port 73. Not Multiplexed. [3]
SML1ALERT#/ GPIO74 [2]	I/O	SML1ALERT#	1	I	SUS	When SMBUS: External pull-up required	System Management Link Alert 1. This signal can be connected to an external BMC. External pull-up resistor to VCCSUS3P3 is required. Resistor value should be calculated based on the bus load, refer to the Platform Design Guide. If SML1ALERT# interface is not used, the signals can be used as GPIO Port 74.
SML1DAT/ GPIO75 [2]	I/O	SML1DAT	1	I	SUS	When SMBUS: External pull-up required	System Management Link 1 Data. SMBus link to external BMC. External pull-up required to VCCSUS3P3 is required. Resistor value should be calculated based on the bus load, refer to the Platform Design Guide. If SML1DAT interface is not used, the signals can be used as GPIO Port 75.
TOTAL			67				

1. When this signal is configured as GPO, the output stage is an open drain.
2. When the multiplexed GPIO is used as GPIO functionality, care should be taken to ensure the signal is stable in its inactive state of the native functionality, immediately after reset until it is initialized to GPIO functionality. Multiplexed signals is visible or Intel reserved.

Signal Name	I/O Type	Default Mode	Ball Count	Default Direction and Logic State	Power Well	Internal/ External Resistor Pull-Up/Down	Description
3. For GPIOs where GPIO versus Native Mode is configured using SPI Soft Strap, the corresponding GPIO_USE_SEL bits for these GPIOs have no effect. The GPIO_USE_SEL bits for these GPIOs may change to reflect the Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set. For signals that have Native defaults, these signals must be configured by using SPI Soft Strap. 4. The functionality that is multiplexed with the GPIO may not be used in desktop configuration. 5. In a ME disabled system, GPIO31 may be used as ACPRESENT from the EC.							



Appendix B Error Messages and LED Codes

This appendix describes the progress codes and the corresponding LED codes that are reported by the BIOS. The LED codes are 8-bit quantities and are used as Port 80 codes with the platform Port 80 capturing device. The higher nibble alone is used for a 4-bit LED.

B.1 Port 0x80 Progress Codes

Table 30. Port 0x80 Progress Codes

Description	Port 0x80 Code
SEC Phase	
First POST code after CPU reset	0x01
Microcode load begin	0x02
CRAM initialization begin	0x03
PEI Cache When Disabled	0x04
SEC Core At Power On Begin	0x05
Early CPU initialization during Sec Phase	0x06
Early SB initialization during Sec Phase	0x07
Early NB initialization during Sec Phase	0x08
End Of Sec Phase	0x09
Microcode Not Found	0x0E
Microcode Not Loaded	0x0F
PEI Phase	
PEI Core Initialization	0x10
CPU PEIM Initialization	0x11
NB PEIM Initialization	0x15
SB PEIM Initialization	0x19
Memory Detection PEIM (SPD READ)	0x1D
Memory Detection PEIM (Memory Presence Detect)	0x1E
Memory Detection PEIM (Memory Timing)	0x1F
Memory Detection PEIM (Memory Configuring)	0x20
Memory Detection PEIM (Memory Init)	0x21
Memory Installed	0x31
CPU PEIM (CPU Init)	0x32
CPU PEIM (Cache Init)	0x33

continued...

Description	Port 0x80 Code
CPU PEIM (BSP Select)	0x34
CPU PEIM (AP Init)	0x35
CPU PEIM (CPU SMM Init)	0x36
NB PEIM (Mem_NB_Init)	0x37
SB PEIM (Mem_SB_Init)	0x3B
DXE IPL started	0x4F
DXE Phase	
DXE Core started	0x60
DXE NVRAM Initialization	0x61
SB RUN Initialization	0x62
DXE CPU Initialization	0x63
DXE PCI Host Bridge Initialization	0x68
DXE NB Initialization	0x69
DXE NB SMM Initialization	0x6A
DXE SB Initialization	0x70
DXE SB SMM Initialization	0x71
DXE SB devices Initialization	0x72
DXE ACPI Initialization	0x78
DXE CSM Initialization	0x79
DXE BDS Started	0x90
DXE BDS connect drivers	0x91
DXE PCI Bus begin	0x92
DXE PCI Bus HPC Initialization	0x93
DXE PCI Bus enumeration	0x94
DXE PCI Bus resource requested	0x95
DXE PCI Bus assign resource	0x96
DXE CON_OUT connect	0x97
DXE CON_IN connect	0x98
DXE SIO Initialization	0x99
DXE USB start	0x9A
DXE USB reset	0x9B
DXE USB detect	0x9C
DXE USB enable	0x9D
DXE IDE begin	0xA1
DXE IDE reset	0xA2
DXE IDE detect	0xA3

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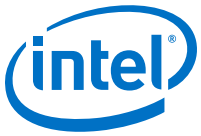


Description	Port 0x80 Code
DXE IDE enable	0xA4
DXE SCSI begin	0xA5
DXE SCSI reset	0xA6
DXE SCSI detect	0xA7
DXE SCSI enable	0xA8
DXE verifying SETUP password	0xA9
DXE SETUP start	0xAB
DXE SETUP input wait	0xAC
DXE Ready to Boot	0xAD
DXE Legacy Boot	0xAE
DXE Exit Boot Services	0xAF
RT Set Virtual Address Map Begin	0xB0
RT Set Virtual Address Map End	0xB1
DXE Legacy Option ROM init	0xB2
DXE Reset system	0xB3
DXE USB Hot plug	0xB4
DXE PCI BUS Hot plug	0xB5
DXE NVRAM cleanup	0xB6
DXE Configuration Reset	0xB7
CSM16	0x00
S3 Resume PEIM (S3 started)	0xE0
S3 Resume PEIM (S3 boot script)	0xE1
S3 Resume PEIM (S3 Video Repost)	0xE2
S3 Resume PEIM (S3 OS wake)	0xE3
PEIM which detected forced Recovery condition	0xF0
PEIM which detected User Recovery condition	0xF1
Recovery PEIM (Recovery started)	0xF2
Recovery PEIM (Capsule found)	0xF3
Recovery PEIM (Capsule loaded)	0xF4

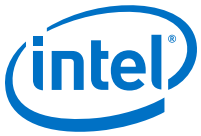
B.2 Port 0x80 Error Codes

Table 31. Port 0x80 Error Codes

Description	Port 0x80 Code
Memory Type Invalid	0x50
Memory Speed Invalid	0x50
Memory SPD failure	0x51

continued...

Description	Port 0x80 Code
Memory Size Invalid	0x52
Memory Mismatch	0x52
Memory not detected	0x53
None of the Memory installed valid	0x53
Memory Error	0x54
Memory not installed	0x55
CPU type invalid	0x56
CPU Speed invalid	0x56
CPU Mismatch	0x57
PEI CPU Self-test failure	0x58
PEI CPU Cache Error	0x58
CPU Microcode Update failure	0x59
No CPU microcode	0x59
PEI CPU internal error	0x5A
PEI CPU error	0x5A
PEI reset not available	0x5B
DXE CPU Error	0xD0
DXE NB Error	0xD1
DXE SB Error	0xD2
DXE Arch Protocol not available	0xD3
Out of resources for PCI device	0xD4
Insufficient space to dispatch legacy option ROM	0xD5
No Console Output device detected	0xD6
No Console Input device detected	0xD7
Invalid Password	0xD8
Error loading the boot option	0xD9
Boot Option failure	0xDA
Flash updated failure	0xDB
DXE reset not available	0xDC
S3 resume memory failure	0xE8
S3 resume PPI not found	0xE9
S3 Boot Script Error	0xEA
S3 OS Wake Vector error	0xEB
Recovery PPI not found	0xF8
Recovery capsule not found	0xF9
Invalid Recovery Capsule	0xFA



B.3 Port 0x80 Error Debug

Table 32. Port 0x80 Error Debug

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.

Appendix C Board Reference Diagrams

Figure 11. Top View

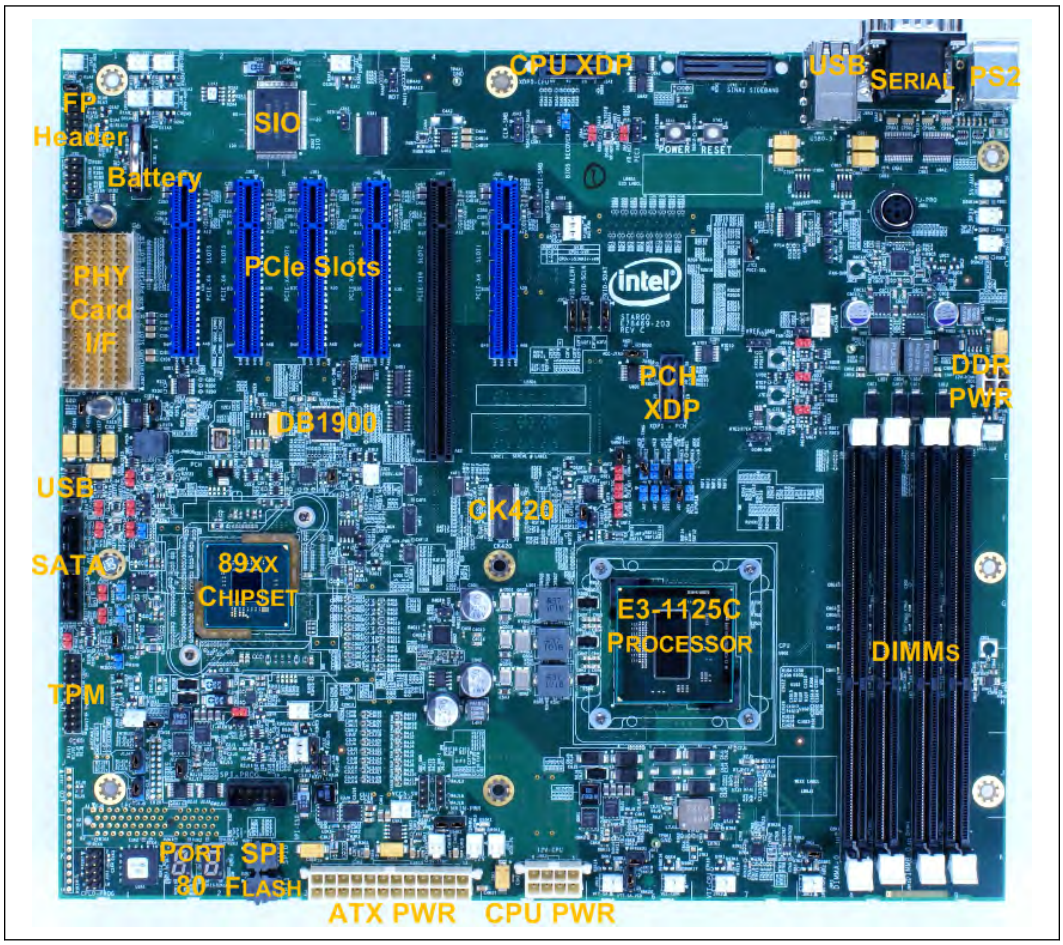


Figure 12. DDR3 Memory Components

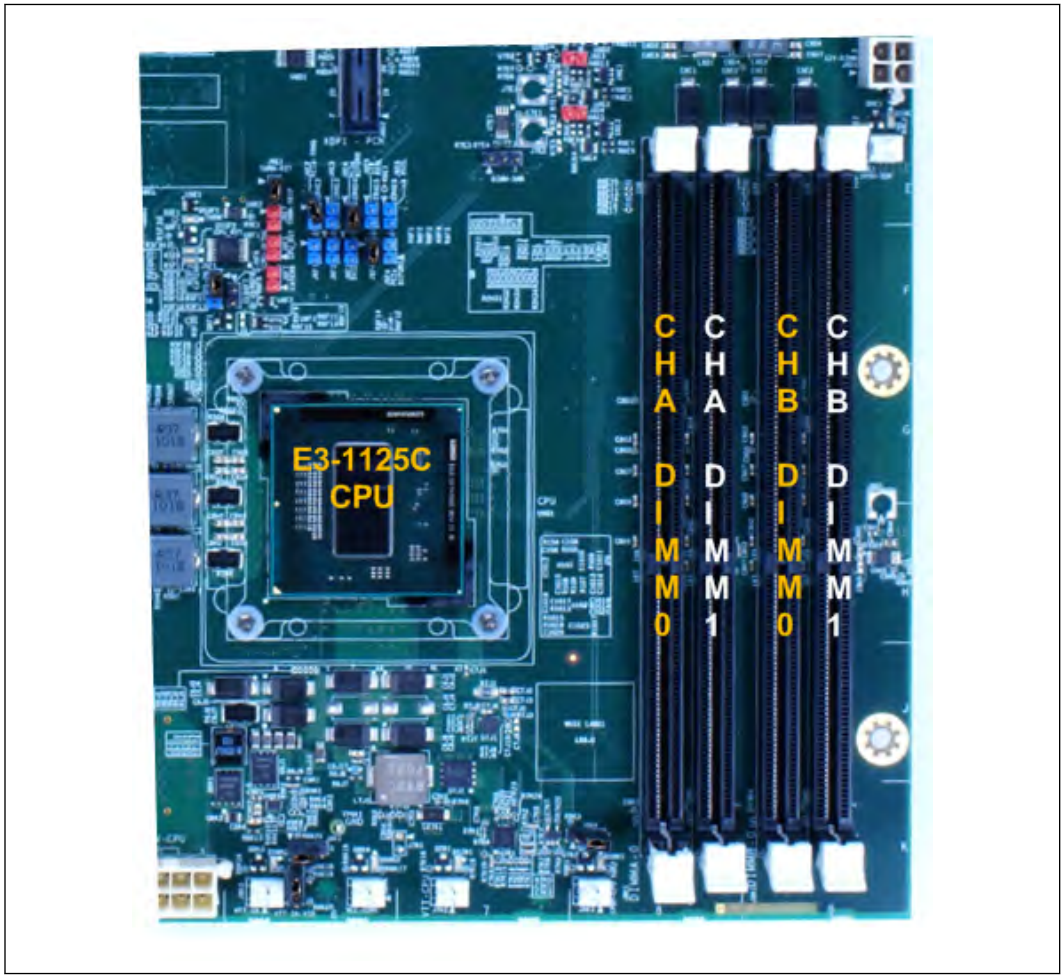


Figure 13. PCIe Slots

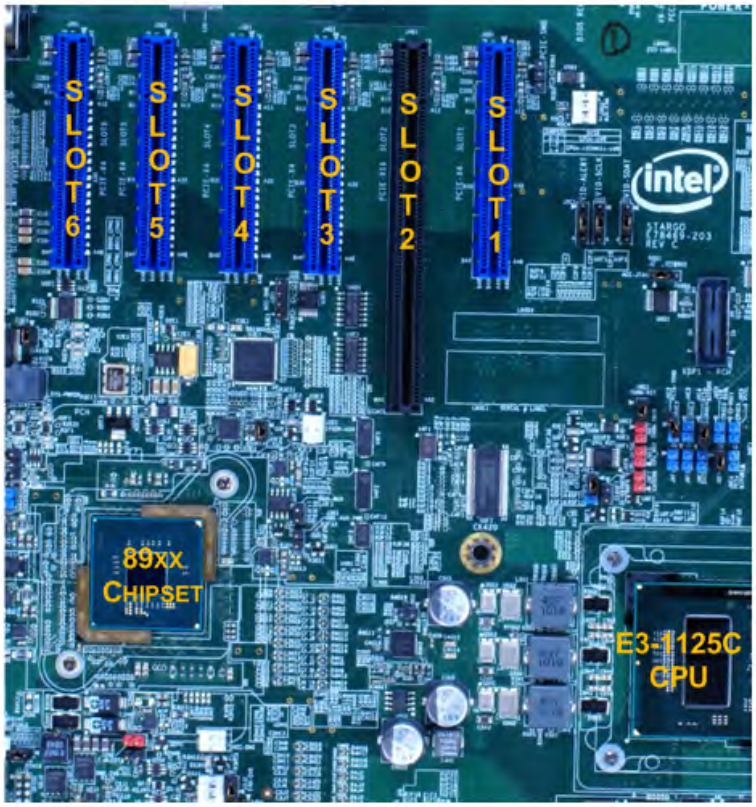


Figure 14. PECI & Thermal Diode Components

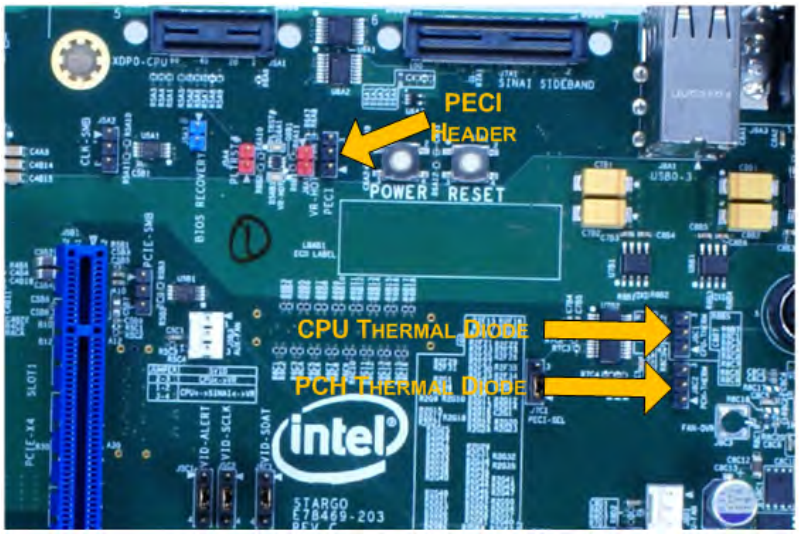


Figure 15. LEDs and Power Button Switches

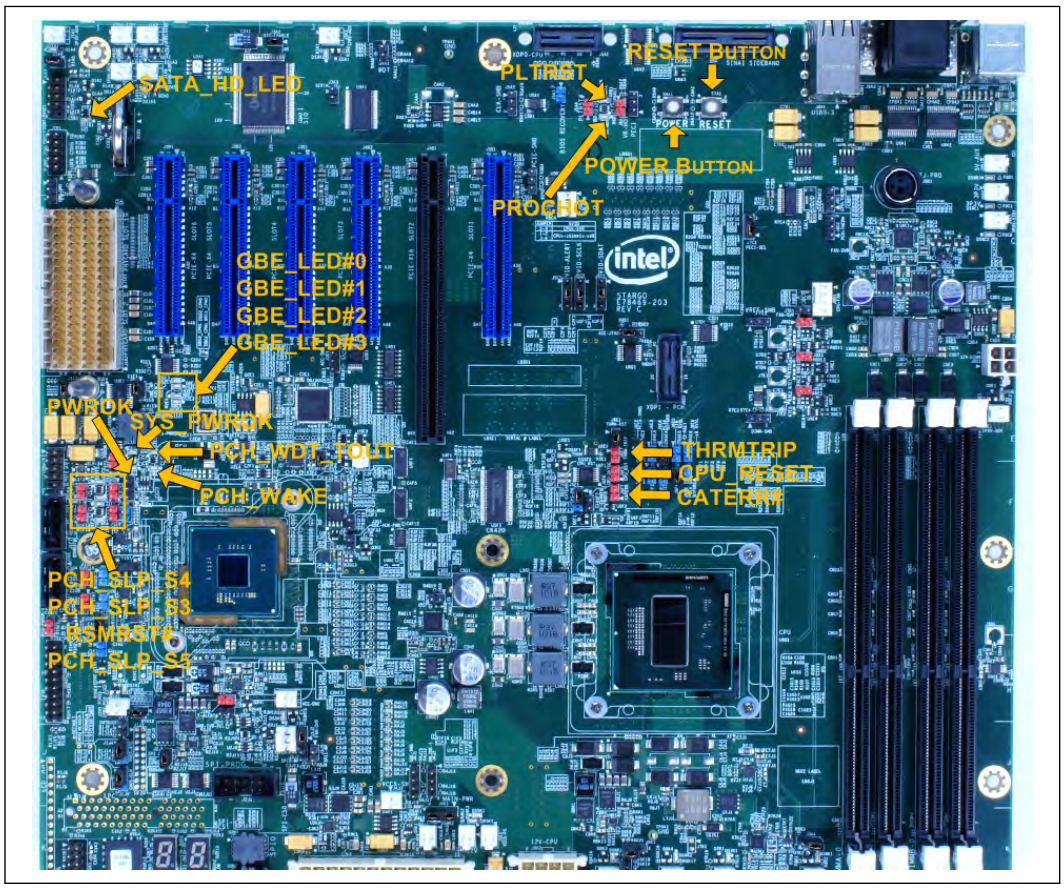


Figure 16. Power Supply Headers

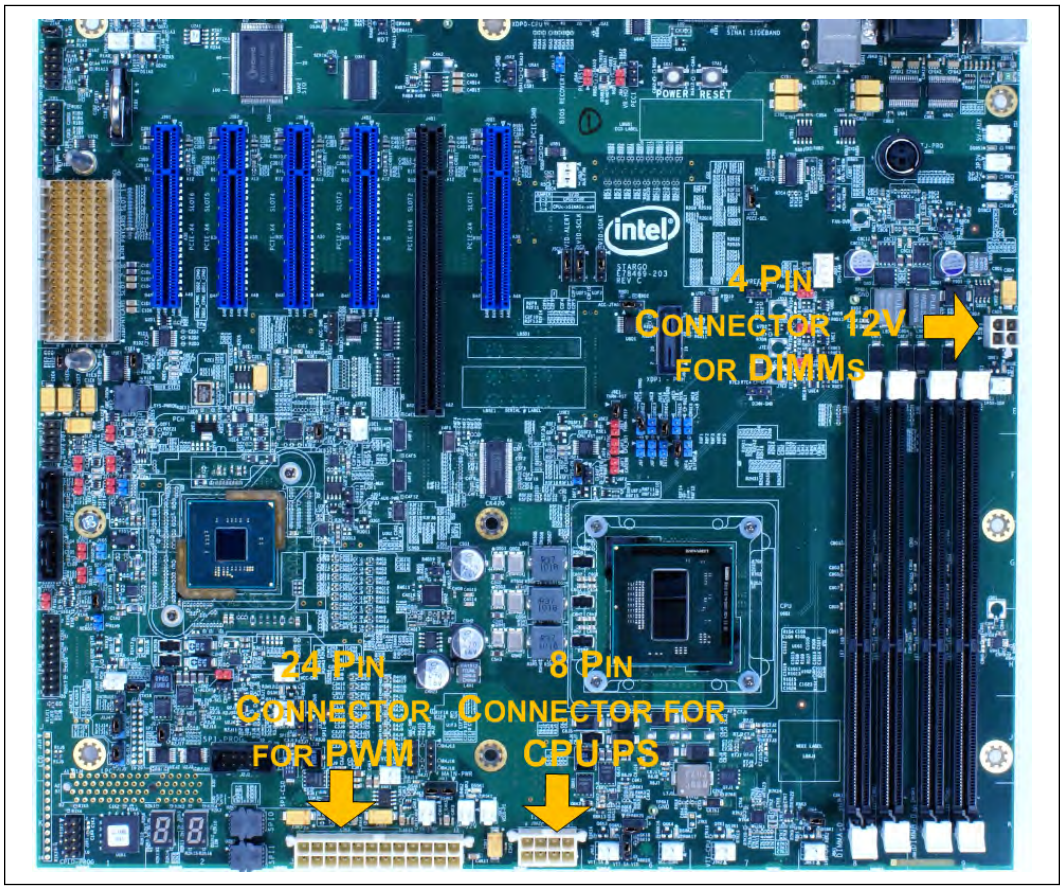


Figure 17. SMBus Headers

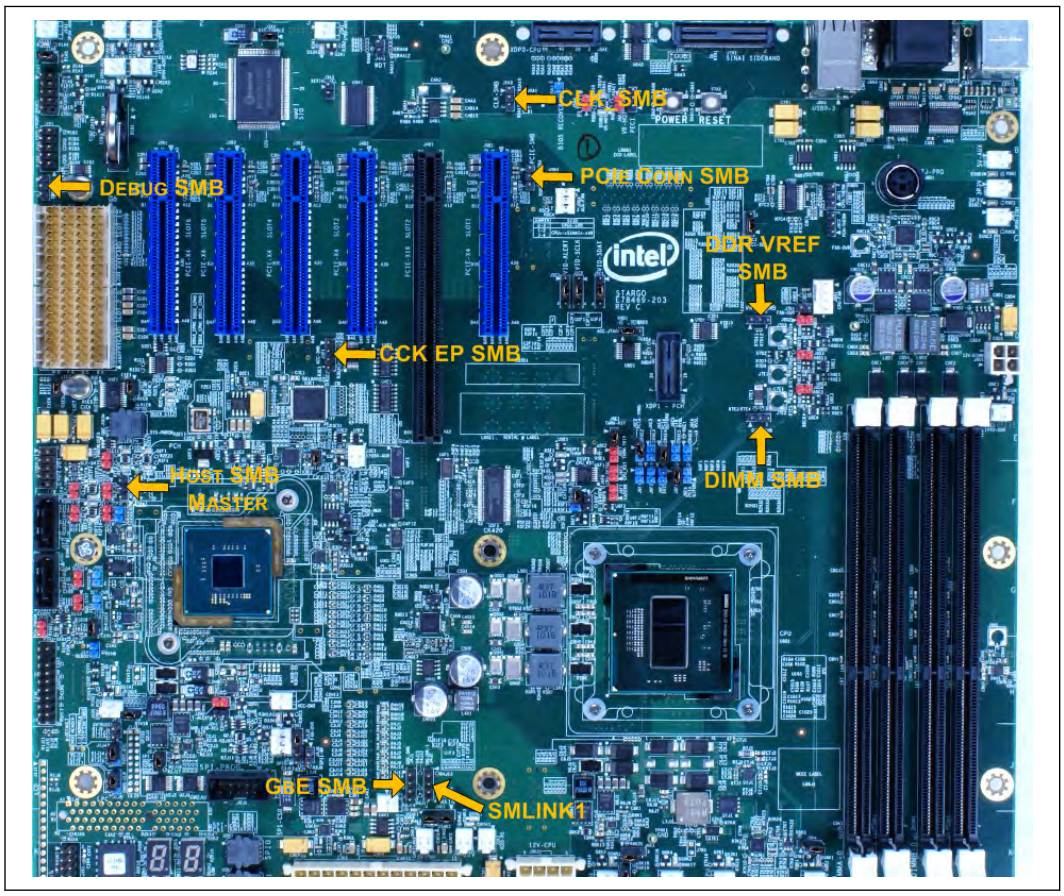


Figure 18. Configuration Jumper Locations (1 of 2)

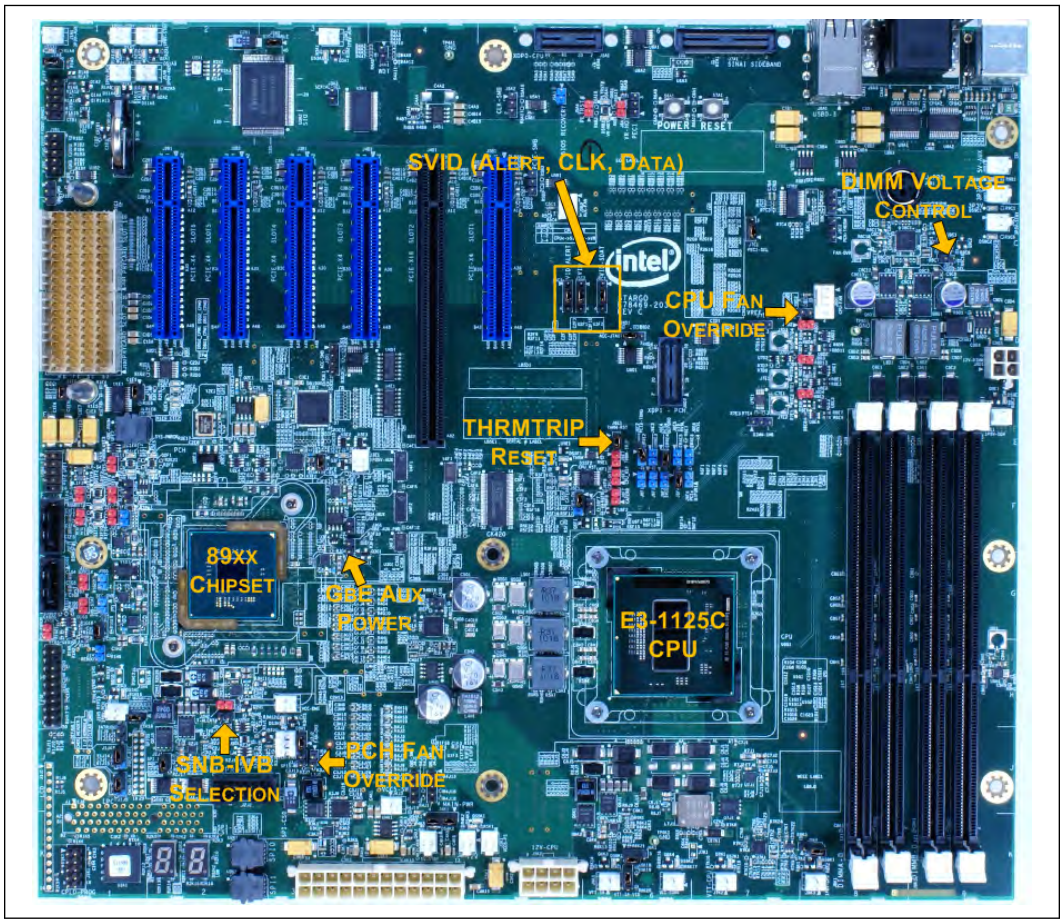


Figure 19. Configuration Jumper Locations (2 of 2)

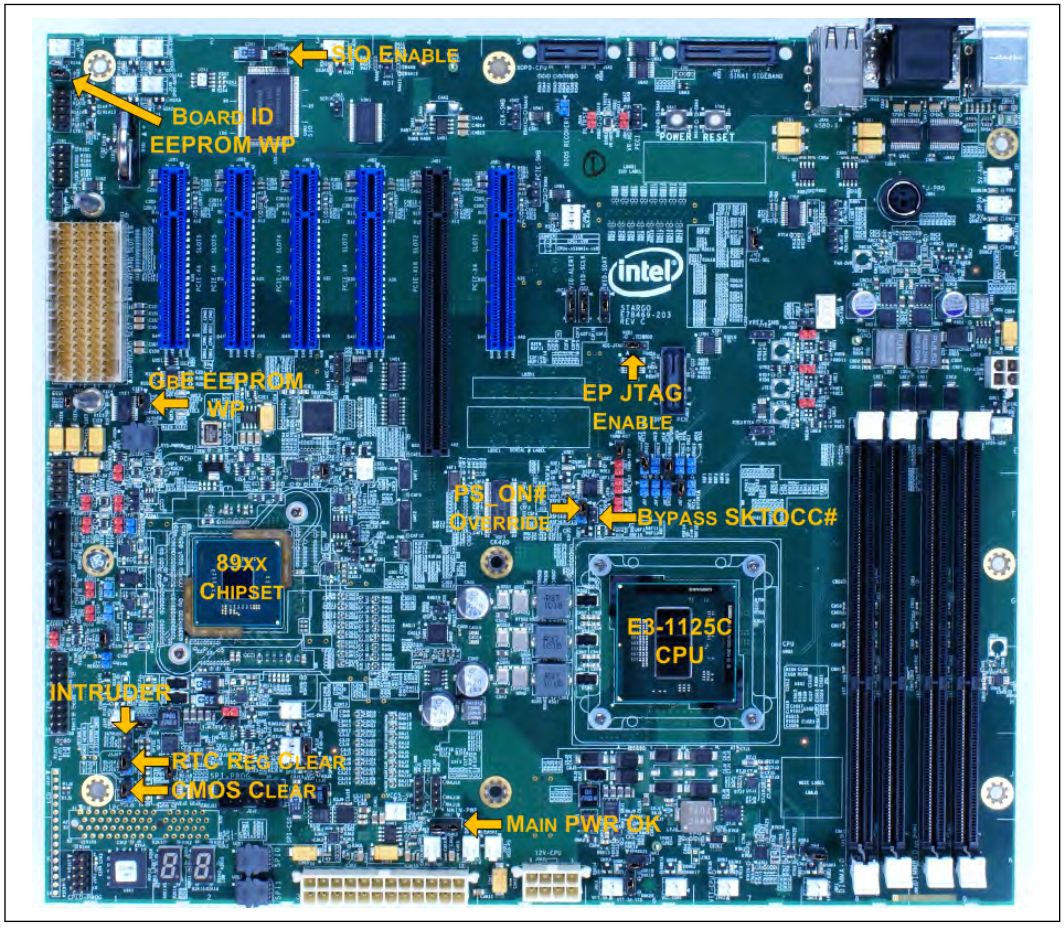


Figure 20. Intel® Communications Chipset 89xx Series Straps

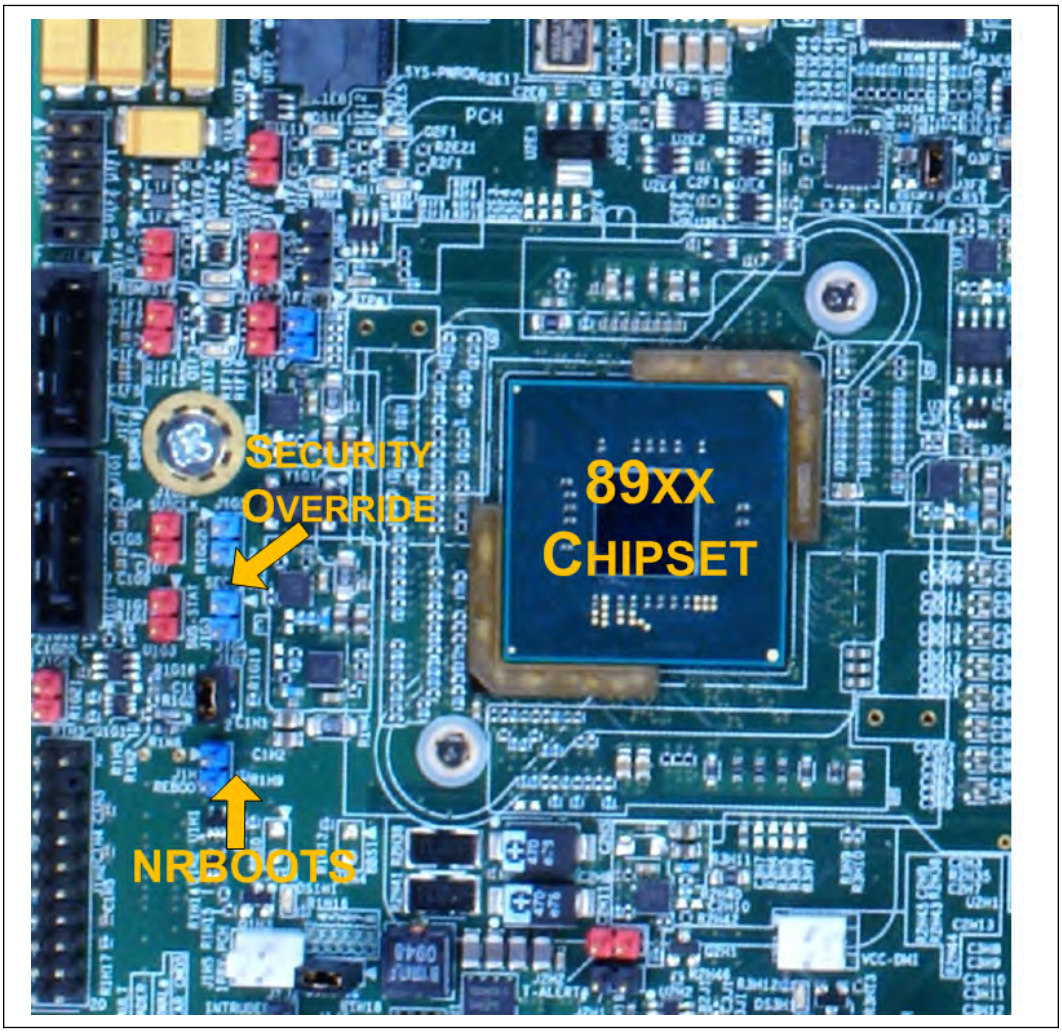


Figure 21. Intel® Xeon® and Intel® Core™ Processor For Communications Infrastructure Straps

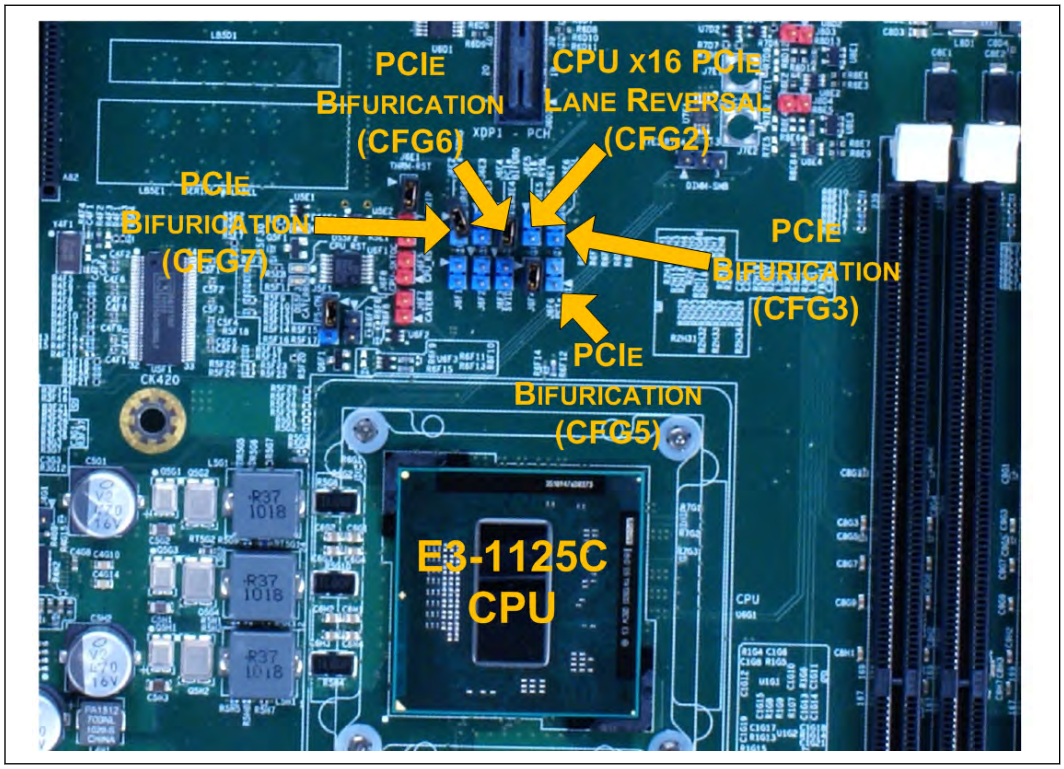


Figure 22. Front Panel