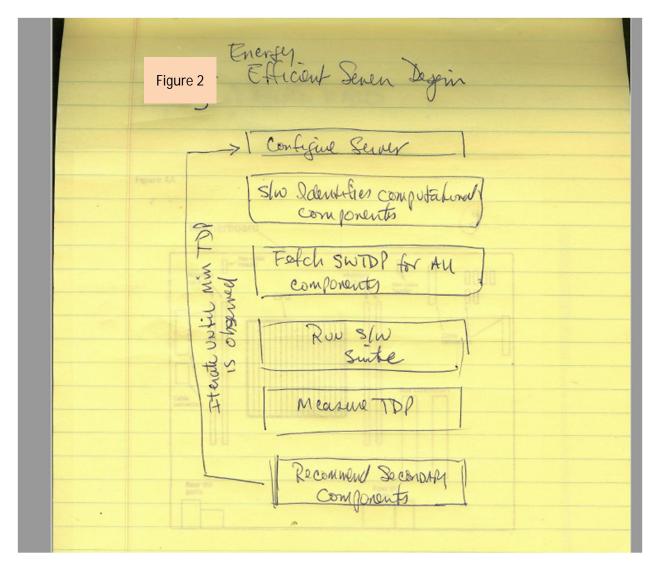


Notice how the curves don't align vertically. That's because we're willing to give up a small percentage of unneeded performance for large increases in efficiency. I tried to draw the curves to indicate less than 10% performance difference. For many applications that are not CPU bound, the actual throughput difference will be neglibilble.

## Figure 2



## Lopoco Provisional Drawings

Figure 4 P Tertin w in the Gyste dist roup dists into routps arrer power meter to MAX if necessary] Fret iting to disk ) N+Z Start wri all thread cores on G paralle ed record max ernined dings

Figure 5A

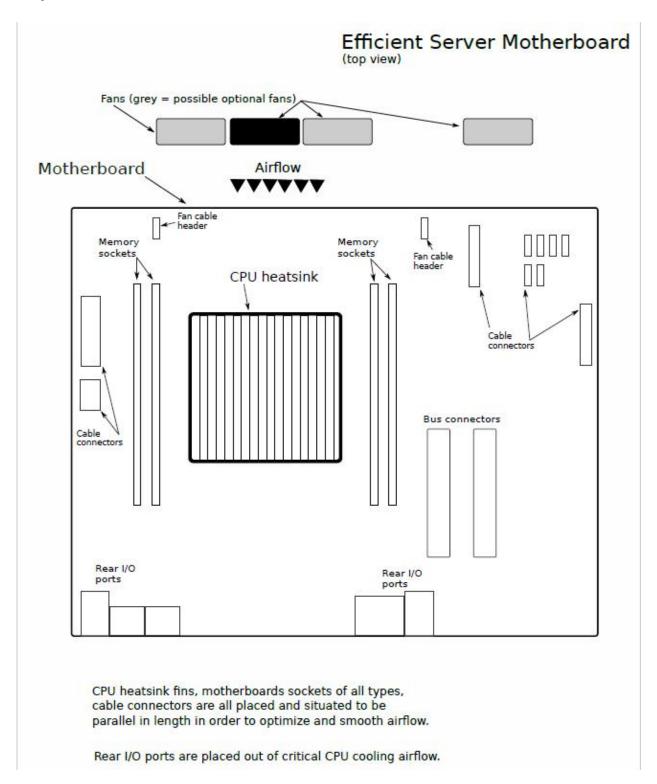
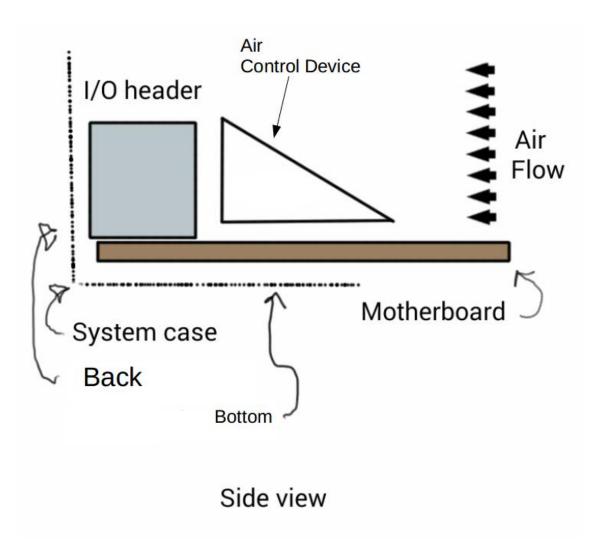
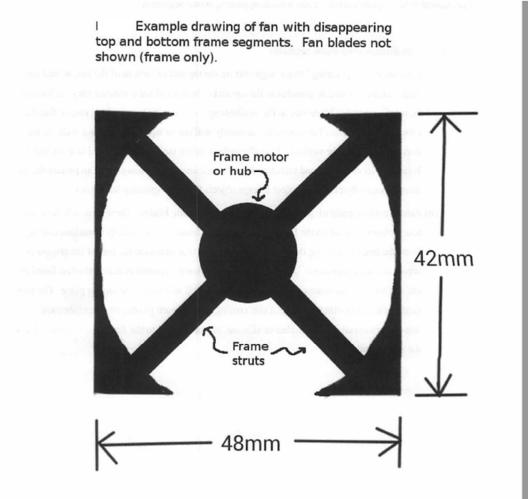
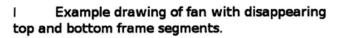


Figure 5B Mother Board Side View Airflow









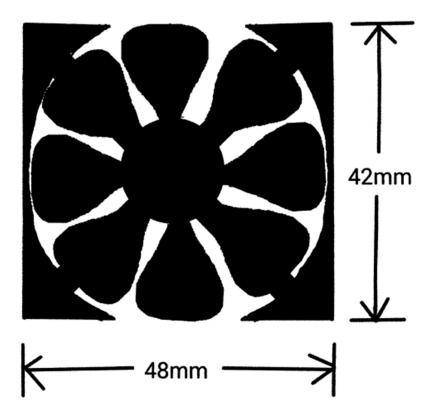


Figure 9

Ultra Efficient Data Conter Design Set 5 Set or mfigura fert results per application lass data center subsections

Figure 8 Vien

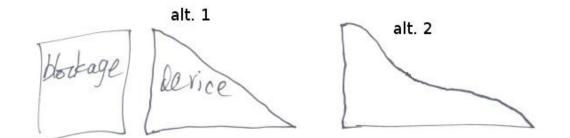


Figure 10

NEW

alt. 1 alt. 2 device blockage

FIGURE 11

## **Ultra-Efficient Data Center**

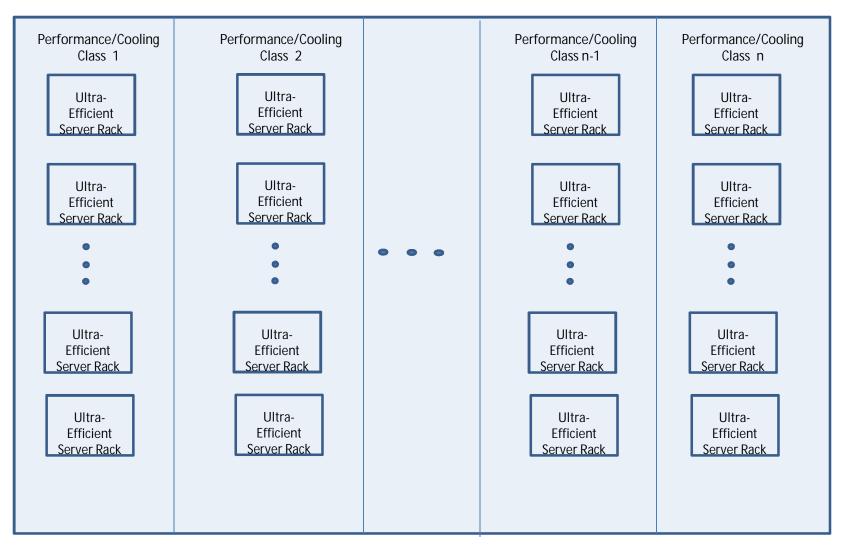


Diagram of Ultra-Efficient Data Center layout showing multiple racks of servers of different performance and cooling classes allowing highly efficient cooling provisioning and application migration based on application computational requirement. Highest performance is Class-1; lowest performance is Class-n.