RM9200 Memory Map

Virtual Space	Region	Size
0000.0000	Reserved	256MB
1000.0000	Local memory (cached)	256MB
2000.0000	Local memory (reserved)	512MB
4000.0000	Marvell memory (cached)	1GB
8000.0000	Local memory	256MB
9000.0000	OCD registers	16K
9000.4000	Reserved	127.9MB
9800.0000	SysAD peripherals	128MB
a000.0000	Local memory	256MB
b000.0000	OCD registers	16KB
b000.4000	Scratch RAM	8KB
b000.6000	Reserved	127.9MB
b800.0000	CF Controller I/O	8MB
b880.0000	CF Controller Memory	8MB
b900.0000	DP83816	8MB
b980.0000	DP83816	8MB
ba00.0000	TXRX Shared Memory	16MB
bb00.0000	FP Shared Memory	16MB
bc00.0000	Marvell registers	64KB
bc04.0000	Marvell SRAM	256KB
bd00.0000	QLogic registers	16MB
be00.0000	Reserved	16MB
bf00.0000	RTC	2MB
bf20.0000	Reserved	2MB
bf40.0000	BM-FPGA	2MB
bf60.0000	Non-boot PROM	2MB
bf80.0000	PROM	8MB
c000.0000	Marvell memory (uncached)	1GB

Physical Space	Region	Size
0000.0000	Local memory	256MB
1000.0000	OCD registers	16KB
1000.4000	Scratch RAM	8KB
1000.6000	Reserved	127.9MB
1800.0000	CF Controller I/O	8MB
1880.0000	CF Controller Memory	8MB
1900.0000	DP83816	8MB
1980.0000	DP83816	8MB
1a00.0000	TXRX Shared Memory	16MB
1b00.0000	FP Shared Memory	16MB
1c00.0000	Marvell registers	64KB
1c04.0000	Marvell SRAM	256KB
1d00.0000	QLogic registers	16MB
1e00.0000	Reserved	16MB
1f00.0000	RTC	2MB
1f20.0000	Reserved	2MB
1f40.0000	BM-FPGA	2MB
1f60.0000	Non-boot PROM	2MB
1f80.0000	PROM	8MB
2000.0000	Local memory	256MB
4000.0000	Marvell memory	1GB
8000.0000	Reserved	2048MB

Region	Virtual	Physical	Size	Region	Path	Notes
Reserved	0000.0000	-	256MB	-	-	
Local memory	1000.0000	2000.0000	256MB	TLB -- cached	SDRAM1	SDRAM2, 3 are reserved
	2000.0000	3000.0000	256MB	TLB -- cached	SDRAM2	
	3000.0000	4000.0000	256MB	TLB -- cached	SDRAM3	
Marvell memory	4000.0000	4000.0000	256MB	TLB -- cached	SysAD1, SCS0	SysAD1 = 1GB
	5000.0000	5000.0000	256MB	TLB -- cached	SysAD1, SCS0	
	6000.0000	6000.0000	256MB	TLB -- cached	SysAD1, SCS1	
	7000.0000	7000.0000	256MB	TLB -- cached	SysAD1, SCS1	
Local memory	8000.0000	0000.0000	256MB	kseg0	SDRAM0	
SysAD peripherals	9800.0000	1800.0000	128MB	kseg0	SysAD2	SysAD2 = 128MB
Local memory	a000.0000	0000.0000	256MB	kseg1	SDRAM0	
OCD registers	b000.0000	1000.0000	16KB	kseg1	Internal	
Scratch RAM	b000.4000	1000.4000	8KB	kseg1	Internal	
CF Controller I/O	b800.0000	1800.0000	8MB	kseg1	SysAD2	PCI Bridge Secondary
CF Controller Memory	b880.0000	1880.0000	8MB	kseg1	SysAD2	PCI Bridge Secondary
DP83816	b900.0000	1900.0000	8MB	kseg1	SysAD2	PCI Bridge Secondary
DP83816	b980.0000	1980.0000	8MB	kseg1	SysAD2	PCI Bridge Secondary
TXRX Shared Memory	ba00.0000	1a00.0000	16MB	kseg1	SysAD2	
FP Shared Memory	bb00.0000	1b00.0000	16MB	kseg1	SysAD2	
Marvell registers	bc00.0000	1c00.0000	64KB	kseg1	SysAD2	
Marvell SRAM	bc04.0000	1c04.0000	256KB	kseg1	SysAD2	
QLogic registers	bd00.0000	1d00.0000	16MB	kseg1	SysAD2	
Reserved	be00.0000	1e00.0000	16MB	kseg1	SysAD2	
RTC	bf00.0000	1f00.0000	2MB	kseg1	SysAD2, CS0	
Reserved	bf20.0000	1f20.0000	2MB	kseg1	SysAD2, CS1	
BM-FPGA	bf40.0000	1f40.0000	2MB	kseg1	SysAD2, CS2	
Non-boot PROM	bf60.0000	1f60.0000	2MB	kseg1	SysAD2, CS3	
PROM	bf80.0000	1f80.0000	8MB	kseg1	SysAD2, Boot CS	
Marvell memory	c000.0000	4000.0000	256MB	TLB -- uncached	SysAD1, SCS0	SysAD1 = 1GB
	d000.0000	5000.0000	256MB	TLB -- uncached	SysAD1, SCS0	
	e000.0000	6000.0000	256MB	TLB -- uncached	SysAD1, SCS1	
	f000.0000	7000.0000	256MB	TLB -- uncached	SysAD1, SCS1	

Notes:
Total memory space of Local Memory is 1GB -- this is divided between 2 regions that are NOT contiguous; also note that the first region is mapped to kseg0 and kseg1 while the other 3 regions are TLB mapped.

Marvell memory space is 1GB -- note that this is also divided between 2 virtual regions that are NOT contiguous; this is not possible since we do not want to locate anything at a virtual address of 0000.0000 and since this space needs to mapped as uncached and cached space through the TLB (which means a total of 2GB of virtual space).

RM9000 allows for 2 SysAD regions (noted as SysAD1 and SysAD2); these regions MUST be aligned to a power of 2.

After reset, Marvell registers are defaulted to base address of b400.0000. SysAD2 must first be set to cover this address and then the default base address must be changed to bc00.0000. Next, SysAD2 must then be set to base of b800.0000 with size of 128MB.

The TXRX and FP SiBytes only allow a 16MB region from PCI.

BEV can be 0 or 1 with this map.

RM9200 Serial Initialization -- populated on Rev 1

Bit	Value	Definition	Settings
0	0	Rsvd	
1	0	preBigEndian	Little Endian
2	0	CohSerial	Parallel coherency
3	0	SAD64Wide	Must be 0
4	0	SADRdOverlap	Read overlap disabled
6:5	10	SADWrProt	Pipelined writes
10:7	0000	SADDatRate	Dd data rate
11	0	CoreIsolate	*Processors not isolated*
12	0	SDRAM32Wide	Must be 0
13	0	MCSglTrkEnbl	Multiple concurrent accesses in MC
14	0	MCInOrder	MC accesses can be reordered
15	1	ScrNoReOrder	Scratch RAM reads in order
16	1	HTDis	Disable HT
17	0	HTLpBack	HT Loopback disabled
18	1	HTIsochHP	Isochronous bit high priority on HT
20:19	00	BootDevWd	8-bit wide boot path
22:21	01	BootType	Boot from SysAD
23	0	NonOvlpXact	Overlap packet buffer transactions
25:24	00	OCDCnfgRsvd	Must be 0
40:26	100000000000000	OCDCnfgAddr	OCB Base Address = 0x1000.0000
42:41	10	preDrvStren	Drive strength is Class II medium high
46:43	0000	SyncSysAD	2:1 sample and drive sync
47	0	SyncHalfSysAD	
51:48	0000	SyncSDRAM	2:1 sample and drive sync
52	0	SyncHalfSDRAM	
60:53	00100000	SemiSBIURatio	3:1 ratio for switch to BIU
68:61	00010000	SemiSHTRatio	2:1 ratio for BIU to HT bus
76:69	00110010	SemiHTLnkRatio	4:3 ratio for HT boundary to HT bus
77	0	Rsvd	
78	0	TimIntdis	Timer enabled on interrupt bit 5
79	0	Timer1X	Timer is normal frequency
81:80	00	SysConfig	User-configurable bits
82	1	OCacheEn	Secondary cached enabled
83	1	OTClrEn	Secondary cache tags cleared on cold reset
84	0	ParChkDis	Parity check enabled processor-wide
85	1	TLB64Ent	64 entry TLB
86	0	HitShrFtch	Send invalidate
87	0	MIPS64Compat	PMC-Sierra compatible CP0
88	0	PowerSave	Power save disabled
92:89	0000	CorePbRsvd	Must be 0

94:93	00	CkPdAlgn	No swing control on MasterClock
95	0	PLLDis	Core PLLs enabled
96	0	preHTPLLDis	HT PLL enabled
97	0	DivMa2BIU	BIU PLL divide by 1
102:98	00100	MulFundBIU	BIU PLL multiplier = 6
107:103	00001	DivXBIU	BIU core clock divisor = 3
112:108	00100	DivXSDRAM	SDRAM clock divisor from BIU clock = 6
117:113	10111	DivXLocBus	LocalBus clock divisor from BIU block = 25
122:118	00100	DivXHTBus	HT clock divisor from BIU block = 6
123	0	DivMa2HT	HT PLL divide by 1
128:124	00100	MulFundHT	HT PLL multiplier = 6
133:129	11111	DivXHTBus	HT PLL divisor = 1
134	0	HTUseHTClk	Use HT ref clock instead of MasterClock
135	0	DivMa2Core	Core PLL divide by 1
140:136	00100	MulFundCore	Core PLL multiplier = 6
145:141	11111	DivXCore	Core PLL divisor = 1
146	0	V2p5Out	Not used
147	0	DbgSESDnEnbl	Disable BIU clocks on system error
148	0	DbgHBeatEnbl	DmaAckOB will indicate valid IOAddr cycle
151:149	010	preScratchSpeed	Set normal memory sense amps
153:152	00	preScratchStart	Early start strobe on scratch memory
154	0	ProcADsbl	Core 0 enabled
155	0	ProcBDsbl	Core 1 enabled
157:156	01	SemiSBIUAdj	Semi-sync boundary adjust for switch to BIU
159:158	00	SemiSHTAdj	Semi-sync boundary adjust for BIU to HT
160	0	FastTest	Fast test mode disabled
161	0	BIUPrRsvd	Reserved
163:162	00	RegFStTime	Start time of all register files
165:164	01	ODataSpeed	Set speed of odata sense amps
167:166	01	OTagSpeed	Set speed of odata sense amps
170:168	100	ShTagSpeed	Set speed of shadow tag sense amps
173:161	010	CDataSpeed	Set speed of ddata and idata sense amps
176:174	100	CTagSpeed	Set speed of dtag and itag sense amps
178:177	00	aPHTSpeed	Set speed of branch predictor senseamps
180:179	11	OTagStart	Set start strobe of otag
182:181	00	ODataStart	Set start strobe of odata
184:183	11	ShTagStart	Set start strobe of shadow tag
186:185	11	DCTagStart	Set start strobe of dtag
188:187	11	DCDataStart	Set start strobe of ddata
190:189	00	ICTagStart	Set start strobe of itag
192:191	00	ICDataStar	Set start strobe of idata
194:193	00	aPHTStart	Set start strobe of branch predictor
196:195	00	CorePrRsvd	Reserved

200:197	0000	PLLAlign	Align MasterClock and internal ph1 clock
201	1	PLLVCOCap	PLL Frequency Doubler enabled
202	0	PLLVCOSw	PLL control mode bit
204:203	00	PLLVCOI	Adjust PLL Center Frequency
206:205	10	PLLCMV	PLL control mode bits
208:207	00	ClockPrRsvd	Reserved
215:209	0000000	None1	Reserved
223:216	00000000	None2	Reserved
231:224	00000000	None3	Reserved
239:232	00000000	None4	Reserved
247:240	00000000	None5	Reserved
255:248	00000000	None6	Reserved

RM9200A Serial Initialization -- populated on Rev 2 and higher

Bit	Value	Definition	Settings
0	0	Rsvd	Must be 0
1	0	Rsvd	Must be 0
2	0	Rsvd	Must be 0
3	0	Rsvd	Must be 0
4	0	LBParEnable	Enable local bus parity
6:5	00	GDICkAlign	Align the GDI Early clock
8:7	00	GDIRcSyncDist	Set the GDI read to write pointer receive
10:9	00	GDIXtSyncDist	Set the GDI Dist read to write pointer transmit
18:11	00000000	GDISyncCtl	Set the GDI clock relationship
19	0	GDIReOrder	GDI transactions cannot be reordered
20	1	EnSysAD	Enable the SysAD interface, disable GigE
21	0	PciRstInputOnly	Reset pin is open-drain (n/a)
22	0	PciDlyTranOff	Enable PCI delay transaction buffer
26:23	0000	PciClkRatio	Set the BIU to PCI clock ratio
27	0	PciInOrder	Force all PCI transactions in order
28	0	PciEnWrMrge	Disable PCI write merging capability
30:29	00	PciDrvStren	Drive strength control for PCI
31	0	PciArbtrDsbl	Disable the on-chip PCI arbiter
32	0	preBigEndian	Little Endian
33	0	CohSerial	Parallel coherency
34	0	SAD64Wide	Must be 0
35	0	SADRdOverlap	Read overlap disabled
37:36	10	SADWrProt	Pipelined writes
41:38	0000	SADDatRate	Dd data rate
42	0	CoreIsolate	*Processors not isolated*

43	0	SDRAM32Wide	Must be 0
44	0	MCSglTrkEnbl	Multiple concurrent accesses in MC
45	0	MCInOrder	MC accesses can be reordered
46	1	ScrNoReOrder	Scratch RAM reads in order
47	1	HTDis	Disable HT
48	0	HTLpBack	HT Loopback disabled
49	1	HTIsochHP	Isochronous bit high priority on HT
51:50	00	BootDevWd	8-bit wide boot path
53:52	01	BootType	Boot from SysAD
54	0	NonOvlpXact	Overlap packet buffer transactions
56:55	00	OCDCnfgRsvd	Must be 0
71:57	100000000000000	OCDCnfgAddr	OCB Base Address = 0x1000.0000
73:72	10	preDrvStren	Drive strength is Class II medium high
77:74	0000	SyncSysAD	2:1 sample and drive sync
78	0	SyncHalfSysAD	
82:79	0000	SyncSDRAM	2:1 sample and drive sync
83	0	SyncHalfSDRAM	
91:84	00100000	SemiSBIURatio	3:1 ratio for switch to BIU
99:92	00010000	SemiSHTRatio	2:1 ratio for BIU to HT bus
107:100	00110010	SemiHTLnkRatio	4:3 ratio for HT boundary to HT bus
108	0	Rsvd	
109	0	TimIntdis	Timer enabled on interrupt bit 5
110	0	Timer1X	Timer is normal frequency
112:111	00	SysConfig	User-configurable bits
113	1	OCacheEn	Secondary cached enabled
114	1	OTClrEn	Secondary cache tags cleared on cold reset
115	0	ParChkDis	Parity check enabled processor-wide
116	1	TLB64Ent	64 entry TLB
117	0	HitShrFtch	Send invalidate
118	0	MIPS64Compat	PMC-Sierra compatible CP0
119	0	PowerSave	Power save disabled
123:120	0000	CorePbRsvd	Must be 0
125:124	00	ClkReserved	Must be 0
126	0	PLLTF	Must be 0
127	0	PLLVI	Must be 0
129:128	00	CkPdAlgn	No swing control on MasterClock
130	0	PLLDis	Core PLLs enabled
131	0	preHTPLLDis	HT PLL enabled
132	0	DivMa2BIU	BIU PLL divide by 1
137:133	00100	MulFundBIU	BIU PLL multiplier = 6
142:138	00001	DivXBIU	BIU core clock divisor = 3
147:143	00100	DivXSDRAM	SDRAM clock divisor from BIU clock = 6
152:148	10111	DivXLocBus	LocalBus clock divisor from BIU block = 25

157:153	00100	DivXHTBus	HT clock divisor from BIU block = 6
158	0	DivMa2HT	HT PLL divide by 1
163:159	00100	MulFundHT	HT PLL multiplier = 6
168:164	11111	DivXHTBus	HT PLL divisor = 1
169	0	HTUseHTClk	Use HT ref clock instead of MasterClock
170	0	DivMa2Core	Core PLL divide by 1
175:171	00100	MulFundCore	Core PLL multiplier = 6
180:176	11111	DivXCore	Core PLL divisor = 1
181	0	PciArbtrDbg	Must be 0
182	0	V2p5Out	Not used
183	0	DbgSESDnEnbl	Disable BIU clocks on system error
184	0	DbgHBeatEnbl	DmaAckOB will indicate valid IOAddr cycle
187:185	010	preScratchSpeed	Set normal memory sense amps
189:188	00	preScratchStart	Early start strobe on scratch memory
190	0	ProcADsbl	Core 0 enabled
191	0	ProcBDsbl	Core 1 enabled
193:192	01	SemiSBIUAdj	Semi-sync boundary adjust for switch to BIU
195:194	00	SemiSHTAdj	Semi-sync boundary adjust for BIU to HT
196	0	FastTest	Fast test mode disabled
197	0	FastTimeOut	Must be 0
199:198	00	RegFStTime	Start time of all register files
201:200	01	ODataSpeed	Set speed of odata sense amps
203:202	01	OTagSpeed	Set speed of odata sense amps
206:204	100	ShTagSpeed	Set speed of shadow tag sense amps
209:207	010	CDataSpeed	Set speed of ddata and idata sense amps
212:210	100	CTagSpeed	Set speed of dtag and itag sense amps
214:213	00	aPHTSpeed	Set speed of branch predictor senseamps
216:215	11	OTagStart	Set start strobe of otag
218:217	00	ODataStart	Set start strobe of odata
220:219	11	ShTagStart	Set start strobe of shadow tag
222:221	11	DCTagStart	Set start strobe of dtag
224:223	11	DCDataStart	Set start strobe of ddata
226:225	00	ICTagStart	Set start strobe of itag
228:227	00	ICDataStar	Set start strobe of idata
230:229	00	aPHTStart	Set start strobe of branch predictor
232:231	00	CorePrRsvd	Reserved
234:233	00	PLLSCP	Must be 0
238:235	0000	PLLAlign	Align MasterClock and internal ph1 clock
239	1	PLLVCOCap	PLL Frequency Doubler enabled
240	0	PLLVCOSw	PLL control mode bit
242:241	00	PLLVCOI	Adjust PLL Center Frequency
244:243	10	PLLCMV	PLL control mode bits
245	1	HTPLLVCOCap	HT PLL Frequency Doubler

246	0	HTPLLVCOSw	PLL control mode bit
248:247	00	HTPLLVCOI	Adjust PLL Center Frequency
250:249	00	HTPLLCMV	PLL control mode bits
251	0	HTBypShftDiv	HT Bypassing 90 degree shifter divide
255:252	0000	PCIPLLAlign	Feedback clock delay

	133MHz Master, 133MHz SysAD, 333MHz BIU, 167MHz SDRAM, 1GHz core	
SyncSysAD	2.5:1	0011
SyncHalfSysAD		1
SyncSDRAM	2:1	0000
SyncHalfSDRAM		0
SemiSBIURatio	3:1	00100000
SemiSHTRatio	2:1	00010000
SemiHTLnkRatio		
DivMa2BIU	1	0
MulFundBIU	10	01000
DivXBIU	4	00010
DivXSDRAM	8	00110
DivXLocBus	25	10111
DivXHTBus	8	00110
DivMa2HT	0	0
MulFundHT	3	00001
DivXHTBus	2	00000
HTUseHTClk		
DivMa2Core	2	1
MulFundCore	15	01101
DivXCore	1	11111

OCD Registers **Base address = 0xb000.0000**

Register	Offset	Value	Description
LKB0 High (OCD)	0x0038	0x01000000	Base address of OCD = 0x1000.0000
LKB0 Low (OCD)	0x0100	0x01000001	Base address of OCD = 0x1000.0000
LKM0	0x0104	0x00000100	OCD Size = 16KB (fixed)
LKB1 (SDRAM0)	0x0108	0x00000001	Base address = 0x0000.0000
LKM1	0x010c	0x00ffff00	Size = 256MB
LKB2 (SDRAM1)	0x0110	0x02000001	Base address = 0x2000.0000
LKM2	0x0114	0x00ffff00	Size = 256MB
LKB3 (SDRAM2)	0x0118	0x03000001	Base address = 0x3000.0000
LKM3	0x011c	0x00ffff00	Size = 256MB
LKB4 (SDRAM3)	0x0120	0x04000001	Base address = 0x4000.0000
LKM4	0x0124	0x00ffff00	Size = 256MB
LKB5 (SysAD1)	0x0128	0x05000001	Base address = 0x5000.0000
LKM5	0x012c	0x03FFFF00	Size = 1GB
LKB6 (SysAD2)	0x0130	0x01800000	Base address = 0x1800.0000
LKM6	0x0134	0x007fff00	Size = 128MB
LKB13 (Scratch)	0x0168	0x01000401	Base address = 0x1000.4000
LKM13	0x016c	0x00000100	Size = 8KB (fixed)
SDCFG	0x0300	0x000302d9	Set drive strength; initially disable ECC
SDMW	0x0304	0x00000000	Default settings initially
SDM0	0x0340	0x00004045	Enable 1GB SDRAM with x8 chips; initially disable ECC
SDT0	0x0344	0x002f9482	Initial timing parameters; these should be derived from DIMM SEEP
SDM1	0x0350	0x00004045	Enable 1GB SDRAM with x8 chips; initially disable ECC
SDT1	0x0354	0x002f9482	Initial timing parameters; these should be derived from DIMM SEEP
SDM2	0x0360	0x00004045	Enable 1GB SDRAM with x8 chips; initially disable ECC
SDT2	0x0364	0x002f9482	Initial timing parameters; these should be derived from DIMM SEEP
SDM3	0x0370	0x00004045	Enable 1GB SDRAM with x8 chips; initially disable ECC
SDT3	0x0374	0x002f9482	Initial timing parameters; these will eventually be derived from DIMM SEEP

Marvell Registers **Base Address = 0xbc00.0000**

Register	Offset	Value	Description
CPU Configuration	0x0000	0x00821000	Various config
CPU Mode	0x0120		Read-only
CPU Pads Cal	0x03b4		Read-only
Internal Space Base	0x0068	0x01001c00	Base address = 1c00.0000; remapped from default 0x1400.0000
SRAM Base	0x0268	0x00001c04	Base address = 1c04.0000; must be aligned to 256KB boundary
Base Address Enable	0x0278	0x00043a00	Enable various base addresses
Reset Sample	0x03c4		Read-only
Reset Sample (high)	0x03d4		Read-only
CS0 Base	0x0008	0x00005000	Base address = 0x5000.0000
CS0 Size	0x0010	0x00001fff	Size = 512MB
CS1 Base	0x0208	0x00007000	Base address = 0x7000.0000
CS1 Size	0x0210	0x00001fff	Size = 512MB
CS2 Base	0x0018	0x00000000	Disabled
CS2 Size	0x0020	0x00000000	
CS3 Base	0x0218	0x00000000	Disabled
CS3 Size	0x0220	0x00000000	
DevCS0 Base	0x0028	0x00001f00	Base address = 0x1f00.0000
DevCS0 Size	0x0030	0x0000001f	Size = 2MB
DevCS1 Base	0x0228	0x00001f20	Base address = 0x1f20.0000
DevCS1 Size	0x0230	0x0000001f	Size = 2MB
DevCS2 Base	0x0248	0x00001f40	Base address = 0x1f40.0000
DevCS2 Size	0x0250	0x0000001f	Size = 2MB
DevCS3 Base	0x0038	0x00001f60	Base address = 0x1f60.0000
DevCS3 Size	0x0040	0x0000001f	Size = 2MB
BootCS Base	0x0238	0x00001f80	Base address = 0x1f80.0000
BootCS Size	0x0240	0x0000007f	Size = 8MB
PCI0 I/O Base	0x0048	0x00000000	Disabled
PCI0 I/O Size	0x0050	0x00000000	
PCI0 Memory 0 Base	0x0058	0x00001d00	Base address = 0x1d00.0000
PCI0 Memory 0 Size	0x0060	0x000000ff	Size = 16MB

PCI0 Memory 1 Base	0x0080	0x00000000	Disabled
PCI0 Memory 1 Size	0x0088	0x00000000	
PCI0 Memory 2 Base	0x0258	0x00000000	Disabled
PCI0 Memory 2 Size	0x0260	0x00000000	
PCI0 Memory 3 Base	0x0280	0x00000000	Disabled
PCI0 Memory 3 Size	0x0288	0x00000000	
PCI1 I/O Base	0x0090	0x00001800	Base address = 0x1800.0000
PCI1 I/O Size	0x0098	0x0000007f	Size = 8MB
PCI1 Memory 0 Base	0x00a0	0x00001a00	Base address = 0x1a00.0000
PCI1 Memory 0 Size	0x00a8	0x000001ff	Size = 32MB
PCI1 Memory 1 Base	0x00b0	0x00001900	Base address = 0x1900.0000
PCI1 Memory 1 Size	0x00b8	0x000000ff	Size = 16MB
PCI1 Memory 2 Base	0x02a0	0x00001880	Base address = 0x1880.0000
PCI1 Memory 2 Size	0x02a8	0x0000001f	Size = 8MB
PCI1 Memory 3 Base	0x02b0	0x00000000	Disabled
PCI1 Memory 3 Size	0x02b8	0x00000000	
PCI Remap			PCI1 I/O remapped to 0; PCI1 Mem 2 remapped to 0x0080.0000
Headers Retarget			Not implemented
CPU Access Protection			Not implemented
Sync Barrier			Not implemented
CPU Interface Crossbar			Default values
SRAM			Default values; eventually enable ECC
SDRAM Configuration	0x1400	0x58220400	Initially disable ECC
Dunit Control (Low)	0x1404	0xc3000541	Default values -- may need to tune
Dunit Control (High)	0x1424	0x0300f777	Default values -- reserved for Marvell usage
DDR Timing (Low)	0x1408	0x01511220	Can probably shorten some of these values
DDR Timing (High)	0x140c	0x00000009	
SDRAM Addr Control	0x1410	0x00000012	512Mbit SDRAM devices
SDRAM Open Pages	0x1414	0x00000000	Leave page open whenever possible
SDRAM Operation	0x1418	0x00000000	Write 0x00000003 after setting SDRAM Mode; then write 0x00000000
SDRAM Mode	0x141c	0x00000062	CL=2.5; BL=4
SDRAM Extended Mode	0x1420	0x00000000	Default settings
SDRAM Crossbar			Default settings

SDRAM Pads Cal			Default settings
SDRAM Error			Default settings; initially disable ECC
SDRAM CDL			Default settings
Device Bank0	0x045c	0xf009e6f7	Various timing parameters
Device Bank1	0x0460	0x146fffff	Various timing parameters
Device Bank2	0x0464	0xf226e87f	Various timing parameters
Device Bank3	0x0468	0x1449e6f0	Various timing parameters
Device Boot	0x046c	0x1449e6f0	Various timing parameters
Device Control	0x04c0	0x0005ffff	
Device Crossbar			Default values
Device Interrupt			Default values
Device Error			Default values
PCI CS0 BAR Size	0xc08, 0xc88	0x1ffff000	512MB
PCI CS1 BAR Size	0xd08, 0xd88	0x1ffff000	512MB
PCI CS2 BAR Size	0xc0c, 0xc8c	0x00000000	Disabled
PCI CS3 BAR Size	0xd0c, 0xd8c	0x00000000	Disabled
DevCS0 BAR Size	0xc10, 0xc90	0x00000000	Disabled
DevCS1 BAR Size	0xd10, 0xd90	0x00000000	Disabled
DevCS2 BAR Size	0xd18, 0xd98	0x00000000, 0x001ff000	Disabled from PCI0, 2MB on PCI1
DevCS3 BAR Size	0xc14, 0xc94	0x00000000	Disabled
BootCS BAR Size	0xd14, 0xd95	0x00000000	Disabled
P2P Mem0 BAR Size	0xd1c, 0xd9c	0x00000000	Disabled
P2P Mem0 BAR Size	0xd20, 0xda0	0x00000000	Disabled

P2P I/O BAR Size	0xd24, 0xda4	0x00000000	Disabled
SRAM BAR Size	0xe00, 0xe80	0x00000000	Disabled
Expansion ROM BAR Size	0xd2c, 0xdac	0x00000000	Disabled
Base Address Enable	0xd2c, 0xdac	0xffff7ff0, 0xffff7db0	Enable SRAM and CS windows on PCI0, enable SRAM, CS, and DevCS2 windows on PCI1
CS0 Remap	0xc48, 0xcc8	0x50000000	
CS1 Remap	0xd48, 0xdc8	0x70000000	
CS2 Remap	0xc4c, 0xccc	0x00000000	
CS3 Remap	0xd4c, 0xdcc	0x00000000	
Other Remaps			Automatically set to base address -- no remap necessary
DRAM BAR Select	0xc1c, 0xc9c	0x000000e8	Default value
PCI Address Decode	0xd3c, 0xdbc	0x00000008	Default value
Headers Retarget			Not implemented
PCI Command	0xc00, 0xc80	0x0107e371	Swapping, combining, multiple reads, etc.
PCI Retry	0xc04, 0xc84	0x00400000	Retry counter = 64
PCI Discard	0xd04, 0xd84	0x0000ffff	Disard timer
MSI Trigger	0xc38, 0xcb8	0x0000ffff	Default value
PCI Arbiter Control	0x1d00, 0x1d80	0x8000030	Enable PCI arbiter
PCI Crossbar			Default values
PCI P2P Config	0x1d94	0x00010000	Bus number = 1, dev number = 0 for PCI1
PCI Access Control			Default values
Config Registers			See spec; must set CS0:3, DevCS2, SRAM BAR
Error Registers			See spec

Messaging Registers			Not currently implemented
GigE PHY Address	0x2000	0x00000000	No PHYs connected
Base Address 0	0x2200	0x50000e00	CS0 enabled
Base Address 1	0x2208	0x70000d00	CS1 enabled
Base Address 2	0x2210	0x00000000	Disabled
Base Address 3	0x2218	0x00000000	Disabled
Base Address 4	0x2220	0x00000002	Disabled
Base Address 5	0x2228	0x00000000	Disabled
Size 0	0x2204	0x1fff0000	512MB
Size 1	0x220c	0x1fff0000	512MB
Size 2	0x2214	0x00000000	Disabled
Size 3	0x221c	0x00000000	Disabled
Size 4	0x2224	0x00000000	Disabled
Size 5	0x222c	0x00000000	Disabled
Base Address Enabled	0x2290	0x0000003c	Enable 0 and 1
Headers Retarget			Not implemented
Access Control	0x2294, 0x2298, 0x229c	0x00000fff	Default values; full access
Ethernet DFCDL			Default values
Port Config	0x2400, 0x2800, 0x2c00	0x00000000	Default values
Port Serial Control	0x243c, 0x283c, 0x2c3c	0x00ea061b	
Various Port Control			Default values; need to eventually set some of these (i.e. MAC address)
Comm Unit			Same as eval board for now; UART ports
Baud Rate Generator 0	xb200	0x002100d7	133MHz in; 9600 baud -- this is different than the eval board since that has 100MHz in
		0x00210023	133MHz in; 57600 baud -- this is different than the eval board since that has 100MHz in

IDMA			Not implemented; initially default values
XOR			Not implemented; initially default values
Timers/Counters			Default values for now; use as needed
Watchdog			Not used on Bobcat
I2C			Same as Disco 1
GPP Control	0xf100	0xffe55515	1 = output; 0 = input
GPP Level Control	0xf110	0x00000000	default value; active high inputs
GPP Value	0xf104	0x00000000	bits 31:27 and 24:21 control LEDs -- write a '1'
Interrupt Cause Low	0x0004		Read-only
Interrupt Cause High	0x000c		Read-only
CPU_Int[0] Mask Low	0x0014	0x00000000	Initially disable interrupts; will eventually want to enable various ECC errors here
CPU_Int[0] Mask High	0x000c	0x00000000	Initially disable interrupts; will eventually want GbE and SDMA interrupts here
CPU_Int[1] Mask Low	0x0034	0x00000000	Initially disable interrupts
CPU_Int[1] Mask High	0x0044	0x00000000	Initially disable interrupts
MPP Control0	0xf000	0x00111111	Set-up GPP pins (GPIO, arbiter, UART, etc.)
MPP Control1	0xf004	0x33332222	
MPP Control2	0xf008	0x00000011	
MPP Control3	0xf00c	0x00000000	

Marvell Reset Initialization

Pin	Value	Description
AD[0]	0	Serial ROM not supported
AD[1]	1	DRAM Pads auto-calibration enabled -- can also pulldown
AD[3:2]	00	Serial ROM id – NA
AD[4]	1	Little endian -- can also pullup
AD[5]	0	Default internal space = 0x1400.0000
AD[7:6]	10	SysAD CPU bus
AD[8]	1	CPU Pads auto-calibration enabled -- can also pulldown
AD[9]	0	Single GT64240A
AD[11:10]	00	N/A
AD[12]	1	PCI_0 auto-calibration enabled -- can also pulldown
AD[13]	1	PCI_1 auto-calibration enabled -- can also pulldown
AD[15:14]	00	8-bit boot width
AD[16]	1	PCI Retry enabled
AD[17]	1	CPU Interface CMOS -- can also pulldown
AD[18]	1	Bypass synchronizers (same clock source) -- can also pulldown
AD[19]	1	DRAM address and control off of rising edge (can also set to 0) -- can also pulldown
AD[20]	0	Standard DDR SDRAM
AD[21]	Rsvd	Can pullup or pulldown
AD[22]	1	SYS_CLK PLL 3.3V CMOS -- can also pulldown
AD[23]	1	Normal op
AD[24]	1	Normal op
AD[25]	1	PCI1_AD[63:40] used for GigE Port 2
AD[28:26]	111	Set for PCI66 and PCI-X -- can also pulldown
AD[31:29]	111	Set for PCI66 and PCI-X -- can also pulldown
P0_TXD[2:0]	010	Port 0 is GMII -- can also set TBI
P1_TXD[2:0]	010	Port 1 is GMII -- can also set TBI
P1_TXD[5:3]	010	Port 2 is GMII -- can also set TBI
DEV_WE[0]	0	SYS_CLK PLL enabled -- can also pullup
DEV_WE[3:1]	000	SYS_CLK PLL CMOS 3.3V -- can set to other options
DEV_DP[0]	1	SYS_CLK input set to CMOS
DEV_DP[1]	1	Normal op
DEV_DP[2]	1	CMOS GigE Port 1 I/O
DEV_DP[3]	1	CMOS GigE Port 0 I/O
BADR[0]	0	Must pulldown
BADR[1]	0	Must pulldown
BADR[2]	1	GigE Pads auto-calibration enabled -- can also pulldown
P0_TXD[6:4]	000	Normal op -- can also pullup
P0_TXD[7]	0	JTAG Pad calibration bypassed -- can also pullup
P0_TXD[3]	0	TCLK PLL enabled -- can also pullup
P1_TXD[7:6]	00	Reserved -- can also pullup

Values from internal registers

ffcf3192 Matches with these settings
0120140f

0153e40f
02442c0f

	0153e40f	FIFO mode 02442c0f	w/o LUC GMII mode 0220140f	w/ LUC ??? 0153e40f	0120140f Regular 0120140f
3d4					
0	DEV_DP[0]	1	1	1	1
1	DEV_DP[1]	1	1	1	1
2	DEV_DP[2]	1	1	1	1
3	DEV_DP[3]	1	1	1	1
4	DEV_WE[0]	0	0	0	0
5	DEV_WE[1]	0	0	0	0
6	DEV_WE[2]	0	0	0	0
7	DEV_WE[3]	0	0	0	0
8	BADR[0]	0	0	0	0
9	BADR[1]	0	0	0	0
10	BADR[2]	1	1	1	1
11	P0_TXD[0]	0	1	0	0
12	P0_TXD[1]	0	0	1	1
13	P0_TXD[2]	1	1	0	0
14	P0_TXD[3]	1	0	0	0
15	P0_TXD[4]	1	0	0	0
16	P0_TXD[5]	1	0	0	0
17	P0_TXD[6]	1	0	0	0
18	P1_TXD[0]	0	1	0	0
19	rsvd	0	0	0	0
20	P0_TXD[7]	1	0	0	0
21	P1_TXD[1]	0	0	1	1
22	P1_TXD[2]	1	1	0	0
23	P1_TXD[3]	0	0	0	0
24	P1_TXD[4]	1	1	1	1
25	P1_TXD[5]	0	0	0	0
26	P1_TXD[6]	0	0	0	0
27	P1_TXD[7]	0	0	0	0
28		0	0	0	0
29		0	0	0	0
30		0	0	0	0
31		0	0	0	0

change to 0120140f

PCI0 Memory Map

Physical Address	Size	Function
1d00.0000	4KB	QLogic port 0 registers
1d00.1000	4KB	QLogic port 1 registers
4000.0000	1GB	Marvell memory

PCI ID

Vendor	ID
Marvell	648011ab
TXRX	0001166d
FP	0001166d
Bridge	b1548086
National	0020100b
CF	11001013

PCI0 Configuration

Device	Dev #	IDSEL	PCI Config-cycle Address
Primary Bus (0)			
QLogic	0	16	1000_0000_0000_0000_0000_0fff_rrrrrr00
Marvell PCI0	1	17	1000_0000_0000_0000_0000_1fff_rrrrrr00

PCI0 Reset Configuration

Pin	Value	Description
MV64EN_L	0	Enable 64-bit mode
REQ640_L	0	Enable 64-bit mode -- tied to MV64EN_L
M66EN0	n/a	Can pullup or pulldown
DEVSEL0_L, STOP0_L, TRDY0_L	100	DEVSEL0_L goes to pullup as per PCI spec; STOP0_L and TRDY0_L can also be set to 1; selects 133MHz PCI-X

PCI1 Memory Map

Physical Address	Size	Function	Notes
1800.0000	8MB	CF Controller I/O	Remapped to 0x0000.0000
1880.0000	8MB	CF Controller Memory	Remapped to 0x0080.0000
1900.0000	8MB	National MAC	
1980.0000	8MB	National MAC	
1a00.0000	16MB	TXRX Shared Memory	TXRX accesses this locally at 0x9000.0000
1b00.0000	16MB	FP Shared Memory	FP accesses this locally at 0x9000.0000
1c00.0000	64KB	Marvell registers	
1c04.0000	256KB	Marvell SRAM	
1f40.0000	2MB	BM-FPGA	
4000.0000	1GB	Marvell memory	

PCI ID

Vendor	ID
Marvell	648011ab
TXRX	0001166d
FP	0001166d
Bridge	b1548086
National	0020100b
CF	11001013

PCI1 Configuration

Device	Dev #	IDSEL	PCI Config-cycle Address
Primary Bus (1)			
TXRX	0	16	1000_0000_0000_0001_0000_0fff_rrrrrr00
FP	1	17	1000_0000_0000_0001_0000_1fff_rrrrrr00
Bridge	2	18	1000_0000_0000_0001_0001_0fff_rrrrrr00
Marvell PCI1	3	19	1000_0000_0000_0001_0001_1fff_rrrrrr00
Secondary Bus (2)			
National MAC	0	16	1000_0000_0000_0010_0000_0fff_rrrrrr00
National MAC	1	17	1000_0000_0000_0010_0000_1fff_rrrrrr00
CF Controller	2	18	1000_0000_0000_0010_0001_0fff_rrrrrr00

PCI1 Reset Configuration

Pin	Value	Description
REQ641_L	1	Disable 64-bit mode
M66EN1	1	Enable 66MHz operation
DEVSEL0_L, STOP0_L, TRDY0_L	111	Pullups select conventional PCI operation

RM9200 Interrupts

Interrupt	Function
NMI	Watchdog Timer
IRQ0	MV64440 CPU_Int0
IRQ1	MV64440 CPU_Int1
IRQ2	BM-FPGA Message Interrupt (Core 0)
IRQ3	BM-FPGA Status Interrupt (Core 0)
IRQ4	BM-FPGA Message Interrupt (Core 1)
IRQ5	BM-FPGA Status Interrupt (Core 1)
IRQ6	ISP2312/22 Interrupt
IRQ7	Temperature Status Interrupt
IRQ8	PCMCIA Socket A Interrupt
IRQ9	PCMCIA Socket B Interrupt

Marvell GPIO Definition

Bit	Dir	Description
31:30	O	CF1 LED (00 = off; 01 = red; 10 = green; 11 = amber)
29:28	O	CF0 LED (00 = off; 01 = red; 10 = green; 11 = amber)
27	O	LOS Mux Sel (0 = SFP; 1 = LSI MAC)
26	O	GigE Port Disable (set to 0)
25	O	GigE SFP Rate Sel (set to 0)
24:23	O	FLT LED (00 = off; 01 = red; 10 = green; 11 = amber)
22:21	O	OK LED (00 = off; 01 = red; 10 = green; 11 = amber)
20	I	GigE Port 3 TX Fault (0 = ok; 1 = fault)
19	I	GigE Port 2 TX Fault (0 = ok; 1 = fault)
18	O	Frontpanel LED Enable (0 = on; 1 = off)
17	I	ISP2312 PCI0 Request
16	O	ISP2312 PCI0 Grant
15	I	U1 CTS
14	O	U1 RXD
13	I	U1 RTS
12	O	U1 TXD
11	I	U0 CTS
10	O	U0 RTS
9	I	U0 RXD
8	O	U0 TXD
7	I	GigE Port 1 TX Fault (0 = ok; 1 = fault)
6	I	GigE Port 0 TX Fault (0 = ok; 1 = fault)
5	I	PCI Bridge PCI1 Request
4	O	PCI Bridge PCI1 Grant
3	I	FP PCI1 Request
2	O	FP PCI1 Grant
1	I	TXRX PCI1 Request
0	O	TXRX PCI1 Grant

BM-FPGA Address Map

Register	Offset
Board Status	0x000
Interrupt	0x004
GPP	0x008
Test Register	0x00c
FP Control	0x010
FP Control (Expansion)	0x014
FP Status	0x018
FP Status (Expansion)	0x01c
FP Power Usage Out	0x020
FP Power Usage In	0x024
FP Mailbox Message Out	0x028
FP Mailbox Message In	0x02c
FC Control -- Core 0	0x030
FC Control (Expansion) -- Core 0	0x034
FC Status -- Core 0	0x038
FC Status (Expansion) -- Core 0	0x03c
FC Power Usage -- Core 0	0x040
FC Power Usage In -- Core 0	0x044
FC Mailbox Message Out -- Core 0	0x048
FC Mailbox Message In -- Core 0	0x04c
FC Control -- Core 1	0x050
FC Control (Expansion) -- Core 1	0x054
FC Status -- Core 1	0x058
FC Status (Expansion) -- Core 1	0x05c
FC Power Usage -- Core 1	0x060
FC Power Usage In -- Core 1	0x064
FC Mailbox Message Out -- Core 1	0x068
FC Mailbox Message In -- Core 1	0x06c

Board Status Register (RO)

Bit	Definition
0	Diag Select (0 = normal, 1 = diags)
1	Prom Select (0 = recovery, 1 = normal)
13:2	Reserved
14	Board rev (0 = prototype 1; 1 = prototype 2 and later)
15	Clock speed (0 = 100MHz; 1 = 133MHz)
23:16	BM-FPGA Version
31:24	Reserved

Status and Control Register (RW)

Bit	Definition
0	FP Status Interrupt
1	FP Message Interrupt
2	FC Status Interrupt
3	FC Message Interrupt
4	PS0 ok (1 = good)
5	PS0 good (1 = good)
6	PS1 ok (1 = good)
7	PS1 good (1 = good)
8	Fan Controller 0 status (1 = good)
9	Fan Controller 1 status (1 = good)
15:10	Reserved
16	Fan Control (0 = normal; 1 = full on)
31:17	Reserved

General Purpose Register (RW)

Bit	Definition
0	TXRX Cold Reset (1 = reset)
1	TXRX Warm Reset (1 = reset)
2	FP Cold Reset (1 = reset)
3	FP Warm Reset (1 = reset)
4	LSI MAC Reset (1 = reset)
5	LUC Reset (1 = reset)
6	PCI0 Reset (1 = reset)
7	PCI1 Reset (1 = reset)
8	Secondary PCI1 Reset (1 = reset)
9	Serdes Reset (1 = reset)
11:10	Reserved
15:12	FP Port Enable (1 = enable)
31:16	Reserved

BM-FPGA Register Routing

CPU	Register Written	CPU	Register Read	Notes
SSC	FP Control	TXRX	Status	
SSC	FP Control (Expansion)	TXRX	Status (Expansion)	Not currently implemented
SSC	FP Power Usage Out	TXRX	Power Usage In	Not currently implemented
SSC	FP Mailbox Message Out	TXRX	Mailbox Message In	
SSC	FC Control -- Core 0	FC	FC Status -- Core 1	
SSC	FC Control (Expansion) -- Core 0	FC	FC Status (Expansion) -- Core 1	Not currently implemented
SSC	FC Power Usage Out -- Core 0	FC	FC Power Usage In -- Core 1	Not currently implemented
SSC	FC Mailbox Message Out -- Core 0	FC	FC Mailbox Message In -- Core 1	
FC	FC Control -- Core 1	SSC	FC Status -- Core 0	
FC	FC Control (Expansion) -- Core 1	SSC	FC Status (Expansion) -- Core 0	Not currently implemented

FC	FC Power Usage Out -- Core 1	SSC	FC Power Usage In -- Core 0	Not currently implemented
FC	FC Mailbox Message Out -- Core 1	SSC	FC Mailbox Message In -- Core 0	
TXRX	Control	SSC	FP Status	
TXRX	Control (Expansion)	SSC	FP Status (Expansion)	Not currently implemented
TXRX	Power Usage Out	SSC	FP Power Usage In	Not currently implemented
TXRX	Mailbox Message Out	SSC	FP Mailbox Message In	

I2C Addresses

Device	7-bit Address	Notes
Board SEEP	1010000	Board parameters and info
FC SEEP	1010001	Rev 2 and higher only
PMC Memory SEEP	1010100	PMC memory parameters
Marvell Memory SEEP	1010101	Marvell memory parameters
Temperature Sensor	1001101	Board temperature
Temperature Sensor	1001110	Board temperature (exhaust) -- Rev 2 and higher only
Fan Controller	1001011	Fans 1-3
Fan Controller	1001000	Fans 4-6

MDIO Addresses

Device	Address	Master
Frontpanel SERDES	0x10	MV64440 (accessible by RM9000 or TXRX)

Board Configuration Jumpers

Jumper	Description	Pos 1-2	Pos 2-3
J6007	Prom Select	*Normal*	Recovery
J6008	Diagnostics mode	*Normal*	Diagnostics
J7309	12V Remote Sense	*On*	Off

LUC Programming Jumpers

Jumper	Description	Pos 1-2	Pos 2-3
J3201	LUC Load	*SW Load*	Xilinx Load
J6009	LUC Load	Xilinx Load	*SW Load*

To program via Xilinx Load, must also move R3214 to R3213

Default setting is in italics

Debug headers

Header	Description	Location
J1101	FP Core 0	Back right
J1102	FP Core 1	Back right
J1104	Muxed FP Core 0 and 1	Front right
J2501	TXRX Core 0	Middle center
J2502	TXRX Core 1	Middle center
J2504	Muxed Core 0 and Core 1	Front right
J5904	SSC	Back center
J5905	FC	Back center
J5907	Muxed SSC and FC	Front right
J7201	Debug SSC	Front right
J7202	Debug FC	Front right

PMC Memory init algorithm:

Registers to program	SDCFG	LKB0
	SDM0	LKM0
	SDM1	LKB1
	SDT0	LKM1
	SDT1	

Sizing	Calculate total size of memory populated
	if SDRAM Banks (byte 5) = 2, then enable 2 chip select regions; i.e. program SDT0, SDM0, SDT1, SDM1; each chip select has half of the memory
	if SDRAM Banks (byte 5) = 1, then enable 1 chip select region; i.e. program SDT0, SDM0; chip select has all of the memory
	SDRAM Banks then sets LKB/M size; i.e. with 2 chip selects, both LKB/M0, 1 get programmed
	if SDRAM Device Width (byte 13) = 8 then SDM0 9:8 = 0; = 10 then SDM0 9:8 = 1; = 20 then SDM0 9:8 = 2
	if memory size = 512MB then SDM 6:4 = 011; = 1GB then SDM 6:4 = 100
	if SDRAM Module Attributes (byte x21) = 0x26, then SDM 2 = 1; else SDM 2 = 0
	Set bit 1 in SDM
	Set bit 0 in SDM
	Example with current modules:
	SDCFG = 0x000002d9
	SDM0,1 = 0x00004047 with 1GB; SDM0,1 = 0x00004037 with 512MB
Timing	tREF = 3f
	tRP = (tRP (byte 27) >> 2) / clock cycle time => if 2 then tRP = 00; 3 = 01; 4 = 10
	tRCD = (tRCD (byte 29) >> 2) / clock cycle time => if 2 then tRCD = 00; 3 = 01; 4 = 10
	tRC = tRP (byte 27) + tRCD (byte 29) + 1; set tRC accordingly (most likely will be 8)
	tCAC => Set to 01
	Example with current modules:
	SDT0, 1 = 0x003f8481
Scrub memory	Must write before any read

Marvell Memory init algorithm:

Registers to program	SDRAM Config	CS0 Base
	Dunit Control (Low)	CS0 Size
	Dunit Control (High)	CS1 Base
	SDRAM Addr Control	CS1 Size
	DDR Timing (Low)	PCI CS0 BAR Size
	DDR Timing (High)	PCI CS0 (Config space)
	SDRAM Mode	PCI CS1 BAR Size
	SDRAM Open Pages	PCI CS1 (Config space)

Sizing	Calculate total size of memory populated	
	if SDRAM Banks (byte 5) = 2, then enable 2 chip select regions; i.e. program CS0, CS1; each chip select has half of the memory	
	if SDRAM Banks (byte 5) = 1, then enable 1 chip select region; i.e. program CS0; CS0 has all of the memory	
	SDRAM Banks then sets CS Base/Size; i.e. with 2 chip selects, both CS0, 1 Base/Size are programmed	
	if SDRAM Module Attributes (byte x21) = 0x26, then SDRAM Config 17 = 1; else SDRAM Config 17 = 0	
	Set bit 18 to enable ECC	
	Program SDRAM Addr Control -- if 256MB size => Dcfg = 0; 512MB/1GB => Dcfg = 1; 2GB => Dcfg = 2	
	Example with current modules:	
	SDRAM Config = 0x58260400	
	Dunit Control (Low) unchanged	
	Dunit Control (High) unchanged	
	SDRAM Addr Control = 0x00000012	
	SDRAM Open Pages unchanged	
Timing	tRCD = ((tRCD (byte 29) >> 2) / clock cycle time) - 1	7:4
	tRP =((tRP (byte 27) >> 2) / clock cycle time) - 1	11:8
	tWR = 1	15:12
	tWTR = 1	19:16
	tRAS = (tRAS (byte 30) / clock cycle time) - 1	23:20
	tRRD = ((tRRD (byte 28) >> 2) / clock cycle time) - 1	27:24
	tRFC = tRFC (byte 42) / clock cycle time - 1	3:0
	Example with current modules:	
	DDR Timing (Low) = 0x01511220	
	DDR Timing (High) = 0x00000009	
	SDRAM Mode = 0x00000062	
Scrub memory	Must write before any read	