ISP2312 Designer's Guide

Dual 2-Gb Fibre Channel to 133-MHz PCI-X Controller

Document Revision History	
Rev. A release, 4/4/01, chip affected: ISP2312 (2405236)	
Rev. B update, 5/31/01, chip affected: ISP2312 (2405236)	
Rev. C update, 6/27/01, chip affected: ISP2312 (2405236)	
Rev. D update, 4/19/02, chips affected: ISP2312-ES1 (2405236), ISP2312-ES2 (2405311, 2405322)	
Rev. E update, 8/1/03, chips affected: ISP2312-ES1 (2405236), ISP2312-ES2 (2405311, 2405322)	
Changes	Document Sections Affected
Electrical characteristics: Changed maximum power dissipation (Pmax) value. Changed maximum case temperature @Pmax (Tc) value. Provided measurements for IDD (previously preliminary estimates). Removed statement "Capacitance in and out (CIN, COUT) is 10 pf maximum for all pins." DC characteristics: removed SSTL parameter for VOH and VOL.	2.4
Pins $\overline{\text{RADDR18–20\_1}}$ and $\overline{\text{RADDR18–20\_2}}$ can be used only for debug purposes; they can no longer be used an SRAM chip select.	3.2.2
NCVS pin is no longer used as a sense input during power-up reset.	3.2.4
GPIO_1[0] and GPIO_2[0] can no longer be configured as input pins for RISC debugging. GPIO_1[1] and GPIO_2[1] can no longer be configured as output pins for RISC debugging.	3.2.7, 6.7.13

For QLogic HBA designs, the GPIO_1[0, 7–6] and GPIO_2[0, 7–6] pins are programmed to control the LEDs on the HBA. These pins are controlled by the RISC firmware to indicate I/O activity and status information. To maintain firmware compatibility, these signals must not be used for any other purpose.	3.2.7, 6.7.13
The REFCLK2 pin is reserved; it no longer provides a clock for the internal ISP2312 logic.	3.2.7, removed 5.3, 5.3.2
Corrected PCI interface signal connection diagrams to show PCIXCAP.	6.2.1, 6.2.2, 6.2.3
Corrected PCI 64-bit addressing with Dual Address Cycle command.	6.4.1
PCI Vendor ID register: The value in this register can no longer be loaded from an external serial EEPROM when the NVCS pin is pulled up.	6.6.1, A.2, removed 8.3 and 12.6
PCI Device ID register: The value in this register can no longer be loaded from an external serial EEPROM when the NVCS pin is pulled up.	6.6.2, A.2 removed 8.3 and 12.6
PCI-X Status register: corrected description of Function Number bits (bits 2–0).	6.6.20.4
ISP Control/Status register is accessible from the RISC processor (documentation error).	6.7.3, A.3
GPIOD register: The RISC processor and host driver must coordinate access to this register.	6.7.13
The RISC interface can be implemented using the additional SRAM configurations of 1M×18 and 2M×18.	7.1
Changed SRAM connection configurations. RISC SRAM supports loading for only one SRAM device. SRAM device core voltage can be any value (was previously limited to 2.5 volts or 3.3 volts). Updated recommended SRAM devices.	7.2.1
The following locations are no longer used for system vendor and device IDs for each function: Function 0/port 1: system vendor ID 72h, system device ID 73h Function 1/port 2: system vendor ID F2h, system device ID F3h	8.1
Added function/port information to PCI subsystem ID and subsystem vendor ID.	8.3
Added list of recommended flash ROM devices.	9.2
Updated transmitter termination illustrations.	10.2, 10.3
Removed RISC Clock Frequency Sense Pins section has been removed (PDATA3–2 pins are no longer sampled at PCI bus rest to determine the ISP2312 clock frequency).	was 12.2
Changed recommended program to compute differential impedance.	13
Updated schematics.	15

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Section 1
Overview

1.1 Introduction

The ISP2312 is a complete PCI to Fibre Channel host adapter on a single chip. This guide is for design engineers who are implementing a board design using the ISP2312 chip. This guide covers all the interfaces of the device and gives details about how to design the ISP2312 into a board-level product. The reader should be familiar with the following PCI and Fibre Channel standards:

- *PCI Local Bus Specification,* revision 2.2, December 8, 1998
- *PCI-X Addendum (*revision 1.0) *to the PCI Local Bus Specification*, September 22, 1999
- *PCI Bus Power Management Interface Specification* revision 1.1 (PC99)
- *SCSI-3 Fibre Channel Protocol* (SCSI-FCP), X3.269:1996
- *Fibre Channel Physical and Signaling Interface (FC-PH)* X3.230:1994
- *Fibre Channel 2nd Generation* (FC-PH-2), X3.297:1997
- *Third Generation Fibre Channel Physical and Signaling Interface* (FC-PH-3), X3.303:1998
- *Fibre Channel—Arbitrated Loop (FC-AL-2)*, working draft, revision 6.4, August 28, 1998
- *Fibre Channel Fabric Loop Attachment Technical Report (FC-FLA)* NCITS/TR-20:1998
- *Fibre Channel—Private Loop Direct Attach Technical Report* (FC-PLDA), NCITS/TR-19:1998
- *Fibre Channel Tape (FC-TAPE)* profile, T11/99-069v4, revision 1.17, May 14, 1999
- *SCSI Fibre Channel Protocol-2* (FCP-2) working draft, revision 3, October 1, 1999
- *ANSI Information Technology—SCSI 3 Architecture Model*, revision 18, November 27, 1995

Note that this document does not cover firmware or software.

Topics covered in each section are summarized below.

- **Section 1—Overview.** This section describes the content of this guide and its audience.
- **Section 2—Package Information.** This section contains information about the ISP2312 chip.
- **Section 3—Pin Descriptions.** This section defines the pins on the ISP2312 chip.
- **Section 4—Power Connections.** This section defines the digital and analog power requirements and PCI clamp voltage input for the ISP2312 chip.
- **Section 5—Clock Requirements.** This section defines the requirements for the BCLK and REFCLK1 clock inputs for the ISP2312 chip.
- **Section 6—PCI Interface.** This section defines the PCI connections to the ISP2312 chip.
- **Section 7—RISC Interface.** This section defines the RISC interface connections to the ISP2312 chip.
- **Section 8—NVRAM Interface.** This section defines the NVRAM interface connections to the ISP2312 chip.
- **Section 9—Flash ROM Interface.** This section defines the Flash ROM interface connections to the ISP2312 chip.

  NOTE: The flash BIOS pins can be used only during the power-up initialization sequence. When the ISP2312 begins normal operations, some flash BIOS pins become RISC interface pins.

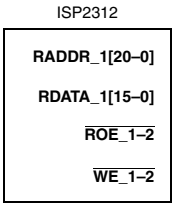
- **Section 10—Fibre Channel Interface.** This section defines the Fibre Channel interface connections to the ISP2312 chip.

- **Section 11—JTAG Boundary Scan Interface.** This section defines the JTAG boundary scan interface connections to the ISP2312 chip.
- **Section 12—Sense Pins.** This section what pins the ISP2312 samples at power up to determine certain settings, such as the chip operating mode, RISC clock frequency, and PCI-X mode.
- **Section 13—Layout Considerations.** This section contains recommendations to consider when designing the printed circuit board (PCB).
- **Section 14—Compatibility with Future ISP2312 Devices.** This section summarizes the PCB design changes necessary to accommodate future ISP2312 devices.
- **Section 15—Reference Schematics.** This section defines the ISP2312 chip reference schematics.
- **Section 16—Timing.** This section contains RISC and EEPROM timing diagrams.
- **Appendix A—Register Summary.** This section lists the PCI registers described in this guide.
- **Index.** The index lists major subjects and concepts with page numbers for easy reference.

1.2 Documentation Conventions

The *ISP2312 Designer's Guide* uses the following documentation conventions:

- In graphics, ISP2312 pins are always bold, as illustrated below.



- Information that is very important to the board design is set off by **bold** text.
- Information that is critical to the board design is set off by a note:

NOTE: Be sure to read everything in the note boxes.

1.3 Features

The following features are available in the ISP2312:

- Two completely independent 2-Gb serial Fibre Channel ports, each identical in functionality to the single Fibre Channel port on the ISP2300/2310
- Support for multifunction PCI
- Two of each of the following modules to support the two Fibre Channel ports:
  - Internal RISC processor
  - Receive DMA sequencer
  - Frame buffer
  - DMA channels (transmit, receive, command, auto-request, and auto-response)
- Support for JTAG boundary scan for I/Os; full scan for internal logic and built-in self test (BIST) for onboard memories
- Support for CompactPCI Hot Swap (PCI 2.2 mode only)
- PCI-X support
- Support for Fibre Channel virtual interface (VI) protocol
- Support for 2-Gb Fibre Channel using internal or external transceivers
- Automatically negotiates Fibre Channel bit rate (1 Gb or 2 Gb)
- Supports up to 400 MBps sustained Fibre Channel data transfer rate
- Complete data and code parity protection
- No host intervention required to execute complete SCSI, IP, or VI operations
- Supports multi-ID aliasing in target mode
- Improved loopback functionally

Section 2
Package Information

2.1
Mechanical Drawings

The ISP2312 is packaged in a 388-pin thermally enhanced package plastic ball grid array (EPBGA-T). The ISP2312 mechanical drawings are illustrated in figure 2-1.

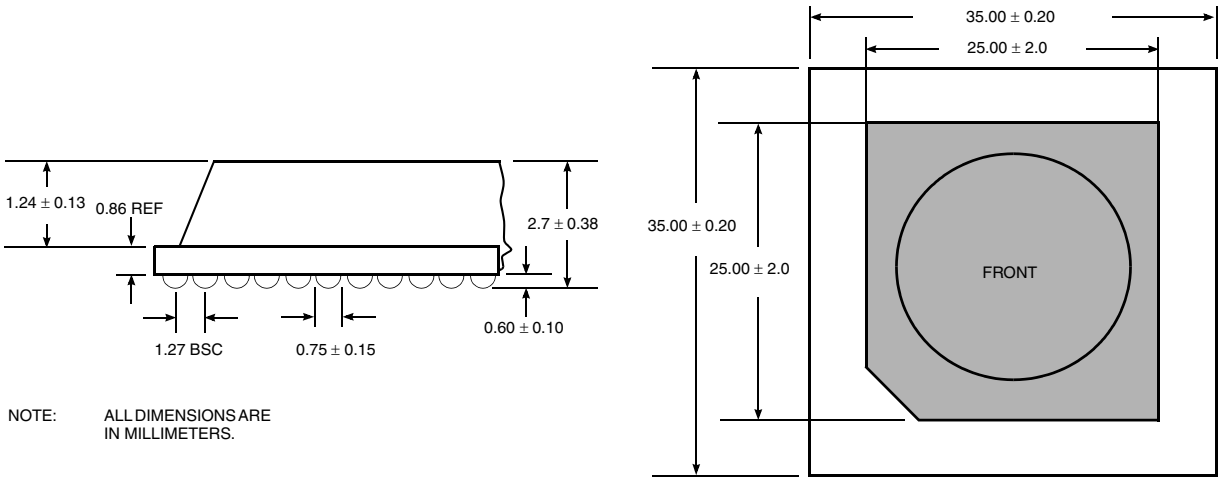


Figure 2-1. ISP2312 Mechanical Drawings

2.2
Pad Stacking

Adhere to the following requirements when creating the printed circuit board (PCB) pads to place the ISP2312 on the PCB.

- Determine the placement and spacing of the pads from the mechanical drawing (see figure 2-1).
- The PCB pads must be 0.026-inch in diameter.
- The PCB pad solder mask must be a 0.026-inch diameter hole.
- Each PCB pad must have a via. Place each via diagonally from its pad, equidistant from the surrounding pads. The via pad must be 0.020-inch in diameter and have a central 0.010-inch diameter finish hole. Cover the vias with the solder mask. Connect the vias to their pad with a maximum width etch of 0.007 inch for signals, 0.10 for power and ground.
- Use a 0.026-inch pad with a 0.030-inch ball to allow for a 0.015–0.018-inch collapse of the ball during solder reflow (see figure 2-2).

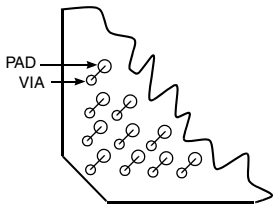


Figure 2-2. PCB Pads and Vias

2.3 Thermal Requirements

Proper cooling must be provided in all applications so that the maximum operating temperature of the ISP2312 remains within the specified limits. The thermal information for the ISP2312 is listed in table 2-1.

2.4 Electrical Characteristics

Tables 2-2 through 2-4 define the ISP2312 electrical characteristics.

Table 2-1. Thermal Parameters

Name	Description	Value
Pmax	Maximum power dissipation	3.975 watts
Tc	Maximum case temperature @ Pmax	87.7°C
Tj	Maximum junction temperature @ Pmax	100°C
θja	Junction to ambient thermal impedance:	
	No airflow	12.4°C/watts
	0.5 meter/sec airflow	10.7°C/watts
	1.0 meter/sec airflow	9.9°C/watts
	2.0 meters/sec airflow	9.1°C/watts
	3.0 meters/sec airflow	8.6°C/watts
θjc	Junction to case thermal impedance	3.1°C/watts

Table Notes
Do not exceed the maximum case or junction temperature limits in this table while power is applied.

Table 2-2. Absolute Maximum Stress Ratings

Symbol	Description	Rating	Unit
TSTG	Storage temperature	–40 to 125	°C
VDD2.5	Supply voltage	–0.3 to 3.1	V
VDD3.3	Supply voltage	–0.3 to 3.9	V
VIN	Input voltage		
	3.3-V drive	–1.0 to VDD3.3	V
	5-V compatible	–1.0 to 6.5	V
	LVTTL	–1.0 to VDD + 0.3	V
ILP	Latch-up current	–150 to 150	mA
ESD	Electrostatic discharge	2[a]	kV

Table Notes
Conditions that exceed the absolute maximum stress rating may destroy the chip.
[a]Human body model

Table 2-3. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
VDD3.3	Supply voltage	3.13	3.47	V
VDD2.5	Supply voltage	2.375	2.625	V
IDD	Supply current (dynamic IDD at 3.3 V; ISP2312 (PCI-X mode))	3.0	200.0	mA
	Supply current (dynamic IDD at 2.5 V; ISP2312 (PCI-X mode))	115.0	1250.0	mA

Table Notes
Conditions that exceed the operating conditions but are within the absolute maximum stress ratings may cause the chip to malfunction.

Table 2-4. DC Characteristics

Symbol	Parameter	Condition[a]	Min.	Typical	Max.	Unit
VIL	Voltage input low					
	LVTTL		VSS – 0.5		0.8	V
	PCI (5 V)		–0.5		0.8	V
	PCI (3.3 V)		–0.5		0.3 VDD	V
VIH	Voltage input high					
	LVTTL		2.0		VDD3.3 + 0.3	V
	PCI (5 V)		2.0		5.5	V
	PCI (3.3 V)		0.5 VDD3.3		VDD3.3 + 0.3	V
VT	Switching threshold (standard input only)					
	LVTTL			1.4	2.0	V
IIN	Input current					
	LVTTL-D	VIN = VDD3.3	35	120	280	µA
	LVTTL-U	VIN = VSS	–35	–100	–214	µA
	All other buffer types	VIN = VDD3.3 or VSS	–10	±1	10	µA
VOH	Voltage output high					
	C-4	IOH = –4 mA	2.0		VDD3.3	V
	C-6	IOH = –6 mA	2.0		VDD3.3	V
	C-8	IOH = –8 mA	2.0		VDD3.3	V
	C-12	IOH = –12 mA	2.0		VDD3.3	V
	PCI (5 V)	IOH = –2 mA	2.4			V
	PCI (3.3 V)	IOH = –0.5 mA	0.9 VDD3.3			V
VOL	Voltage output low					
	C-4	IOL = 4 mA			0.4	V
	C-6	IOL = 6 mA			0.4	V
	C-8	IOL = 8 mA			0.4	V
	C-12	IOL = 12 mA			0.4	V
	PCI (5 V)	IOL = 6 mA			0.55	V
	PCI (3.3 V)	IOL = 1.5 mA			0.1 VDD3.3	V
VSRX	Differential input voltage sensitivity					
	GRX		0.4		2.3	V
VSTX	Differential output swing voltage, peak to peak					
	GTX		1.6		3.2	V
IOZ	Tristate output leakage current	VOH = VSS or VDD3.3	–10	±1	10	µA
IOS	Output short circuit current	VO = VDD3.3 (PCI) VO = VSS (PCI) VO = VDD3.3 (non-PCI) VO = VSS (non-PCI)			220 –150 140 –80	mA mA mA mA
CIN	Input pin capacitance	Any input buffer			4.0	pF
COUT	Output pin capacitance	Any output buffer			4.0	pF
CIN/ COUT	Bidirectional pin capacitance (except PCI)	Any bidirectional buffer			4.0	pF
	PCI				5.0	pF

Table Notes

[a]The case temperature cannot exceed the value defined in table 2-1.

Section 3
Pin Descriptions

3.1
Pin Configuration

The ISP2312 pin layout is illustrated in figure 3-1.

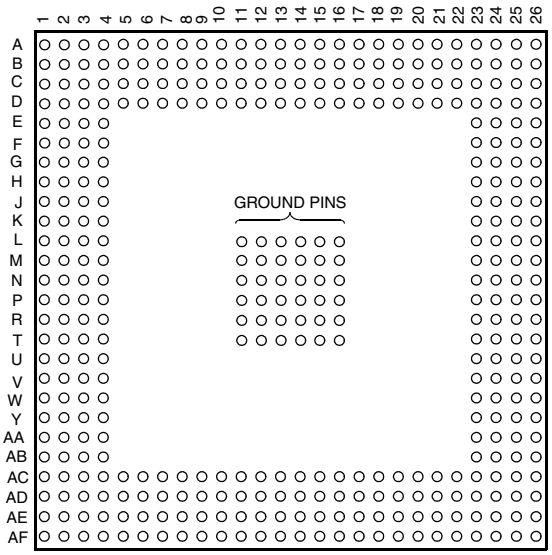


Figure 3-1. ISP2312 Solder Ball Configuration (Top View)

The ISP2312 pins are grouped by function in figure 3-2.

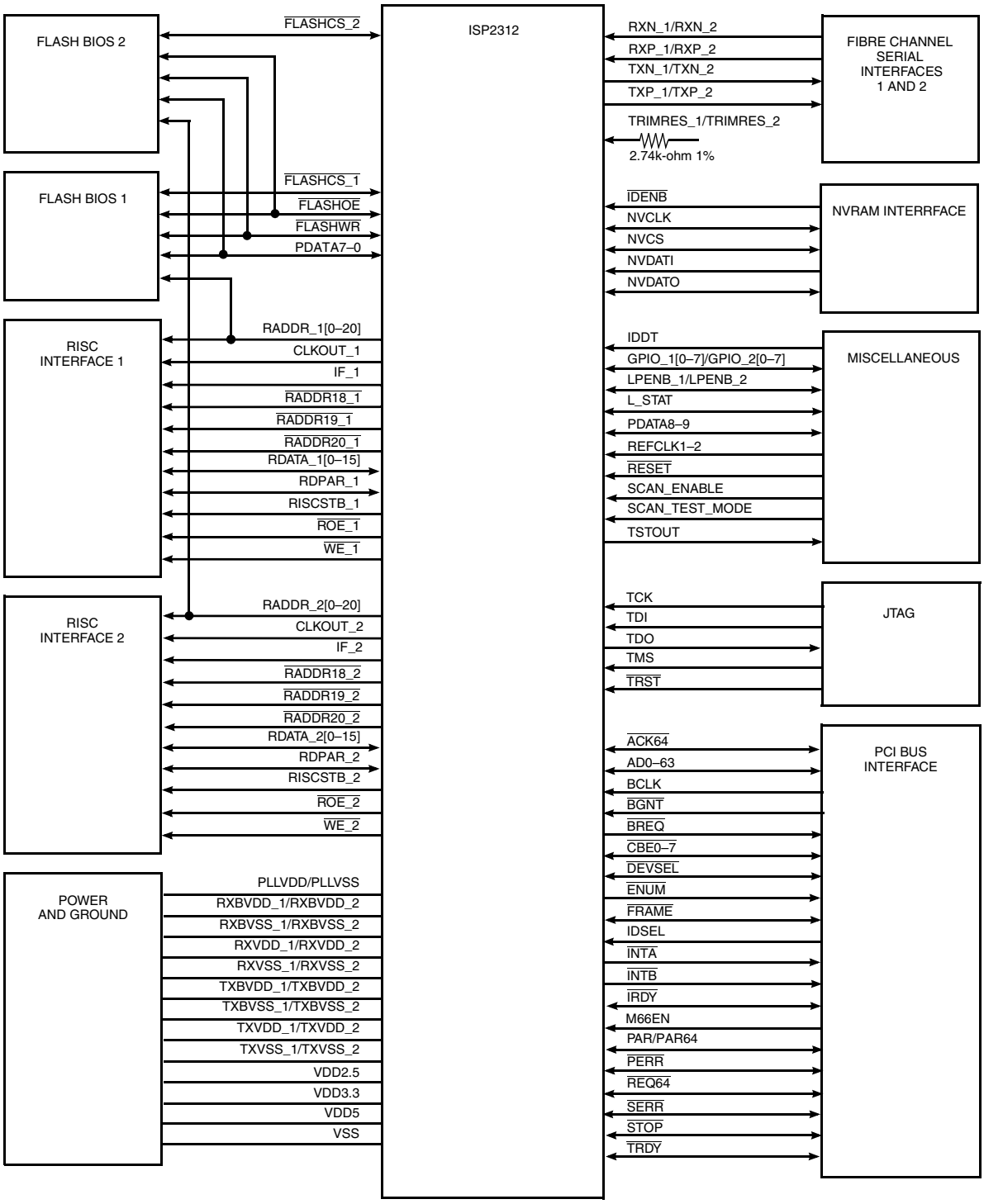


Figure 3-2. ISP2312 Functional Signal Grouping

The pins are identified by location in table 3-1 and alphabetically by name in table 3-2.

Table 3-1. ISP2312 Pins by Location

Solder Ball	Pin Name
A1	VSS
A2	VSS
A3	GPIO_2[7]
A4	GPIO_2[6]
A5	GPIO_2[5]
A6	TSTOUT
A7	VDD3.3
A8	VSS
A9	$\overline{\text{TRST}}$
A10	TRIMRES_2
A11	TXN_2
A12	RXP_2
A13	VSS
A14	VDD3.3
A15	TXVSS_1
A16	TXN_1
A17	RXP_1
A18	NC
A19	VSS
A20	VDD3.3
A21	REFCLK2
A22	NVCLK
A23	$\overline{\text{FLASHWR}}$
A24	PDATA8
A25	VSS
A26	VDD3.3
B1	VSS
B2	GPIO_2[4]
B3	GPIO_2[3]
B4	GPIO_2[2]
B5	GPIO_2[1]
B6	SCAN_TEST_MODE
B7	SCAN_ENABLE
B8	TDO
B9	TMS
B10	TXVSS_2

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
B11	TXP_2
B12	RXN_2
B13	RXVSS_2
B14	TXVDD_1
B15	TXP_1
B16	NC
B17	RXN_1
B18	RXVSS_1
B19	GPIO_1[7]
B20	GPIO_1[6]
B21	GPIO_1[5]
B22	NVDATI
B23	$\overline{\text{FLASHCS\_1}}$
B24	PDATA7
B25	PDATA0
B26	VSS
C1	IF_2
C2	$\overline{\text{WE\_2}}$
C3	VSS
C4	CLKOUT_2
C5	GPIO_2[0]
C6	IDDT
C7	TCK
C8	$\overline{\text{FLASHCS\_2}}$
C9	TDI
C10	TXBVSS_2
C11	RXBVDD_2
C12	RXVDD_2
C13	TRIMRES_1
C14	TXBVSS_1
C15	TXBVDD_1
C16	NC
C17	RXBVSS_1
C18	GPIO_1[4]
C19	GPIO_1[3]
C20	GPIO_1[2]
C21	NVCS
C22	NVDATO

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
C23	PDATA9
C24	VSS
C25	PDATA4
C26	PDATA5
D1	$\overline{\text{ROE\_2}}$
D2	RISCSTB_2
D3	$\overline{\text{RADDR20\_2}}$
D4	VDD3.3
D5	VDD2.5
D6	VDD2.5
D7	LPENB_2
D8	VDD2.5
D9	LPENB_1
D10	TXVDD_2
D11	TXBVDD_2
D12	RXBVSS_2
D13	VDD3.3
D14	VSS
D15	RXBVDD_1
D16	NC
D17	RXVDD_1
D18	VDD2.5
D19	GPIO_1[1]
D20	GPIO_1[0]
D21	PDATA6
D22	$\overline{\text{FLASHOE}}$
D23	VDD3.3
D24	PDATA1
D25	PDATA2
D26	PDATA3
E1	REFCLK1
E2	$\overline{\text{RADDR19\_2}}$
E3	$\overline{\text{RADDR18\_2}}$
E4	RADDR_2[20]
E23	$\overline{\text{RADDR20\_1}}$
E24	$\overline{\text{ROE\_1}}$
E25	RISCSTB_1
E26	CLKOUT_1

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
F1	RADDR_2[19]
F2	RADDR_2[18]
F3	RADDR_2[17]
F4	VDD2.5
F23	VDD2.5
F24	RADDR_1[20]
F25	$\overline{\text{RADDR18\_1}}$
F26	$\overline{\text{RADDR19\_1}}$
G1	VDD3.3
G2	RADDR_2[16]
G3	RADDR_2[15]
G4	RADDR_2[14]
G23	RADDR_1[17]
G24	RADDR_1[18]
G25	RADDR_1[19]
G26	VDD3.3
H1	VSS
H2	RADDR_2[13]
H3	RADDR_2[12]
H4	VDD2.5
H23	RADDR_1[14]
H24	RADDR_1[15]
H25	RADDR_1[16]
H26	VSS
J1	RADDR_2[11]
J2	RADDR_2[10]
J3	RADDR_2[9]
J4	RADDR_2[8]
J23	RADDR_1[10]
J24	RADDR_1[11]
J25	RADDR_1[12]
J26	RADDR_1[13]
K1	RADDR_2[7]
K2	RADDR_2[6]
K3	RADDR_2[5]
K4	RADDR_2[4]
K23	RADDR_1[6]
K24	RADDR_1[7]

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
K25	RADDR_1[8]
K26	RADDR_1[9]
L1	RADDR_2[3]
L2	RADDR_2[2]
L3	RADDR_2[1]
L4	VDD2.5
L11	VSS
L12	VSS
L13	VSS
L14	VSS
L15	VSS
L16	VSS
L23	RADDR_1[2]
L24	RADDR_1[3]
L25	RADDR_1[4]
L26	RADDR_1[5]
M1	RADDR_2[0]
M2	RDPAR_2
M3	RDATA_2[15]
M4	RDATA_2[14]
M11	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS
M16	VSS
M23	RDATA_1[15]
M24	RDPAR_1
M25	RADDR_1[0]
M26	RADDR_1[1]
N1	VDD3.3
N2	RDATA_2[13]
N3	RDATA_2[12]
N4	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
N15	VSS
N16	VSS
N23	VDD3.3
N24	RDATA_1[14]
N25	NC
N26	VSS
P1	VSS
P2	RDATA_2[11]
P3	VDD2.5
P4	VDD3.3
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
P23	VSS
P24	RDATA_1[12]
P25	RDATA_1[13]
P26	VDD3.3
R1	RDATA_2[10]
R2	RDATA_2[9]
R3	RDATA_2[8]
R4	RDATA_2[7]
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R16	VSS
R23	RDATA_1[8]
R24	RDATA_1[9]
R25	RDATA_1[10]
R26	RDATA_1[11]
T1	RDATA_2[6]
T2	RDATA_2[5]
T3	RDATA_2[4]
T4	VDD2.5

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
T11	VSS
T12	VSS
T13	VSS
T14	VSS
T15	VSS
T16	VSS
T23	VDD2.5
T24	RDATA_1[5]
T25	RDATA_1[6]
T26	RDATA_1[7]
U1	RDATA_2[3]
U2	RDATA_2[2]
U3	RDATA_2[1]
U4	RDATA_2[0]
U23	RDATA_1[1]
U24	RDATA_1[2]
U25	RDATA_1[3]
U26	RDATA_1[4]
V1	$\overline{\text{INTB}}$
V2	PLLVDD
V3	VDD2.5
V4	PLLVSS
V23	IF_1
V24	$\overline{\text{WE\_1}}$
V25	RDATA_1[0]
V26	NC
W1	VSS
W2	$\overline{\text{INTA}}$
W3	$\overline{\text{RESET}}$
W4	$\overline{\text{BGNT}}$
W23	AD32
W24	AD33
W25	$\overline{\text{IDENB}}$
W26	VSS
Y1	VDD3.3
Y2	VDD5
Y3	$\overline{\text{BREQ}}$
Y4	AD31

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
Y23	VDD2.5
Y24	AD34
Y25	VDD5
Y26	VDD3.3
AA1	BCLK
AA2	AD30
AA3	AD29
AA4	AD28
AA23	AD37
AA24	AD36
AA25	AD35
AA26	L_STAT
AB1	AD27
AB2	AD26
AB3	AD25
AB4	VDD2.5
AB23	AD41
AB24	AD40
AB25	AD39
AB26	AD38
AC1	VDD5
AC2	AD24
AC3	$\overline{\text{CBE3}}$
AC4	VDD3.3
AC5	VDD2.5
AC6	VDD2.5
AC7	$\overline{\text{TRDY}}$
AC8	VDD2.5
AC9	PAR
AC10	AD13
AC11	AD10
AC12	$\overline{\text{CBE0}}$
AC13	VSS
AC14	VDD3.3
AC15	AD2
AC16	$\overline{\text{CBE7}}$
AC17	VDD2.5
AC18	AD59

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
AC19	AD61
AC20	AD58
AC21	AD55
AC22	VDD2.5
AC23	VDD3.3
AC24	$\overline{\text{ENUM}}$
AC25	AD42
AC26	VDD5
AD1	IDSEL
AD2	AD23
AD3	VSS
AD4	AD18
AD5	AD17
AD6	$\overline{\text{FRAME}}$
AD7	$\overline{\text{DEVSEL}}$
AD8	$\overline{\text{PERR}}$
AD9	$\overline{\text{CBE1}}$
AD10	AD12
AD11	M66EN
AD12	AD7
AD13	AD5
AD14	VDD2.5
AD15	AD1
AD16	$\overline{\text{ACK64}}$
AD17	$\overline{\text{CBE5}}$
AD18	AD63
AD19	VDD2.5
AD20	AD57
AD21	AD54
AD22	AD52
AD23	AD46
AD24	VSS
AD25	AD44
AD26	AD43
AE1	VSS
AE2	AD22
AE3	AD21
AE4	VDD5

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
AE5	AD16
AE6	$\overline{\text{IRDY}}$
AE7	$\overline{\text{STOP}}$
AE8	$\overline{\text{SERR}}$
AE9	AD15
AE10	AD14
AE11	AD9
AE12	AD6
AE13	AD4
AE14	AD3
AE15	AD0
AE16	$\overline{\text{CBE6}}$
AE17	$\overline{\text{CBE4}}$
AE18	AD62
AE19	AD60
AE20	AD56
AE21	VDD5
AE22	AD51
AE23	AD49
AE24	AD47
AE25	AD45
AE26	VSS
AF1	VDD3.3
AF2	VSS
AF3	AD20
AF4	AD19
AF5	$\overline{\text{CBE2}}$
AF6	VDD5
AF7	VDD3.3
AF8	VSS
AF9	VDD5
AF10	AD11
AF11	AD8
AF12	VDD5
AF13	VDD3.3
AF14	VSS
AF15	$\overline{\text{REQ64}}$
AF16	VDD5

Table 3-1. ISP2312 Pins by Location (Continued)

Solder Ball	Pin Name
AF17	PAR64
AF18	VDD5
AF19	VSS
AF20	VDD3.3
AF21	AD53
AF22	AD50
AF23	AD48
AF24	VDD5
AF25	VSS
AF26	VDD3.3

Table 3-2. ISP2312 Pins by Name

Pin Name	Solder Ball
$\overline{\text{ACK64}}$	AD16
AD0	AE15
AD1	AD15
AD2	AC15
AD3	AE14
AD4	AE13
AD5	AD13
AD6	AE12
AD7	AD12
AD8	AF11
AD9	AE11
AD10	AC11
AD11	AF10
AD12	AD10
AD13	AC10
AD14	AE10
AD15	AE9
AD16	AE5
AD17	AD5
AD18	AD4
AD19	AF4
AD20	AF3
AD21	AE3
AD22	AE2

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
AD23	AD2
AD24	AC2
AD25	AB3
AD26	AB2
AD27	AB1
AD28	AA4
AD29	AA3
AD30	AA2
AD31	Y4
AD32	W23
AD33	W24
AD34	Y24
AD35	AA25
AD36	AA24
AD37	AA23
AD38	AB26
AD39	AB25
AD40	AB24
AD41	AB23
AD42	AC25
AD43	AD26
AD44	AD25
AD45	AE25
AD46	AD23
AD47	AE24
AD48	AF23
AD49	AE23
AD50	AF22
AD51	AE22
AD52	AD22
AD53	AF21
AD54	AD21
AD55	AC21
AD56	AE20
AD57	AD20
AD58	AC20
AD59	AC18
AD60	AE19

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
AD61	AC19
AD62	AE18
AD63	AD18
BCLK	AA1
$\overline{\text{BGNT}}$	W4
$\overline{\text{BREQ}}$	Y3
$\overline{\text{CBE0}}$	AC12
$\overline{\text{CBE1}}$	AD9
$\overline{\text{CBE2}}$	AF5
$\overline{\text{CBE3}}$	AC3
$\overline{\text{CBE4}}$	AE17
$\overline{\text{CBE5}}$	AD17
$\overline{\text{CBE6}}$	AE16
$\overline{\text{CBE7}}$	AC16
CLKOUT_1	E26
CLKOUT_2	C4
$\overline{\text{DEVSEL}}$	AD7
$\overline{\text{ENUM}}$	AC24
$\overline{\text{FLASHCS\_1}}$	B23
$\overline{\text{FLASHCS\_2}}$	C8
$\overline{\text{FLASHOE}}$	D22
$\overline{\text{FLASHWR}}$	A23
$\overline{\text{FRAME}}$	AD6
GPIO_1[0]	D20
GPIO_1[1]	D19
GPIO_1[2]	C20
GPIO_1[3]	C19
GPIO_1[4]	C18
GPIO_1[5]	B21
GPIO_1[6]	B20
GPIO_1[7]	B19
GPIO_2[0]	C5
GPIO_2[1]	B5
GPIO_2[2]	B4
GPIO_2[3]	B3
GPIO_2[4]	B2
GPIO_2[5]	A5
GPIO_2[6]	A4

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
GPIO_2[7]	A3
IDDT	C6
$\overline{\text{IDENB}}$	W25
IDSEL	AD1
IF_1	V23
IF_2	C1
$\overline{\text{INTA}}$	W2
$\overline{\text{INTB}}$	V1
$\overline{\text{IRDY}}$	AE6
LPENB_1	D9
LPENB_2	D7
L_STAT	AA26
M66EN	AD11
NC	A18
NC	B16
NC	C16
NC	D16
NC	N25
NC	V26
NVCLK	A22
NVCS	C21
NVDATI	B22
NVDATO	C22
PAR	AC9
PAR64	AF17
PDATA0	B25
PDATA1	D24
PDATA2	D25
PDATA3	D26
PDATA4	C25
PDATA5	C26
PDATA6	D21
PDATA7	B24
PDATA8	A24
PDATA9	C23
$\overline{\text{PERR}}$	AD8
PLLVDD	V2
PLLVSS	V4

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
RADDR_1[0]	M25
RADDR_1[1]	M26
RADDR_1[2]	L23
RADDR_1[3]	L24
RADDR_1[4]	L25
RADDR_1[5]	L26
RADDR_1[6]	K23
RADDR_1[7]	K24
RADDR_1[8]	K25
RADDR_1[9]	K26
RADDR_1[10]	J23
RADDR_1[11]	J24
RADDR_1[12]	J25
RADDR_1[13]	J26
RADDR_1[14]	H23
RADDR_1[15]	H24
RADDR_1[16]	H25
RADDR_1[17]	G23
RADDR_1[18]	G24
RADDR_1[19]	G25
RADDR_1[20]	F24
RADDR_2[0]	M1
RADDR_2[1]	L3
RADDR_2[2]	L2
RADDR_2[3]	L1
RADDR_2[4]	K4
RADDR_2[5]	K3
RADDR_2[6]	K2
RADDR_2[7]	K1
RADDR_2[8]	J4
RADDR_2[9]	J3
RADDR_2[10]	J2
RADDR_2[11]	J1
RADDR_2[12]	H3
RADDR_2[13]	H2
RADDR_2[14]	G4
RADDR_2[15]	G3
RADDR_2[16]	G2

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
RADDR_2[17]	F3
RADDR_2[18]	F2
RADDR_2[19]	F1
RADDR_2[20]	E4
$\overline{\text{RADDR18\_1}}$	F25
$\overline{\text{RADDR18\_2}}$	E3
$\overline{\text{RADDR19\_1}}$	F26
$\overline{\text{RADDR19\_2}}$	E2
$\overline{\text{RADDR20\_1}}$	E23
$\overline{\text{RADDR20\_2}}$	D3
RDATA_1[0]	V25
RDATA_1[1]	U23
RDATA_1[2]	U24
RDATA_1[3]	U25
RDATA_1[4]	U26
RDATA_1[5]	T24
RDATA_1[6]	T25
RDATA_1[7]	T26
RDATA_1[8]	R23
RDATA_1[9]	R24
RDATA_1[10]	R25
RDATA_1[11]	R26
RDATA_1[12]	P24
RDATA_1[13]	P25
RDATA_1[14]	N24
RDATA_1[15]	M23
RDATA_2[0]	U4
RDATA_2[1]	U3
RDATA_2[2]	U2
RDATA_2[3]	U1
RDATA_2[4]	T3
RDATA_2[5]	T2
RDATA_2[6]	T1
RDATA_2[7]	R4
RDATA_2[8]	R3
RDATA_2[9]	R2
RDATA_2[10]	R1
RDATA_2[11]	P2

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
RDATA_2[12]	N3
RDATA_2[13]	N2
RDATA_2[14]	M4
RDATA_2[15]	M3
RDPAR_1	M24
RDPAR_2	M2
REFCLK1	E1
REFCLK2	A21
$\overline{\text{REQ64}}$	AF15
$\overline{\text{RESET}}$	W3
RISCSTB_1	E25
RISCSTB_2	D2
$\overline{\text{ROE\_1}}$	E24
$\overline{\text{ROE\_2}}$	D1
RXBVDD_1	D15
RXBVDD_2	C11
RXBVSS_1	C17
RXBVSS_2	D12
RXN_1	B17
RXN_2	B12
RXP_1	A17
RXP_2	A12
RXVDD_1	D17
RXVDD_2	C12
RXVSS_1	B18
RXVSS_2	B13
SCAN_ENABLE	B7
SCAN_TEST_MODE	B6
$\overline{\text{SERR}}$	AE8
$\overline{\text{STOP}}$	AE7
TCK	C7
TDI	C9
TDO	B8
TMS	B9
$\overline{\text{TRDY}}$	AC7
TRIMRES_1	C13
TRIMRES_2	A10
$\overline{\text{TRST}}$	A9

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
TSTOUT	A6
TXBVDD_1	C15
TXBVDD_2	D11
TXBVSS_1	C14
TXBVSS_2	C10
TXN_1	A16
TXN_2	A11
TXP_1	B15
TXP_2	B11
TXVDD_1	B14
TXVDD_2	D10
TXVSS_1	A15
TXVSS_2	B10
VDD2.5	D5
VDD2.5	D6
VDD2.5	D8
VDD2.5	D18
VDD2.5	F4
VDD2.5	F23
VDD2.5	H4
VDD2.5	L4
VDD2.5	P3
VDD2.5	T4
VDD2.5	T23
VDD2.5	V3
VDD2.5	Y23
VDD2.5	AB4
VDD2.5	AC5
VDD2.5	AC6
VDD2.5	AC8
VDD2.5	AC17
VDD2.5	AC22
VDD2.5	AD14
VDD2.5	AD19
VDD3.3	A7
VDD3.3	A14
VDD3.3	A20
VDD3.3	A26

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
VDD3.3	D4
VDD3.3	D13
VDD3.3	D23
VDD3.3	G1
VDD3.3	G26
VDD3.3	N1
VDD3.3	N23
VDD3.3	P4
VDD3.3	P26
VDD3.3	Y1
VDD3.3	Y26
VDD3.3	AC4
VDD3.3	AC14
VDD3.3	AC23
VDD3.3	AF1
VDD3.3	AF7
VDD3.3	AF13
VDD3.3	AF20
VDD3.3	AF26
VDD5	Y2
VDD5	Y25
VDD5	AC1
VDD5	AC26
VDD5	AE4
VDD5	AE21
VDD5	AF6
VDD5	AF9
VDD5	AF12
VDD5	AF16
VDD5	AF18
VDD5	AF24
VSS	A1
VSS	A2
VSS	A8
VSS	A13
VSS	A19
VSS	A25
VSS	B1

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
VSS	B26
VSS	C3
VSS	C24
VSS	D14
VSS	H1
VSS	H26
VSS	L11
VSS	L12
VSS	L13
VSS	L14
VSS	L15
VSS	L16
VSS	M11
VSS	M12
VSS	M13
VSS	M14
VSS	M15
VSS	M16
VSS	N4
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N15
VSS	N16
VSS	N26
VSS	P1
VSS	P11
VSS	P12
VSS	P13
VSS	P14
VSS	P15
VSS	P16
VSS	P23
VSS	R11
VSS	R12
VSS	R13
VSS	R14

Table 3-2. ISP2312 Pins by Name (Continued)

Pin Name	Solder Ball
VSS	R15
VSS	R16
VSS	T11
VSS	T12
VSS	T13
VSS	T14
VSS	T15
VSS	T16
VSS	W1
VSS	W26
VSS	AC13
VSS	AD3
VSS	AD24
VSS	AE1
VSS	AE26
VSS	AF2
VSS	AF8
VSS	AF14
VSS	AF19
VSS	AF25
$\overline{\text{WE\_1}}$	V24
$\overline{\text{WE\_2}}$	C2

3.2 Pin Descriptions

This section summarizes the pins on the ISP2312. The following tables contain the pin name, pin number, pin type (i.e., CMOS input, etc.) and a brief description of each pin. The ISP2312 pins described in this section are arranged in the following categories:

- Fibre channel serial interfaces 1 and 2 pins
- RISC interfaces 1 and 2 pins
- Flash BIOS 1 and 2 pins
- NVRAM interface pins
- PCI bus interface pins
- JTAG pins
- Miscellaneous pins
- Power and ground pins

In the *Type* column of the following pin description tables, input pins are indicated by *I,* output pins are indicated by *O,* bidirectional pins are indicated by *I/O*, power inputs are indicated by *PWR*, and ground lines are indicated by *GND*. Active-low pin names are written with an overbar.

NOTE:

- Unused inputs that do not have an internal pull-up or pull-down must be pulled to ground (or power, as appropriate) through a resistor.
- No connect (NC) pins must not be connected (no external connections).

Table 3-3 defines the pin electrical characteristics listed in the *Driver* and *Receiver* columns of the following pin description tables.

Table 3-3. Pin Electrical Characteristics

Symbol	Definition
Drivers	
C-4	CMOS output. 4-mA drive
C-4, TRI	CMOS output. 4-mA drive. Tristate
C-6	CMOS output. 6-mA drive
C-8	CMOS output. 8-mA drive
C-12	CMOS output. 12-mA drive
GTX	Gigabit transceiver transmit output differential pair
PCI	Special PCI bus pad
PROC_DRV	Process monitor cell
Receivers	
A	Analog input
GRX	Gigabit transceiver receive input differential pair
PCI	Special PCI bus pad
LVTTL	Low-voltage TTL input levels. No internal pull-up or pull-down
LVTTL-U	Low-voltage TTL input levels. Internal pul-lup
LVTTL-D	Low-voltage TTL input levels. Internal pull-down

3.2.1
Fibre Channel Serial Interfaces 1 and 2 Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
RXN_1	B17	I		GRX	RECEIVE SERIAL DATA IN PAIR. These pins carry serial data from the Fibre Channel interface into the ISP2312 chip at 1.0625 Gbps or 2.125 Gbps, as determined by the serial link.
RXN_2	B12	I			
RXP_1	A17	I			
RXP_2	A12	I			
TRIMRES_1	C13	I		A	TRIM RESISTORS. These pins provide the trimming circuit input to set the desired internal termination resistance. TRIMRES_1/ TRIMRES_2 must be connected to RXVDD through a 2.74k-ohm (±1 percent) resistor.
TRIMRES_2	A10	I			
TXN_1	A16	O	GTX		TRANSMIT SERIAL DATA OUT PAIR. These pins carry serial data from the ISP2312 chip to the Fibre Channel interface at 1.0625 Gbps or 2.125 Gbps, as determined by the serial link.
TXN_2	A11	O			
TXP_1	B15	O			
TXP_2	B11	O			

3.2.2
RISC Interfaces 1 and 2 Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
CLKOUT_1	E26	O	C-12		CLOCK OUT. These pins provide the synchronous clock to the external RISC SRAM.
CLKOUT_2	C4	O			
IF_1	V23	O	C-8		INSTRUCTION FETCH. These pins indicate that the current RISC processor memory cycle is an instruction fetch. These pins are used with RISCSTB_1 and RISCSTB_2 for debugging purposes.
IF_2	C1	O			
RADDR_1[0–20]	M25–26, L23–26, K23–26, J23–26, H23–25, G23–25, F24	O	C-12		RISC MEMORY ADDRESS BUS. These pins are driven during all memory cycles for both internal and external memory accesses. During BIOS accesses on the PCI bus, the RADDR_1[0–16] and RADDR_2[0–16] pins drive the flash BIOS address bits.
RADDR_2[0–20]	M1, L3–1, K4–1, J4–1, H3–2, G4–2, F3–1, E4	O			
$\overline{\text{RADDR18–20\_1}}$	F25–26, E23	O	C-12		INVERTED RISC MEMORY ADDRESS BUS. These pins are used only for debug purposes.
$\overline{\text{RADDR18–20\_2}}$	E3–2, D3				
RDATA_1[0–15]	V25, U23–26, T24–26, R23–26, P24–25, N24, M23	I/O	C-8	LVTTL-U	RISC DATA BUS. Data is transferred over these lines during external RISC memory cycles.
RDATA_2[0–15]	U4–1, T3–1, R4–1, P2, N3–2, M4–3	I/O	C-8	LVTTL-U	
RDPAR_1	M24	I/O	C-8	LVTTL	RISC DATA PARITY. These pins provide odd parity for the RISC data bus.
RDPAR_2	M2				

Pin Name	Solder Ball	Type	Driver	Receiver	Description
RISCSTB_1 RISCSTB_2	E25 D2	O O	C-8		RISC STROBE. These pins indicate that instruction or literal data will be loaded on the next clock edge. These pins are used for debugging purposes to trace RISC processor program execution.
$\overline{\text{ROE\_1}}$ $\overline{\text{ROE\_2}}$	E24 D1	O O	C-12		RAM OUTPUT ENABLE. These pins enable the external SRAM to output data. They must be connected to SRAM $\overline{\text{OE}}$.
$\overline{\text{WE\_1}}$ $\overline{\text{WE\_2}}$	V24 C2	O O	C-12		WRITE ENABLE. When $\overline{\text{WE\_1}}$ or $\overline{\text{WE\_2}}$ is active, data is written to memory. When $\overline{\text{WE\_1}}$ or $\overline{\text{WE\_2}}$ is inactive, data is read from memory.

3.2.3
Flash BIOS 1 and 2 Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
$\overline{\text{FLASHCS\_1}}$ $\overline{\text{FLASHCS\_2}}$	B23 C8	I/O I/O	C-4	LVTTL-U	FLASH CHIP SELECT. These pins are asserted by the ISP2312 to select the flash EPROM device during host accesses to the BIOS EPROM.
$\overline{\text{FLASHOE}}$	D22	I/O	C-4	LVTTL-U	FLASH OUTPUT ENABLE. This pin is asserted by the ISP2312 to read the flash EPROM device when the host performs a read access to the BIOS EPROM.
$\overline{\text{FLASHWR}}$	A23	I/O	C-8	LVTTL-U	FLASH WRITE. This pin is asserted by the ISP2312 to write to the flash EPROM device when the host performs a write access to the BIOS EPROM.
PDATA0–7	B25, D24–26, C25–26, D21, B24	I/O	C-4	LVTTL-D	BIOS PROM DATA BUS. These pins read and write the BIOS PROM data. The ISP2312 internally routes this data to the PCI bus. PDATA0–7 are also used as sense input pins (see section 12). PDATA8–9 are used for production testing (see section 3.2.7).

3.2.4
NVRAM Interface Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
$\overline{\text{IDENB}}$	W25	I		LVTTL	ENABLE SUBSYSTEM ID LOAD. This pin enables or disables loading of the PCI subsystem ID registers from the external NVRAM after power-up reset is released. When the pin is pulled down to VSS during power-up reset, the PCI subsystem ID registers are loaded from the NVRAM. During subsystem ID loading, any attempt from the host to access the ISP2312 is terminated with a disconnect and retry response from the ISP2312.
NVCLK	A22	I/O	C-4	LVTTL-D	NONVOLATILE RAM CLOCK. This pin is part of the four-bit NVRAM interface (93C66); it serially clocks data in and out of the NVRAM.
NVCS	C21	I/O	C-4	LVTTL-D	NONVOLATILE RAM CHIP SELECT. This pin, as an output, is part of the four-bit NVRAM interface (93C66); it selects the NVRAM for data read and write operations.
NVDATI	B22	I		LVTTL-D	NONVOLATILE RAM DATA IN. This pin is part of the four-bit NVRAM interface (93C66); it reads data from the NVRAM to the ISP2312. The data is read serially from the NVRAM one bit at a time.
NVDATO	C22	I/O	C-4	LVTTL-D	NONVOLATILE RAM DATA OUT. This pin is part of the four-bit NVRAM interface (93C66); it writes data to the NVRAM from the ISP2312. The data is written serially to the NVRAM one bit at a time. NVDATO is also used as an input sense pin during PCI bus reset (see section 12).

3.2.5
PCI Bus Interface Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
$\overline{\text{ACK64}}$	AD16	I/O	PCI	PCI	PCI BUS 64-BIT ACKNOWLEDGE. The ISP2312, as an initiator, monitors this pin after initiating 64-bit data transfers on the PCI bus to check if the target of the transaction can accept a 64-bit data transfer request. In PCI-X bus mode, the ISP2312 also drives this pin as a target of a split completion transaction, depending on the state of the $\overline{\text{REQ64}}$ input.
AD0–63	AE15, AD15, AC15, AE14–13, AD13, AE12, AD12, AF11, AE11, AC11, AF10, AD10, AC10, AE10–9, AE5, AD5–4, AF4–3, AE3–2, AD2, AC2, AB3–1, AA4–2, Y4, W23–24, Y24, AA25–23, AB26–23, AC25, AD26–25, AE25, AD23, AE24, AF23, AE23, AF22, AE22, AD22, AF21, AD21, AC21, AE20, AD20, AC20, AC18, AE19, AC19, AE18, AD18	I/O	PCI	PCI	PCI ADDRESS AND DATA. These pins carry multiplexed address, attribute, and data information on the PCI bus. During the first clock of the PCI bus cycle (address phase), the AD0–31 pins carry the physical address. During the second clock of the PCI bus cycle (attribute phase), the AD0–31 pins carry transaction attribute information in PCI-X bus mode. During subsequent clocks of the PCI bus cycle (data phases, including second clock in conventional PCI bus mode), the AD0–63 pins carry data. During the address phase of the PCI bus cycle, the ISP2312 receives the address as an input when acting as a PCI bus target. When acting as a PCI bus master, the chip drives the address on the AD0–31 pins. During the attribute phase, the ISP2312 drives or receives additional information related to the transaction, for example, requester ID and byte count, that further defines the transaction on the AD0–31 pins. During the data phase of the PCI bus cycle, the ISP2312 drives or receives data depending on the type of bus transaction (read or write). The AD0–7 pins carry the least significant byte of data; the AD56–63 pins carry the most significant byte.
BCLK	AA1	I		PCI	PCI BUS CLOCK. This pin provides timing and synchronization of control pins and data transfers on the PCI bus. The maximum PCI bus clock frequency allowed by the ISP2312 is 66 MHz in conventional PCI bus mode and 133 MHz in PCI-X bus mode.
$\overline{\text{BGNT}}$	W4	I		PCI	PCI BUS GRANT. This pin indicates that the ISP2312 has been granted ownership of the PCI bus. After receiving $\overline{\text{BGNT}}$, the ISP2312 waits for the PCI bus to become idle before acting as a PCI bus master.
$\overline{\text{BREQ}}$	Y3	O	PCI		PCI BUS REQUEST. This pin requests ownership of the PCI bus. The ISP2312 asserts this pin in response to a transfer request by an ISP2312 DMA channel.

Pin Name	Solder Ball	Type	Driver	Receiver	Description
$\overline{\text{CBE0–7}}$	AC12, AD9, AF5, AC3, AE17, AD17, AE16, AC16	I/O	PCI	PCI	PCI COMMAND/BYTE ENABLE. The PCI bus command, attribute, and byte enable information are multiplexed on the same pins. During the address phase of a transaction, the $\overline{\text{CBE0–3}}$ pins define the bus command. During the attribute phase of a transaction (PCI-X bus mode only), the $\overline{\text{CBE0–3}}$ pins carry the byte count or byte enable information, depending on the type of transaction. During the data phase, the $\overline{\text{CBE0–7}}$ pins carry byte enables information (in conventional PCI bus mode) and memory write transactions (in PCI-X bus mode). The byte lane information determines which byte lanes carry meaningful data.
$\overline{\text{DEVSEL}}$	AD7	I/O	PCI	PCI	PCI BUS DEVICE SELECT. This pin is asserted by the ISP2312 when accessed as a target on the PCI bus. The chip drives $\overline{\text{DEVSEL}}$ active (medium speed) after decoding a valid address that maps into the ISP2312 address space or after decoding a configuration cycle that has an active IDSEL pin. When acting as a PCI bus master, the ISP2312 monitors $\overline{\text{DEVSEL}}$ to check if any device on the bus is selected as a PCI target.
$\overline{\text{ENUM}}$	AC24	O	PCI		COMPACTPCI HOST SWAP EVENT INTERRUPT. This open-drain signal is asserted (low) to indicate that the PCI board is either inserted and ready for initialization or about to be removed. The signal is deasserted when the host clears the Hot Swap Insertion or Extraction Event bit (CompactPCI Hot Swap Control and Status register bit 7 or 6). The host can also mask the generation of this interrupt by setting the Hot Swap Event Interrupt Mask bit (CompactPCI Hot Swap Control and Status register bit 1) to 1. $\overline{\text{ENUM}}$ requires an external pull-up resistor.
$\overline{\text{FRAME}}$	AD6	I/O	PCI	PCI	PCI BUS FRAME. This pin is asserted when the chip acts as a PCI bus master. The ISP2312 asserts $\overline{\text{FRAME}}$ to indicate the beginning of a bus transaction. $\overline{\text{FRAME}}$ remains asserted throughout the data transfer and is negated when the data transfer reaches the final data phase. The ISP2312 receives this pin as an input when the chip acts as a PCI bus target. As a target, the ISP2312 latches command and address information ($\overline{\text{CBE0–7}}$, AD0–63) when $\overline{\text{FRAME}}$ is asserted by the PCI bus master.
IDSEL	AD1	I		PCI	PCI BUS INITIALIZATION DEVICE SELECT. This pin is the ISP2312 chip select during PCI configuration read and write bus transactions.

Pin Name	Solder Ball	Type	Driver	Receiver	Description
$\overline{\text{INTA}}$ $\overline{\text{INTB}}$	W2 V1	O O	PCI PCI		PCI BUS INTERRUPT. These open-drain pins asynchronously interrupt the host. The host can disable this request and instead poll an interrupt bit in the ISP to PCI Interrupt Status register. The $\overline{\text{INTA}}$ pin generates an interrupt from function 0/port 1. The $\overline{\text{INTB}}$ pin generates an interrupt from function 1/port 2.
$\overline{\text{IRDY}}$	AE6	I/O	PCI	PCI	PCI BUS INITIATOR READY. This pin is asserted when the chip acts as a PCI bus master. The ISP2312 asserts $\overline{\text{IRDY}}$ to indicate its ability to complete the current data phase of a bus transaction. When the ISP2312 performs a write transaction on the PCI bus, it activates $\overline{\text{IRDY}}$ after driving valid data on the PCI bus. When the ISP2312 performs a read transaction on the PCI bus, it activates $\overline{\text{IRDY}}$ when the chip is prepared to accept data from the PCI bus target. The ISP2312 receives $\overline{\text{IRDY}}$ as an input pin when acting as a PCI bus target. During PCI bus write transactions to the ISP2312 as a target, the ISP2312 accepts data only when $\overline{\text{IRDY}}$ is active. During PCI bus read transactions to the ISP2312 as a target, the ISP2312 holds valid data on the bus until $\overline{\text{IRDY}}$ is active.
M66EN	AD11	I		LVTTL	PCI 66 MHZ ENABLE. The M66EN is an input pin to the ISP2312. When M66EN input is at logic level 1, the ISP2312 operates in conventional PCI 66-MHz mode; when M66EN input is at logic level 0, the ISP2312 operates in conventional PCI 33-MHz mode. When the ISP2312 operates at a maximum PCI bus frequency of 33-MHz, M66EN must be connected to ground.

Pin Name	Solder Ball	Type	Driver	Receiver	Description
PAR	AC9	I/O	PCI	PCI	PCI BUS PARITY. This pin carries even parity across the AD0–31 and CBE0–3 pins. During address phases, it covers parity across command and address lines. During the attribute phase in PCI-X bus mode, it covers parity across 36-bit attribute information. During data phases, it covers parity across byte enables and data lines. The PAR pin is delayed one PCI clock from the corresponding address, attribute, and data phases. When acting as a PCI bus master, the ISP2312 drives PAR during address, attribute (PCI-X bus mode only), and data phases for PCI bus write transactions and during address and attribute (PCI-X bus mode only) phases for PCI bus read transactions. As a PCI bus master, the ISP2312 receives PAR during the data phases of PCI bus read transactions and performs a check for even parity. When acting as a PCI bus target, the ISP2312 receives PAR (to perform a parity check) during address, attribute (PCI-X bus mode only) and data phases for PCI bus write transactions and during address and attribute (PCI-X bus mode only) phases for PCI bus read transactions. As a PCI bus target, the ISP2312 drives PAR for the data phases during PCI bus read transactions.
PAR64	AF17	I/O	PCI	PCI	PCI BUS PARITY FOR 64-BIT EXTENSIONS. This pin carries even parity across the AD32–63 and CBE4–7 pins. The PAR64 pin is delayed one PCI clock from the corresponding address, attribute (PCI-X bus mode only), and data phases. When acting as a PCI bus master, the ISP2312 drives PAR64 during address, attribute (PCI-X bus mode only) and data phases for PCI bus write transactions and during address and attribute (PCI-X bus mode only) phases for PCI bus read transactions. As a PCI bus master, the ISP2312 receives PAR64 during the data phases of PCI bus read transactions and performs a check for even parity. When acting as a PCI target, the ISP2312 checks PAR64 for even parity during PCI-X mode split completion transactions when the bus size of the transaction is 64 bits.
$\overline{\text{PERR}}$	AD8	I/O	PCI	PCI	PCI PARITY ERROR. When acting as a PCI bus target, the ISP2312 asserts this pin to indicate detection of parity errors across byte enable and data fields during PCI bus write transactions. When acting as a PCI bus master, the ISP2312 monitors the pin for parity error indication from the PCI bus target or asserts this pin when it detects parity errors and parity checking is enabled.

Pin Name	Solder Ball	Type	Driver	Receiver	Description
REQ64	AF15	I/O	PCI	PCI	PCI BUS 64-BIT TRANSFER REQUEST. This pin is asserted when the chip acts as a 64-bit PCI bus master. The ISP2312 asserts REQ64 to indicate the beginning of a 64-bit transfer request. REQ64 remains asserted throughout the data transfer and is negated when the data transfer reaches the final data phase. The ISP2312 monitors this pin as an input during the PCI-X split completion transaction to determine the width of the transaction. When REQ64 is asserted, the ISP2312 responds with an ACK64 assertion and transfers data in 64-bit mode. The REQ64 signal is also used as a power-up reset sense input to determine the width of the PCI bus slot. When REQ64 is sampled active at the end of the PCI reset (RESET deassertion), the ISP2312 is connected to a 64-bit PCI bus; otherwise, it is connected to a 32-bit PCI bus.
SERR	AE8	I/O	PCI	PCI	PCI SYSTEM ERROR. The ISP2312 asserts this open-drain signal to report a fatal error when the System Error Enable bit (PCI Command register bit 8) is set. The signal is asserted under the following conditions: ■ The ISP2312 detects a parity error across the command and address field during the address phase of a PCI bus transaction. ■ The ISP2312 detects a parity error during the attribute phase of a PCI-X bus transaction. ■ The ISP2312, during a master mode Message Signaled Interrupts (MSI) transaction, receives a master abort, target abort, or PERR (data parity error detected) from the PCI target. ■ The ISP2312, during PCI-X master mode and split completion transactions, detects a data parity error (parity error on read data read and PERR on write data) and the Data Parity Error Recovery Enable bit (PCI-X Command register bit 0) is 0. Under the first two conditions, the ISP2312 also terminates the transaction with a target abort condition.

Pin Name	Solder Ball	Type	Driver	Receiver	Description
$\overline{\text{STOP}}$	AE7	I/O	PCI	PCI	PCI BUS STOP. When acting as a PCI bus target, the ISP2312 asserts this pin to disconnect or abort PCI bus transactions. When acting as a PCI bus master, the ISP2312 also samples $\overline{\text{STOP}}$ to see if the target wants to disconnect, retry, or abort the transaction. After detecting $\overline{\text{STOP}}$, the ISP2312 releases ownership of the PCI bus.
$\overline{\text{TRDY}}$	AC7	I/O	PCI	PCI	PCI BUS TARGET READY. When acting as a PCI bus target, the ISP2312 asserts this pin to complete the current data phase of a bus transaction. During PCI bus read transactions as a target to the ISP2312, the chip asserts $\overline{\text{TRDY}}$ when valid data is driven onto the PCI bus. During PCI bus write transactions, the ISP2312 asserts $\overline{\text{TRDY}}$ when it has accepted the data. The ISP2312 receives this pin as an input when acting as a PCI bus master. When the ISP2312 performs read transactions on the PCI bus as a PCI bus master, data is accepted only when the chip samples $\overline{\text{TRDY}}$ active from the PCI target. When the ISP2312 performs write transactions, it drives valid data on the bus until $\overline{\text{TRDY}}$ from the target is sampled active.

3.2.6
JTAG Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
TCK	C7	I		LVTTL-D	JTAG CLOCK. This pin clocks state information and test data into and out of the device during testing.
TDI	C9	I		LVTTL-D	JTAG DATA IN. The JTAG input serially shifts test data and test instructions into the ISP2312 during test access port operation.
TDO	B8	O	C-4, TRI		JTAG DATA OUT. The JTAG output serially shifts test data and test instructions out of the ISP2312 during test access port operation.
TMS	B9	I		LVTTL-U	JTAG MODE SELECTION. This pin controls the state of the test access port controller on the ISP2312.
$\overline{\text{TRST}}$	A9	I		LVTTL-D	JTAG RESET. This pin resets the JTAG controller.

3.2.7
Miscellaneous Pins

Pin Name	Solder Ball	Type	Driver	Receiver	Description
IDDT	C6	I		—	IDDT. This signal is used only for production testing and must be pulled low.
GPIO_1[0–7] GPIO_2[0–7]	D20–19, C20–18, B21–19 C5, B5–2, A5–3	I/O I/O	C-8	LVTTL-U	GENERAL PURPOSE I/O. These pins can be programmed as input (default) or output. The RISC and host processors use these pins as output (to control) or as input (to read) status information from external devices. ***NOTE:*** For QLogic HBA designs, the GPIO_1[0, 7–6] and GPIO_2[0, 7–6] pins are programmed to control the LEDs on the HBA. These pins are controlled by the RISC firmware to indicate I/O activity and status information. To maintain firmware compatibility, these signals must not be used for any other purpose.
LPENB_1 LPENB_2	D9 D7	I/O I/O	C-4	LVTTL-D	LOOP PORT ENABLE. These pins control the external port bypass circuit. When LPENB_1–2 are high, the bypass circuit is disabled and the FPM can transmit to the Fibre Channel. These pins are also used as sense input pins during PCI bus reset (see section 12).
L_STAT	AA26	I/O	PCI	PCI	COMPACTPCI HOT SWAP LED CONTROL/SWITCH STATUS. As an input, this signal indicates the state of the ejector switch used for insertion and removal of the board. When the ejector switch is closed after board insertion, L_STAT transitions from low to high. The ISP2312 uses this state change on L_STAT to set the Hot Swap Insertion or Extraction Event bit (CompactPCI Hot Swap Control and Status register bit 7 or 6). The ISP2312 tristates this signal until it detects a hot swap event. When the event is detected, the ISP2312 drives the L_STAT pin. As an output, this pin controls the hot swap LED. When the Hot Swap LED On/Off bit (CompactPCI Hot Swap Control and Status register bit 3) is set to 1, L_STAT is driven high and the hot swap LED is forced on.
NC	A18, B16, C16, D16, N25, V26	—	—	—	NO CONNECT. These pins are not connected.
PDATA8–9	A24, C23	I/O	C-4	LVTTL-D	BIOS PROM DATA. These signals are used only for production testing and debugging. PDATA0–7 read and write to the PROM data bus (see section 3.2.3).
REFCLK1	E1	I		LVTTL	REFERENCE CLOCK 1. This pin provides a 106.25-MHz reference clock for channels 1 and 2. It can also be used for the RISC processor clocks.

Pin Name	Solder Ball	Type	Driver	Receiver	Description
REFCLK2	A21	I		LVTTL	REFERENCE CLOCK 2. This pin is reserved. It must be pulled down to ground through a 330-ohm resistor.
$\overline{\text{RESET}}$	W3	I		PCI	POWER RESET. This is the asynchronous reset pin for the entire chip. All tristate outputs are disabled while $\overline{\text{RESET}}$ is active. ***NOTE:*** Do not use this pin in JTAG mode, since it tristates all I/O and output buffers.
SCAN_ENABLE	B7	I		LVTTL-D	SCAN ENABLE. This signal is used only for production testing.
SCAN_TEST_ MODE	B6	I		LVTTL-D	SCAN TEST MODE. This signal is used only for production testing.
TSTOUT	A6	O	PROC _DRV		TEST OUT. This signal is used only for production testing.

3.2.8
Power and Ground Pins

Pin Name	Solder Ball	Type	Description
PLLVDD	V2	PWR	PLL POWER. This pin supplies 2.5-volt power to the onboard PLL circuit.
PLLVSS	V4	GND	PLL GROUND. This pin provides ground for the onboard PLL circuit.
RXBVDD_1 RXBVDD_2	D15 C11	PWR PWR	RECEIVER ANALOG INPUT STAGE POWER. These pins supply 2.5-volt power to the input stage of the GSL receiver's analog section and to the RX buffer.
RXBVSS_1 RXBVSS_2	C17 D12	GND GND	RECEIVER ANALOG INPUT STAGE GROUND. These pins connect the input stage of the GSL receiver's analog section and the RX buffer to ground.
RXVDD_1 RXVDD_2	D17 C12	PWR PWR	RECEIVER ANALOG SECTION POWER. These pins supply 2.5-volt power to part of the GSL receiver's analog section.
RXVSS_1 RXVSS_2	B18 B13	GND GND	RECEIVER ANALOG SECTION GROUND. These pins connect part of the GSL receiver's analog section to ground.
TXBVDD_1 TXBVDD_2	C15 D11	PWR PWR	TRANSMITTER ANALOG OUTPUT STAGE POWER. These pins supply 2.5-volt power to the output stage of the GSL transmitter's analog section and to the TX buffer.
TXBVSS_1 TXBVSS_2	C14 C10	GND GND	TRANSMITTER ANALOG OUTPUT STAGE GROUND. This pin connects the output stage of the GSL transmitter's analog section the TX buffer to ground.
TXVDD_1 TXVDD_2	B14 D10	PWR PWR	TRANSMITTER ANALOG SECTION POWER. This pin supplies 2.5-volt power to part of the GSL transmitter's analog section.
TXVSS_1 TXVSS_2	A15 B10	GND GND	TRANSMITTER ANALOG SECTION GROUND. These pins connect part of the GSL transmitter's analog section to ground.
VDD2.5	See note a	PWR	CORE POWER. These pins provide power to the ISP2312 core.
VDD3.3	See note b	PWR	I/O POWER. These pins provide power to the ISP2312 drivers and receivers.

Pin Name	Solder Ball	Type	Description
VDD5	See note c	PWR	PCI CLAMP VOLTAGE INPUT. These pins are +5 V for a 5-volt PCI signaling environment and +3.3 V for a 3-volt PCI signaling environment. These pins can be connected to the PCI VIO pins to automatically switch to the correct voltage levels.
VSS	See note d	GND	GROUND

Table Notes

[a]VDD2.5 = D5–6, D8, D18, F4, F23, H4, L4, P3, T4, T23, V3, Y23, AB4, AC5–6, AC8, AC17, AC22, AD14, AD19

[b]VDD3.3 = A7, A14, A20, A26, D4, D13, D23, G1, G26, N1, N23, P4, P26, Y1, Y26, AC4, AC14, AC23, AF1, AF7, AF13, AF20, AF26

[c]VDD5 = Y2, Y25, AC1, AC26, AE4, AE21, AF6, AF9, AF12, AF16, AF18, AF24

[d]VSS = A1–2, A8, A13, A19, A25, B1, B26, C3, C24, D14, H1, H26, L11–16, M11–16, N4, N11–16, N26, P1, P11–16, P23, R11–16, T11–16, W1, W26, AC13, AD3, AD24, AE1, AE26, AF2, AF8, AF14, AF19, AF25

Section 4
Power Connections

4.1 Introduction

The ISP2312 has both analog and digital power input pins, as well as a current bias reference input. These inputs must be generated and filtered properly due to the high frequency signals employed within the chip.

4.2 Compatibility with Future ISP2312 Family Devices

To accommodate future versions of the ISP2312 family, QLogic recommends that the PCB be designed such that 2.5-V power supplies are easily changed to 1.8-V power supplies. Current and voltage tolerances remain the same.

4.3 Digital Power

The digital power pins are named VDD2.5 and VDD3.3. See section 3 for pin numbers. These power pins see table 4-1 must be connected to a common power plane.

Table 4-1. Digital Power Pin Input Requirements

Parameter	Value
Voltage for VDD2.5	2.5 V ± 5 percent
Power	2.4 watts[a]
Ripple (noise)	100 mV peak-to-peak maximum
Voltage for VDD3.3	3.3 V ± 5 percent
Power	1.0 watts[a]
Ripple (noise)	100 mV peak-to-peak maximum

Table Notes
[a]Preliminary estimate

NOTE: There must be at least six 1-nF decoupling capacitors between VDD2.5 and ground. There must be at least six 1-nf decoupling capacitors between VDD3.3 and ground.

4.4 Analog Power

The analog power inputs supply power to the gigabit transceivers on the ISP2312. Due to the high frequencies involved, these inputs are more sensitive than normal digital inputs. Please follow the recommendations in the following sections.

4.4.1 Analog Power Input Requirements

The analog power pins listed below must meet the requirements listed in table 4-2.

- PLLVDD
- RXBVDD_1, RXBVDD_2/RXVDD_1, RXVDD_2
- TXBVDD_1, TXBVDD_2/TXVDD_1, TXVDD_2

Table 4-2. Analog Power Input Requirements

Parameter	Value
Voltage	2.5 V ± 5 percent
Current	80 mA maximum[a]

Table Notes
[a]Preliminary estimate

4.4.2 Analog Power Input Filtering Requirements

The analog power pins supply voltage and current to the analog sections of the ISP2312 chip. These areas of the chip involve very high-speed signals and analog functions and can be sensitive to noise on the analog power inputs. Consequently, the analog power pins must be individually filtered to keep the power inputs as free of noise as possible.

Make sure the decoupling is done according to the circuit diagram in figure 4-1. The filters must be located as close to the ASIC pins as the layout permits, with the 470-pF capacitor right at the pin.

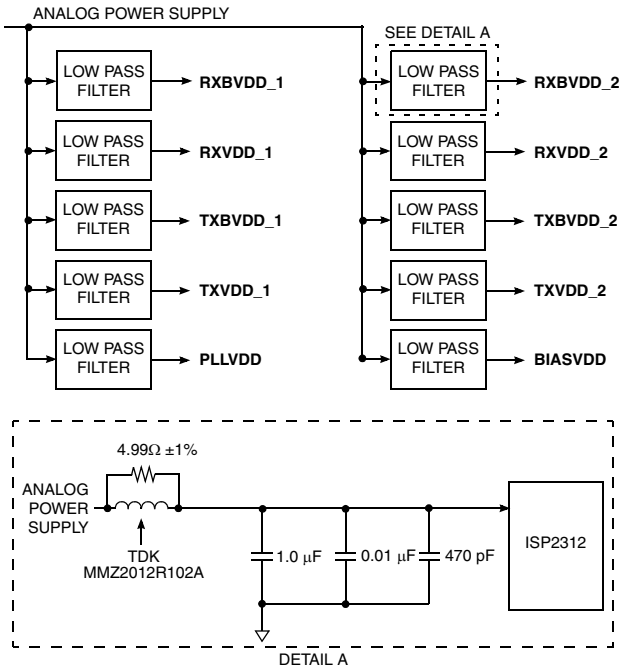


Figure 4-1. Analog Power Decoupling

4.5 PCI Clamp Voltage Input

The ISP2312 works in either a 5.0-V or 3.3-V PCI signaling environment. The signaling environment in a standard PCI environment is determined by the voltage present on the V I/O connector pins (see the universal board connector table in the *PCI Local Bus Specification*). When the voltage on these pins is 3.3 V, then the signaling environment is 3.3 V. When the voltage on these pins is 5.0 V, then the signaling environment is 5.0 V.

The ISP2312 VDD5 power input pins provide clamp voltage to the PCI I/O buffers. The supported voltages are 3.3 V or 5.0 V. The voltage supplied on the PCI connector V I/O pins is applied to the VDD5 pins, which ensures that the ISP2312 uses the correct clamp voltage.

In a custom environment or a motherboard application, the appropriate voltage is applied to the VDD5 pins for the signaling environment being used.

4.6 Power Sequencing Recommendations

NOTE: The voltages listed in this section include the PCI clamp voltage (V I/O pin of a PCI connector).

The ISP2312 VDD5 pins are connected to the PCI buffer clamp. VDD5 must be connected to 5.0 V in a 5-V signaling environment and to 3.3 V in a 3.3-V signaling environment. The V I/O pin on a universal PCI PCB can also supply this voltage.

PCBs should derive VDD3.3 power from a 5.0-V power supply with an onboard 3.3-V power source, as the voltage tolerances required for the ISP2312 are ± 5 percent.

To minimize current and voltage stress on the ISP2312, QLogic recommends that the following power sequencing guidelines be observed during chip power up:

- All voltages must rise continuously from 0.0 V until they reach their regulated voltage.
- The rise time on all voltage supplies (measured from 10 to 90 percent of the regulated voltage) must be in the range of 2 ms to 50 ms.
- During the power-up sequence, all voltages must track within 1 V of each other until each reaches its regulated level.

- The voltages must be applied in the following sequence (see figure 4-2).
  1. VDD2.5 (core power) must be applied before or simultaneously with VDD3.3 (I/O buffer power).

     VDD 2.5 >1 V before VDD3.3 > 1 V
     VDD2.5 ≥ VDD3.3 until VDD2.5 = 2.5 V

  2. VDD5 (PCI buffer input clamping voltage connected to PCI VI/O pins) must be applied before or simultaneously with VDD3.3 (I/O buffer power).

     VDD 5 ≥ VDD 3.3 – 0.3 V

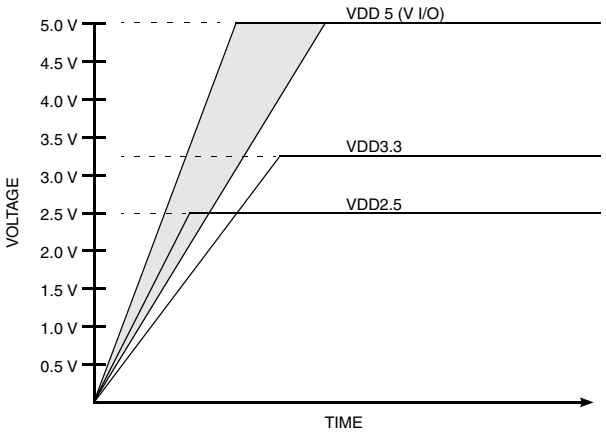


Figure 4-2. Power Sequencing—Voltage Versus Time

These guidelines must be adhered to as strictly as possible.

To minimize current and voltage stress on the ISP2312, QLogic recommends that all voltages be allowed to drop below 0.3 V before power is reapplied.

Section 5
Clock Requirements

5.1 Introduction

This section defines the requirements for the BCLK and REFCLK1 clock inputs for the ISP2312.

5.2 BCLK

The BCLK input signal is the ISP2312 peripheral component interconnect (PCI) clock. The ISP2312 BCLK signal conforms to the requirements in the *PCI-X Addendum* to the *PCI Local Bus Specification*.

The following clock specification information is from the *PCI-X Addendum* to the *PCI Local Bus Specification*.

The clock waveform must be delivered to each PCI component in the system. Compliance with the clock specification is measured at the ISP2312 BCLK pin. The clock waveform requirements for 5.0-V and 3.0-V signaling environments are illustrated in figure 5-1 and listed in table 5-1.

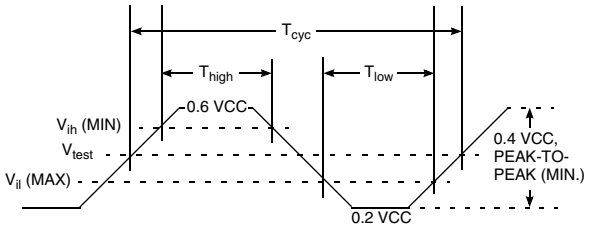


Figure 5-1. 3.3-V Clock Waveforms

Table 5-1. BCLK AC Specifications

Symbol	Parameter	PCI-X 133 MHz		PCI-X 66 MHz		Conventional PCI 66 MHz (ref)		Conventional PCI 33 MHz (ref)		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
T_{cyc}	CLK cycle time [a]	7.5	20	15	20	15	30	30	∞	ns
T_{high}	CLK high time	3		6		6		11		ns
T_{low}	CLK low time	3		6		6		11		ns
—	CLK slew rate[b]	1.5	4	1.5	4	1.5	4	1	4	V/ns

Table Notes

[a]The minimum clock period must not be violated for any single clock cycle (accounting for all system jitter).

[b]This slew rate must be met across the minimum peak-to-peak portion of the clock waveform, as illustrated in figure 5-1.

5.3 REFCLK1

The REFCLK1 input signal is the ISP2312 Fibre Channel clock, which must conform to the requirements listed in table 5-2.

Table 5-2. REFCLK1 Specifications

Parameter	Value	Notes
Frequency	106.25 MHz	Center frequency
Stability	±50 PPM	PPM is parts per million.
Symmetry	45/55 to 55/45	This is the duty cycle, measured at 50 percent of the signal level.
Rise and fall time	2 ns maximum	This value is the maximum rise/fall time measured between 0.8 V and 2.0 V.
Jitter	8 ps	Root mean square (RMS)
CIN	4 pF maximum	Input capacitance
VIH	2.0 V minimum	This is the minimum input high voltage.
VIL	0.8 V maximum	This is the maximum input low voltage.
IIN	±10 µA	Input current
Oscillator	106.25 MHz	QLogic recommends one of the following oscillators: SaRonix (part number STAA99B3-106.25 MHz) Pletronics (part number SQ30057D-106.26 MHz) EPSON (part number EG2001CA106.25M-PCH)

Section 6
PCI Interface

6.1 Introduction

The ISP2312 supports both a conventional PCI bus interface (compliant with the *PCI Local Bus Specification).* and a PCI-X bus interface (compliant with the *PCI-X Addendum* to the *PCI Local Bus Specification*). See these specifications for details of PCI bus operation and for motherboard design requirements.

The ISP2312 accommodates a 32- or 64-bit bus at the maximum clock frequency of 66 MHz for a conventional PCI bus (see sections 6.2.2 and 6.2.3) and 133 MHz for a PCI-X bus. The chip utilizes burst mode master DMA transfers at the maximum width and transfer rate of the bus and also acts as a PCI bus target for register accesses from host. As a PCI target, the ISP2312 allows 8, 16, and 32-bit accesses.

The ISP2312 supports two independent PCI functions. All registers—PCI bus configuration, PCI bus interface, and mailbox incoming and outgoing, are duplicated for each function. Function 0 is connected to Fibre Channel port 1; function 1 is connected to Fibre Channel port 2.

6.2 Signal Connections

The ISP2312 provides a complete pin-for-pin direct connection to a 32-bit or 64-bit PCI bus. The only external logic required is pull-ups (*keepers*) on certain signals. These pull-ups are specified as system resources in the *PCI Local Bus Specification*. The system in which the ISP2312 is designed must provide these system resources. The connection diagrams in this section show these signals and indicate that they must have pull-ups. See the *PCI Local Bus Specification* for details on these signals.

The PCI interface pins are listed in table 6-1.

Table 6-1. PCI Interface Pins

Pin Name	Description
$\overline{\text{ACK64}}$	PCI bus 64-bit acknowledge
AD0–63	PCI address and data
BCLK	PCI bus clock
$\overline{\text{BGNT}}$	PCI bus grant
$\overline{\text{BREQ}}$	PCI bus request
$\overline{\text{CBE0–7}}$	PCI command/byte enable
$\overline{\text{DEVSEL}}$	PCI bus device select
$\overline{\text{FRAME}}$	PCI bus frame
IDSEL	PCI bus initialization device select
$\overline{\text{INTA}}$	PCI bus interrupt (function 0/port 1)
$\overline{\text{INTB}}$	PCI bus interrupt (function 1/port 2)
$\overline{\text{IRDY}}$	PCI bus initiator ready
M66EN	PCI 66 MHz enable
PAR	PCI bus parity
PAR64	PCI bus parity for 64-bit extensions
$\overline{\text{PERR}}$	PCI parity error
$\overline{\text{REQ64}}$	PCI bus 64-bit transfer request
$\overline{\text{RESET}}$	PCI bus reset
$\overline{\text{SERR}}$	PCI system error
$\overline{\text{STOP}}$	PCI bus stop
$\overline{\text{TRDY}}$	PCI bus target ready

6.2.1 M66EN and PCIXCAP Connections

The host adapter board supports conventional PCI bus mode and PCI-X bus mode, as well as the maximum bus frequency, through a combination of the ISP2312 M66EN pin (solder ball AD11) and the PCI bus PCI-X capability (PCIXCAP) pin (pin 38B). The M66EN pin is bussed together on all PCI connectors that support 66 MHz and is pulled up by a central resource. The PCIXCAP pin is also bussed together on all PCI connectors. At power-up, the central resource (system and/or bridge) senses the state of M66EN and PCIXCAP to select the appropriate mode and frequency. The ISP2312 host

adapter board must connect these two signals appropriately to indicate the bus mode and frequency supported by the board (see table 6-2).

Table 6-2. M66EN and PCIXCAP Connections

M66EN	PCIXCAP	Conventional PCI Bus Frequency	PCI-X Bus Frequency
Ground	Ground	33 MHz	Not capable
Not connected	Ground	66 MHz	Not capable
Ground	Pull-down	33 MHz	PCI-X 66 MHz
Not connected	Pull-down	66 MHz	PCI-X 66 MHz
Ground	Not connected	33 MHz	PCI-X 133 MHz
Not connected	Not connected	66 MHz	PCI-X 133 MHz

PCI devices not capable of supporting PCI-X bus mode and conventional PCI 66-MHz operation must ground PCIXCAP and M66EN on the host adapter board so that the central clock generation circuitry can limit the maximum PCI bus clock frequency to 33 MHz. The ISP2312 uses M66EN as an input to determine the operating frequency of the PCI bus *only* in conventional PCI bus mode. When M66EN is deasserted (logic level 0), the PCI bus frequency is in the range of DC to 33 MHz (0 to ≤ 33). When M66EN is asserted (logic level 1), the PCI bus frequency is in the range of 33 MHz to 66 MHz (>33 and ≤ 66).

When the ISP2312 operates at a maximum PCI bus frequency of 66 MHz in both conventional PCI bus and PCI-X bus modes, the PCIXCAP signal must be pulled down on the host adapter board. M66EN must be pulled up by a central resource so that the central clock generation circuitry can limit the maximum PCI bus clock frequency to 66 MHz.

When the ISP2312 operates at a maximum PCI bus frequency of 66 MHz in conventional PCI bus mode and 133 MHz in PCI-X bus mode, PCIXCAP must be left unconnected and M66EN must be pulled up by a central resource. To accommodate both devices on the same board, the board design must optionally pull down both PCIXCAP and M66EN (see figure 6-1).

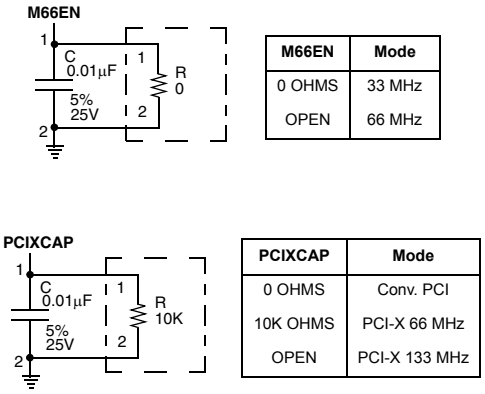


Figure 6-1. M66EN and PCIXCAP

6.2.2 32-Bit Connections

Make connections to a 32-bit bus as shown in figure 6-2. All PCI signals must be connected one-for-one to the PCI bus. Any PCI signals not shown in the figure are not implemented in the ISP2312 or do not need to be connected.

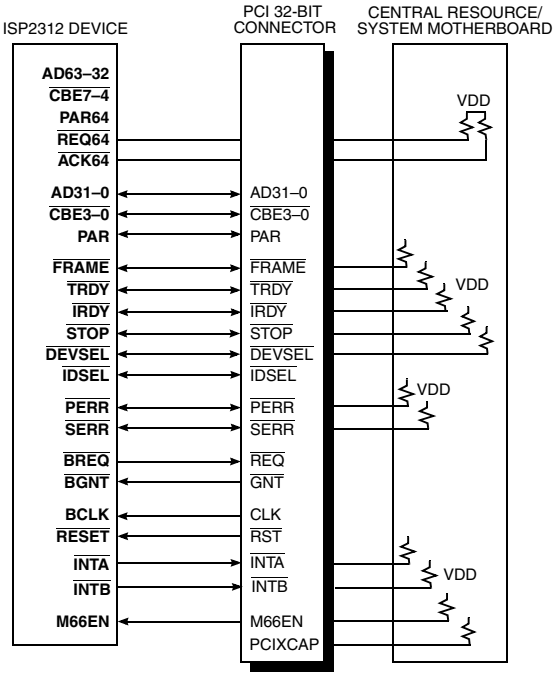


Figure 6-2. 32-Bit Connections

6.2.3
64-Bit Connections

Make connections to a 64-bit bus as shown in figure 6-3. All PCI signals must be connected one-for-one to the PCI bus. Any PCI signals not shown in the figure are not implemented in the ISP2312 or do not need to be connected.

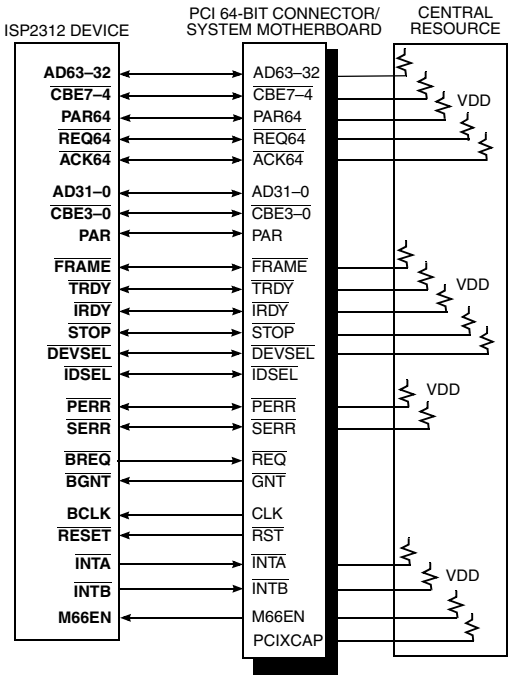


Figure 6-3. 64-Bit Connections

6.3
PCI Bus Target Mode Operation

As a PCI target, the ISP2312 allows the host to access the following:

- PCI bus configuration registers. These registers are mapped in a 256-byte configuration address space and accessed by the host as an 8-bit byte, a 16-bit halfword, or a 32-bit word.
- PCI bus interface registers. These registers are mapped in both I/O and memory space and accessed from the PCI bus an 8-bit byte, a 16-bit halfword, or a 32-bit word.
- BIOS PROM. The external BIOS PROM is mapped into memory space and accessed from the PCI bus as an 8-bit byte, a 16-bit halfword, or a 32-bit word.

As a PCI target, the ISP2312 does not support burst transfers or PCI 64-bit extensions for register access. However, the ISP2312 does support 64-bit addressing in PCI-X mode so that its registers can be mapped in memory space beyond a four gigabyte address.

6.3.1
PCI Bus Address Decode

As a target, the ISP2312 supports host accesses in the configuration, memory, and I/O address spaces (see figure 6-4). The configuration address space is 256 bytes and maps the PCI configuration registers. The ISP2312 internal registers can be mapped into memory and I/O address spaces.

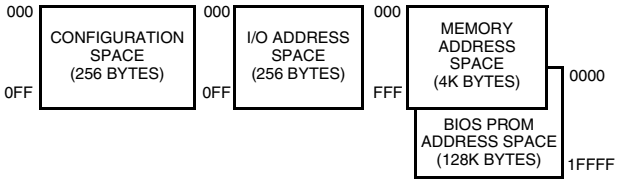


Figure 6-4. Target Mode Address Space

The registers require 256 bytes of I/O address space. The base address for the registers is provided by the 32-bit PCI I/O Base Address register. The upper 24 bits of this register are programmable, allowing ISP2312 registers to relocate to any 256-byte address boundary in four-gigabyte I/O space.

The minimum address space requirement in memory address space is 4K bytes. The base address for the memory address map is located in the 64-bit wide PCI Memory Base Address register. The PCI Upper Memory Base Address register (PCI-X mode only) and the upper 20 bits of the PCI Lower Memory Base Address register are programmable, allowing ISP2312 registers to relocate to any 4K-byte address boundary in memory space. Since the registers use only the 256-byte space (address space 000h–0FFh), the memory address spaces 100h–1FFh through F00h–FFFh are aliased to address spaces 000h–0FFh. The external BIOS PROM is also mapped in memory address space through the PCI Expansion ROM Base Address register and supports 128K bytes of address space when enabled. ISP2312 register mapping in the PCI bus address space is illustrated in figure 6-5.

Internally, the ISP2312 supports registers for the PCI bus configuration and PCI bus interface, as shown in figure 6-5. The PCI registers occupy the first 128 bytes from 00h–7Fh.

In address space 80h–FFh, only the following registers can be accessed:

- C0h (RISC HCCR register)
- CCh (GPIOD register)
- CEh (GPIOE register)

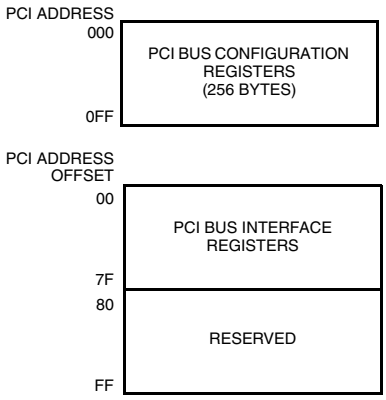


Figure 6-5. ISP2312 Register Map

6.3.2 Target Mode Commands

As a target, the ISP2312 supports the following commands:

- Configuration address space:
  - Configuration Read
  - Configuration Write
- I/O address space:
  - I/O Read
  - I/O Write
- Memory address space (see table 6-3)

Table 6-3. Memory Address Space Target Mode Commands

Conventional PCI	PCI-X	Notes
Memory Read	Memory Read Dword	—
Memory Write	Memory Write	—
Memory Read Line	Memory Read Block	Both commands are aliased to Memory Read by the ISP2312.
Memory Read Multiple	Split Completion	Memory Read Multiple is aliased to Memory Read.

Table 6-3. Memory Address Space Target Mode Commands (Continued)

Conventional PCI	PCI-X	Notes
Memory Write and Invalidate	Memory Write Block	Both commands are aliased to Memory Write by the ISP2312.
—	Alias to Memory Read Block	Aliased to Memory Read by the ISP2312.
—	Alias to Memory Write Block	Aliased to Memory Write by the ISP2312.

The ISP2312 does not respond to any unsupported commands.

6.4 Master Mode Commands

In conventional PCI bus mode, ISP2312 issues the following commands when acting as a PCI bus master:

- Dual Address Cycle (DAC)
- Memory Read
- Memory Read Line
- Memory Read Multiple
- Memory Write
- Memory Write and Invalidate

The type of memory read or write commands issued by the ISP2312 depends on the amount of data that the chip intends to transfer in a single burst and the value of the PCI Cache Line Size register. Refer to table 6-4 for a summary of the master mode commands and operations.

Table 6-4. Conventional PCI Bus Master Mode Commands

Value of PCI Cache Line Size Register	Data to be Transferred in a Burst	Command Issued
Host Memory Read Operations		
Zero or nonbinary	Any number of data words	Memory Read Multiple
Nonzero binary	Less than or equal to four bytes	Memory Read

Table 6-4. Conventional PCI Bus Master Mode Commands (Continued)

Value of PCI Cache Line Size Register	Data to be Transferred in a Burst	Command Issued
Host Memory Read Operations		
Nonzero binary	Greater than four bytes and less than or equal to the value in the PCI Cache Line Size register	Memory Read Line
Nonzero binary	Greater than the value in the PCI Cache Line Size register	Memory Read Multiple

In PCI-X bus mode, ISP2312 issues the following commands when acting as a master on the PCI bus.

- Dual Address Cycle (DAC)
- Memory Read Block
- Memory Write Block

The bus master mode commands are generated by the conditions described in sections 6.4.1 through 6.4.6.

6.4.1 Dual Address Cycle

The Dual Address Cycle (DAC) command is used by the ISP2312 as an additional command phase that precedes the memory commands to transfer a 64-bit address to PCI memory targets that support 64-bit address decode. This allows the ISP2312 to DMA into a memory address space that extends beyond four gigabytes. The DAC command is illustrated in figure 6-6. The 64-bit address is driven onto the PCI bus from a 64-bit DMA address register in two phases. The first phase is the low-order 32-bit address with the DAC command. This phase is driven from a 32-bit DMA address counter. The second phase is the high-order 32-bit address with the actual memory read or write command. This phase is driven from a 32-bit static address register.

The 64-bit addressing function is automatic. A value other than 0 in the upper 32 bits of the 64-bit transfer address register automatically causes the ISP2312 to drive the DAC command onto the PCI bus.

In PCI-X mode, the ISP2312 responds to 64-bit addressing and the DAC command when acting as a PCI target.

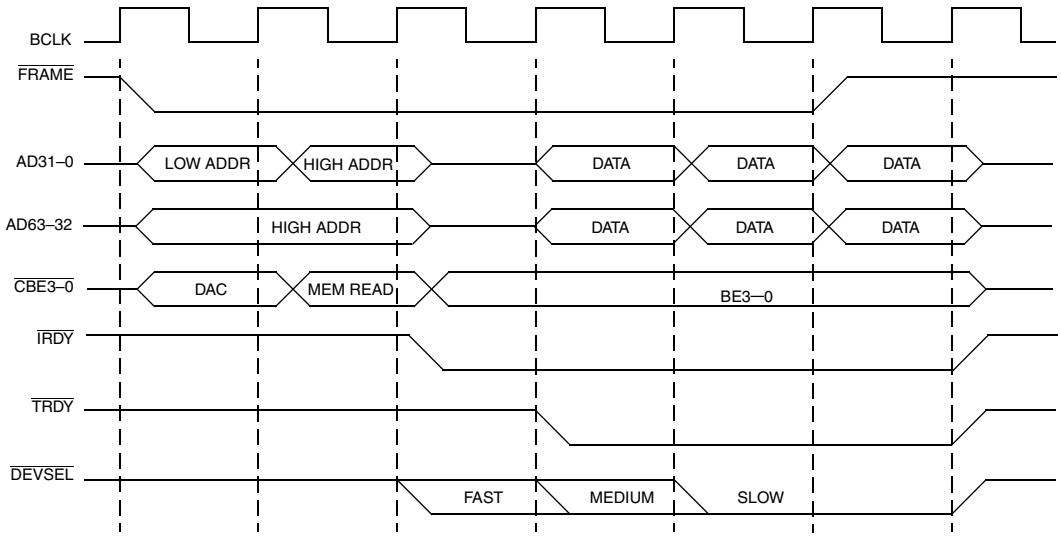


Figure 6-6. PCI 64-Bit Addressing with Dual Address Cycle Command

6.4.2 Memory Read

During host memory read operations, the ISP2312 issues a Memory Read command when a burst is less than or equal to four bytes of data.

6.4.3 Memory Read Line

During host memory read operations, the ISP2312 issues a Memory Read Line command when a burst is greater than four bytes and less than or equal to the value in the PCI Cache Line Size register.

6.4.4
Memory Read Multiple

During host memory read operations, the ISP2312 issues a Memory Read Multiple command when a burst is greater than the value in the PCI Cache Line Size register. Since the ISP2312 is a mass storage controller that transfers large amounts of data, it also uses this command as a default when the value in the PCI Cache Line Size register is 0 or initialized to a nonbinary value, for example, other than 1, 2, 4, 8, 16, 32, 64, and 128.

6.4.5
Memory Write

During host memory write operations, when the value in the PCI Cache Line Size register is zero or nonbinary, the ISP2312 issues a Memory Write command. When the value in the PCI Cache Line Size register is nonzero binary, the ISP2312 issues a Memory Write command when any of the following conditions is met:

- The burst data transfer size is not equal to or not an even multiple of the value in the PCI Cache Line Size register.
- The starting DMA address is **not** aligned to a cacheline boundary.
- The Memory Write and Invalidate command is disabled in the PCI configuration registers.

6.4.6
Memory Write and Invalidate

During host memory write operations, the ISP2312 generates a Memory Write and Invalidate command when all of the following conditions are met:

- The PCI Cache Line Size register is programmed to a nonzero binary value.
- The burst data transfer size is equal to or is a multiple of the value in the PCI Cache Line Size register.
- The starting DMA address is aligned to a cacheline boundary.
- The Memory Write and Invalidate command is enabled in the PCI Configuration register.

6.4.7
Memory Read Block

In PCI-X bus mode, the ISP2312 issues a Memory Read Block command for all memory read operations, regardless of the length of the transfer. When the Memory Read Block command transaction is terminated by the PCI target with a split response, the ISP2312 finishes the transaction as a target by accepting a Split Completion command from a completer.

6.4.8
Memory Write Block

In PCI-X bus mode, the ISP2312 issues a Memory Write Block command for all memory write operations, regardless of the length of the transfer.

6.5
Data Path and Alignment Logic

The data path and alignment logic provide an access path between the PCI bus and ISP2312 modules and perform byte alignment of the data transferred to and from the PCI bus. The byte alignment refers to the placement of PCI data on the appropriate byte lanes within the eight-byte field as defined by the address phase.

The data path logic allows access to the ISP2312 module registers, command FIFO, and external BIOS PROM. For the data transferred out of the ISP2312, the logic implements a data path multiplexor to multiplex data from various sources internal to the chip and to drive the multiplexed data onto the PCI AD bus. For the data received from the PCI AD bus, the ISP2312 de-multiplexes the data and drives it onto internal buses.

The ISP2312 in target mode allows host access to some of the internal registers only in 16-bit word mode. The data is accessed using PCI AD0–31, while the byte enable field on the PCI bus and $\overline{\text{CBE0–3}}$ indicate which byte lanes are valid. When the host performs a 16-bit word write with valid bytes on AD16–31, the data path and alignment logic shifts the information down and drives it onto an internal register access bus. Similarly for PCI reads, when the host requests information on the AD16–31 bus, the ISP2312 shifts the data up after register access and drives it onto the requested byte lanes.

For ISP2312 master mode DMA transfers, both byte alignment and byte merging are performed based on the starting DMA address and DMA transfer count. At the beginning of the DMA operation, the PCI bus interface unit (PBIU) performs partial transfers to align the address to a four-byte boundary for PCI 32-bit mode transfers and to an eight-byte boundary for PCI 64-bit mode transfers. At the end of the DMA operation, the PBIU transfers residual bytes by performing partial transfers. When the starting

address is not aligned to a word boundary, the alignment is performed as shown in tables 6-5 and 6-6.

Table 6-5. Starting Address Alignment for PCI 32-Bit Mode Transfers

Starting Address	Transfer Performed for First PCI Data Phase
1 MOD 4	Three-byte transfer
2 MOD 4	Two-byte transfer
3 MOD 4	One-byte transfer

Table 6-6. Starting Address Alignment for PCI 64-Bit Mode Transfers

Starting Address	Transfer Performed for First PCI Data Phase
1 MOD 8	Seven-byte transfer
2 MOD 8	Six-byte transfer
3 MOD 8	Five-byte transfer
4 MOD 8	Four-byte transfer
5 MOD 8	Three-byte transfer
6 MOD 8	Two-byte transfer
7 MOD 8	One-byte transfer

Table 6-7 indicates how sequential data bytes with values of 00 through 07 are transferred to and from host memory on the PCI bus for different starting DMA addresses. For PCI 32-bit mode transfers, when the DMA address is aligned to a 32-bit boundary, the ISP2312 transfers data on all four byte lanes. When the DMA address is not aligned to 32-bit boundary, the ISP2312 performs one-, two-, or three-byte transfers.

Table 6-7. Data Alignment on the PCI Bus for PCI 32-Bit Mode Transfers

Starting DMA Address[a]				PCI AD Bus Byte Lanes			
A3	A2	A1	A0	Byte 3	Byte 2	Byte 1	Byte 0
0	0	0	0	03	02	01	00
0	1	0	0	07	06	05	04
0	0	0	1	02	01	00	XX
0	1	0	0	06	05	04	03
0	0	1	0	01	00	XX	XX
0	1	0	0	05	04	03	02
0	0	1	1	00	XX	XX	XX
0	1	0	0	04	03	02	01

Table Notes
[a]Least significant bits

Table 6-8 indicates how sequential data bytes with values of 00 through 15 are transferred to and from host memory on the PCI bus for different starting DMA addresses for PCI 64-bit mode transfers. When the DMA address is aligned to a 64-bit boundary, the ISP2312 transfers data on all eight byte lanes. When the DMA address is not aligned to a 64-bit boundary, the ISP2312 performs partial transfer of one through seven bytes during the first data phase.

Table 6-8. Data Alignment on the PCI Bus for PCI 64-Bit Mode Transfers

Starting DMA Address[a]				PCI AD Bus Byte Lanes							
A3	A2	A1	A0	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
0	0	0	0	07	06	05	04	03	02	01	00
1	0	0	0	15	14	13	12	11	10	09	08
0	0	0	1	06	05	04	03	02	01	00	XX
1	0	0	0	14	13	12	11	10	09	08	07
0	0	1	0	05	04	03	02	01	00	XX	XX
1	0	0	0	13	12	11	10	09	08	07	06
0	0	1	1	04	03	02	01	00	XX	XX	XX
1	0	0	0	12	11	10	09	08	07	06	05

Table 6-8. Data Alignment on the PCI Bus for PCI 64-Bit Mode Transfers (Continued)

Starting DMA Address[a]				PCI AD Bus Byte Lanes							
A3	A2	A1	A0	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
0	1	0	0	03	02	01	00	03	02	01	00
1	0	0	0	11	10	09	08	07	06	05	04
0	1	0	1	02	01	00	XX	02	01	00	XX
1	0	0	0	10	09	08	07	06	05	04	03
0	1	1	0	01	00	XX	XX	01	00	XX	XX
1	0	0	0	09	08	07	06	05	04	03	02
0	1	1	1	00	XX	XX	XX	00	XX	XX	XX
1	0	0	0	08	07	06	05	04	03	02	01

Table Notes
[a]Least significant bits

6.6 PCI Bus Configuration Registers

The ISP2312 supports two independent PCI functions. The PCI bus configuration registers are duplicated for each function. Function 0 is connected to Fibre Channel port 1; function 1 is connected to Fibre Channel port 2. The function number field of the PCI AD10–8 pins selects function 0 and function 1 configuration registers.

The PCI bus configuration registers are mapped into the 256-byte configuration address space assigned to the ISP2312. These registers identify, configure, and initialize the ISP2312. The registers are listed in table 6-9 and described in the following sections. The configuration registers can be accessed by the host system as a byte, a 16-bit halfword, or a 32-bit word on the PCI bus. These registers can be reset only through a hard reset applied to the ISP2312 $\overline{\text{RESET}}$ pin. They cannot be reset by applying a soft reset to the ISP2312 through the ISP2312 Soft Reset bit (ISP Control/Status register bit 0).

The PCI bus configuration registers also include capability registers to support the following:

- PCI power management
- PCI message signaled interrupt
- *PCI-X Addendum* to the *PCI Local Bus Specification*

Note the following:

- Register bits are set to 1 and reset or cleared to 0 unless otherwise noted. A reset value of X indicates an indeterminate value.
- Reserved bits are reset to 0 unless otherwise noted. Register bits allow read and write access unless otherwise noted.

Table 6-9. PCI Bus Configuration Registers

PCI Configuration Address Space	Access[a]	Register Name	Reset Value (h)
00	R	PCI Vendor ID	1077
02	R	PCI Device ID	2312
04	R/W	PCI Command	0000
06	R/W	PCI Status	Note b
08	R	PCI Revision ID and Class Code	0C040001
0C	R/W	PCI Cache Line Size	00

Table 6-9. PCI Bus Configuration Registers (Continued)

PCI Configuration Address Space	Access[a]	Register Name	Reset Value (h)
0D	R/W	PCI Latency Timer	Note c
0E	R	PCI Header Type	80
10	R/W	PCI I/O Base Address	00000001
14	R/W	PCI Lower Memory Base Address	Note d
18	R/W	PCI Upper Memory Base Address	00000000
2C	R	PCI Subsystem Vendor ID	Note e
2E	R	PCI Subsystem Device ID	Note e
30	R/W	PCI Expansion ROM Base Address	00000000
34	R	PCI Capability Pointer Register	00000044
3C	R/W	PCI Interrupt Line	00
3D	R	PCI Interrupt Pin	Note f
3E	R	PCI Minimum Grant	40
3F	R	PCI Maximum Latency	00
44	R	PCI Capability ID	01
45	R	PCI-X Capability Item Pointer	4C
46	R	PCI Power Management Capabilities	02
48	R/W	PCI Power Management Control/Status	00
4A	R	PCI Power Management Bridge Support Extensions	00
4B	R	PCI Power Management Data	00
4C	R	PCI-X Capability ID	07
4D	R	PCI MSI Capability Item Pointer	54
4E	R/W	PCI-X Command	0022
50	R	PCI-X Status	0963FFF8
54	R	PCI MSI Capability ID	05
56	R/W	PCI MSI Message Control	0086
58	R/W	PCI MSI Message Address	00000000
5C	R/W	PCI MSI Message Upper Address	00000000
60	R/W	PCI MSI Message Data	0000
64	R/W	CompactPCI Hot Swap Capability	06

Table 6-9. PCI Bus Configuration Registers (Continued)

PCI Configuration Address Space	Access[a]	Register Name	Reset Value (h)
65	R	PCI Next Capability Item Pointer	64
66	R/W	CompactPCI Hot Swap Control and Status	80

Table Notes
[a]R = read, R/W = read/write
[b]The reset value when the ISP2312 is operating in conventional PCI bus mode is 02B0h; the reset value when the ISP2312 is operating in PCI-X bus mode is 0230h.
[c]The reset value when the ISP2312 is operating in conventional PCI bus mode is 00h; the reset value when the ISP2312 is operating in PCI-X bus mode is 40h.
[d]The reset value when the ISP2312 is operating in conventional PCI bus mode is 00000000h; the reset value when the ISP2312 is operating in PCI-X bus mode is 00000004h.
[e]The value in this register is loaded from an external serial EEPROM device at power up when the IDENB pin of the chip is tied to logic 0. Otherwise, this register is initialized to 0.
[f]This register is reset to 01h for function 0 configuration space or to 02h for function 1 configuration space.

6.6.1
PCI Vendor ID Register

This read-only register is accessed by the system software to identify the vendor ID. At power-up reset, this register is initialized to 1077h—the QLogic vendor ID assigned by the PCI special interest group (SIG).

The PCI Vendor ID register bits are shown in table 6-10.

Table 6-10. PCI Vendor ID Register

Configuration Address Space 00 (R)		
Bit	**Name**	**Reset (h)**
15–0	PCI Vendor ID	1077

6.6.2
PCI Device ID Register

This read-only register is accessed by the system software to identify the device on the PCI bus. At power-up reset, this register is initialized to 2312h.

The PCI Device ID register bits are shown in table 6-11.

Table 6-11. PCI Device ID Register

Configuration Address Space 02 (R)		
Bit	**Name**	**Reset (h)**
15–0	PCI Device ID	2312

6.6.3
PCI Command Register

This register controls operation of the ISP2312 on the PCI bus. The ISP2312 logically disconnects from the PCI bus when the value in this register is 0. The register bits are shown in table 6-12 and described in the following paragraphs.

Table 6-12. PCI Command Register

Configuration Address Space 04 (R/W)		
Bit	**Name**	**Reset (h)**
15–10	Reserved	00
9	Fast Back-to-Back Enable (R)	0
8	System Error Enable	0
7	Address/Data Stepping Enable (R)	0
6	Parity Error Response Enable	0
5	VGA Palette Snoop Enable (R)	0
4	Memory Write and Invalidate Enable	0
3	Special Cycles Enable (R)	0
2	Bus Master Enable	0
1	Memory Address Space Enable	0
0	I/O Address Space Enable	0

Table Notes
The (R) indicates a read-only bit.

- **Bits 15–10 (Reserved)**
- **Bit 9 (Fast Back-to-Back Enable).** This read-only bit is hardwired to 0. When the ISP2312 functions as a master, fast back-to-back transactions to different agents are not generated.
- **Bit 8 (System Error Enable).** When this bit is set, the ISP2312 asserts SERR when an address parity error is detected. When this bit is reset, SERR is not asserted.
- **Bit 7 (Address/Data Stepping Enable).** This read-only bit is not used and is hardwired to 0.
- **Bit 6 (Parity Error Response Enable).** When this bit is set, the ISP2312 enables parity checking on all incoming address and data phases. The PCI bus signals AD63–0 and CBE7–0 are checked for even parity. When this bit is reset, parity checking is disabled.
- **Bit 5 (VGA Palette Snoop Enable).** This read-only bit is not used and is hardwired to 0.
- **Bit 4 (Memory Write and Invalidate Enable).** When this bit is set, the ISP2312 is configured as a master to generate a Memory Write and Invalidate command on the PCI bus. When this bit is reset, the ISP2312 generates a Memory Write command.
- **Bit 3 (Special Cycles Enable).** This read-only bit is not used and is hardwired to 0.
- **Bit 2 (Bus Master Enable).** When this bit is set, the ISP2312 acts as a PCI bus master. When this bit is reset, the ISP2312 cannot generate PCI bus cycles.
- **Bit 1 (Memory Address Space Enable).** When this bit is set, the ISP2312 responds to Memory Read and Write commands in memory address space. When this bit is reset, the ISP2312 does not respond.
- **Bit 0 (I/O Address Space Enable).** When this bit is set, the ISP2312 responds to I/O Read and Write commands in I/O address space. When this bit is reset, the ISP2312 does not respond to I/O Read and Write commands in I/O address space.

6.6.4
PCI Status Register

This register monitors the ISP2312 status information for PCI related bus events. The register bits are shown in table 6-13 and described in the following paragraphs.

Table 6-13. PCI Status Register

Configuration Address Space 06 (R/W)		
Bit	**Name**	**Reset (h)**
15	Detected Parity Error	0
14	Signaled System Error	0
13	Received Master Abort	0
12	Received Target Abort	0
11	Signaled Target Abort	0
10–9	Device Select Timing (R)	1
8	Data Parity Detected	0
7	Fast Back-to-Back Capable (R)	Note a
6	UDF	0
5	66 MHz Capable	1
4	Capabilities List	1
3–0	Reserved	0

Table Notes
The (R) indicates a read-only bit.
[a]This bit is set when the ISP2312 operates in conventional PCI bus mode. This bit is reset when the ISP2312 operates in PCI-X bus mode.

- **Bit 15 (Detected Parity Error).** This bit is set when a parity error is detected regardless of the state of the Parity Error Response Enable bit (PCI Command register bit 6).
- **Bit 14 (Signaled System Error).** This bit is set by the ISP2312 (functioning as a target) when it asserts SERR on the PCI bus in response to one of the following error conditions.
  - ❒ The ISP2312 detects a parity error across the command and address field during the address phase of a PCI bus transaction.
  - ❒ The ISP2312 detects a parity error during the attribute phase of a PCI-X bus transaction.
  - ❒ The ISP2312, during a master mode message signaled interrupts (MSI) transaction, receives a master abort, target abort, or PERR (data parity error detected) from the PCI target.

- The ISP2312, during PCI-X master mode and split completion transactions, detects a data parity error (parity error on read data read and PERR on write data) and the Data Parity Error Recovery Enable bit (PCI-X Command register bit 0) is 0.

Under the first two conditions, the ISP2312 also terminates the transaction with a target abort condition.

- **Bit 13 (Received Master Abort).** This bit is set by the ISP2312 (functioning as a master) when its transaction is terminated with a master abort error.
- **Bit 12 (Received Target Abort).** This bit is set by the ISP2312 (functioning as a master) when the target terminates its transaction with a target abort error.
- **Bit 11 (Signaled Target Abort).** This bit is set by the ISP2312 (functioning as a target) when the ISP2312 terminates the transaction with a target abort error.
- **Bits 10–9 (Device Select Timing).** These read-only bits are hardwired to 1, indicating that the ISP2312 (functioning as a target) provides medium-speed DEVSEL on the PCI bus.
- **Bit 8 (Data Parity Detected).** This bit is set by the ISP2312 (functioning as a master) when it detects or asserts PERR on the PCI bus, and the Parity Error Response Enable bit (PCI Command register bit 6) is set.
- **Bit 7 (Fast Back-to-Back Capable).** This read-only bit is set by the ISP2312 when operating in conventional PCI bus mode (functioning as a target) to accept fast back-to-back transactions from a master when the transactions are aimed at two different agents. This bit is reset when the ISP2312 operates in PCI-X bus mode.
- **Bit 6 (User Definable Features (UDF)).** This feature is not supported.
- **Bit 5 (66 MHz Capable).** This bit is hardwired to 1 to indicate ISP2312 support for 66-MHz conventional PCI.
- **Bit 4 (Capabilities List).** This bit is hardwired to 1 to indicate ISP2312 support for new capabilities. The pointer for a new capabilities list is located at PCI configuration address space 34h.
- **Bits 3–0 (Reserved)**

6.6.5 PCI Revision ID and Class Code Register

The PCI Revision ID and Class Code register bits are shown in table 6-14 and described in the following paragraphs.

Table 6-14. PCI Revision ID and Class Code Register

Configuration Address Space 08 (R)		
Bit	**Name**	**Reset (h)**
31–24	PCI Class Code	0C
23–16	PCI Subclass Code	04
15–8	Programming Model	00
7–0	PCI Revision ID	01

- **Bits 31–24 (PCI Class Code).** This field is hardwired to 0Ch, indicating that the ISP2312 is a serial bus controller.
- **Bits 23–16 (PCI Subclass Code).** This field is hardwired to 04h, indicating that the ISP2312 is a Fibre Channel controller.
- **Bits 15–8 (Programming Model).** This field is hardwired to 00h, indicating that there are no special programming requirements.
- **Bits 7–0 (PCI Revision ID).** This field is hardwired to 01h, indicating the first revision of the ISP2312.

6.6.6 PCI Cache Line Size Register

This register specifies the PCI host system's cache line size in units of 32-bit words. The ISP2312 uses this information to generate the Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate commands. Since the ISP2312 transfers large amounts of data to and from host memory when the value in the PCI Cache Line Size register is 0 or nonbinary (other than 1, 2, 4, 8, 16, etc.), the ISP2312 generates a Memory Read Multiple command. When the value in this register is a nonzero binary, the ISP2312 generates the Memory Read Line and Memory Read Multiple commands based on the burst

transfer size. Refer to table 6-4 for a summary of the master mode commands. The register bits are shown in table 6-15.

Table 6-15. PCI Cache Line Size Register

Configuration Address Space 0C (R/W)		
Bit	**Name**	**Reset (h)**
7–0	PCI Cache Line Size	00

6.6.7
PCI Latency Timer Register

This register specifies the minimum number of PCI clocks that the ISP2312 has on the PCI bus when bursting data. The ISP2312 relinquishes control of the PCI bus only when preempted after the ISP2312 latency timer expires. This guarantees the ISP2312 minimum time on the bus when bursting data. Only the upper five bits of this register are programmable. The lower three bits are hardwired to 0 to provide a timer granularity of eight PCI clocks. The register bits are shown in table 6-16.

Table 6-16. PCI Latency Timer Register

Configuration Address Space 0D (R/W)		
Bit	**Name**	**Reset (h)**
7–3	PCI Latency Timer	Note a
2–0	Reserved	0

Table Notes

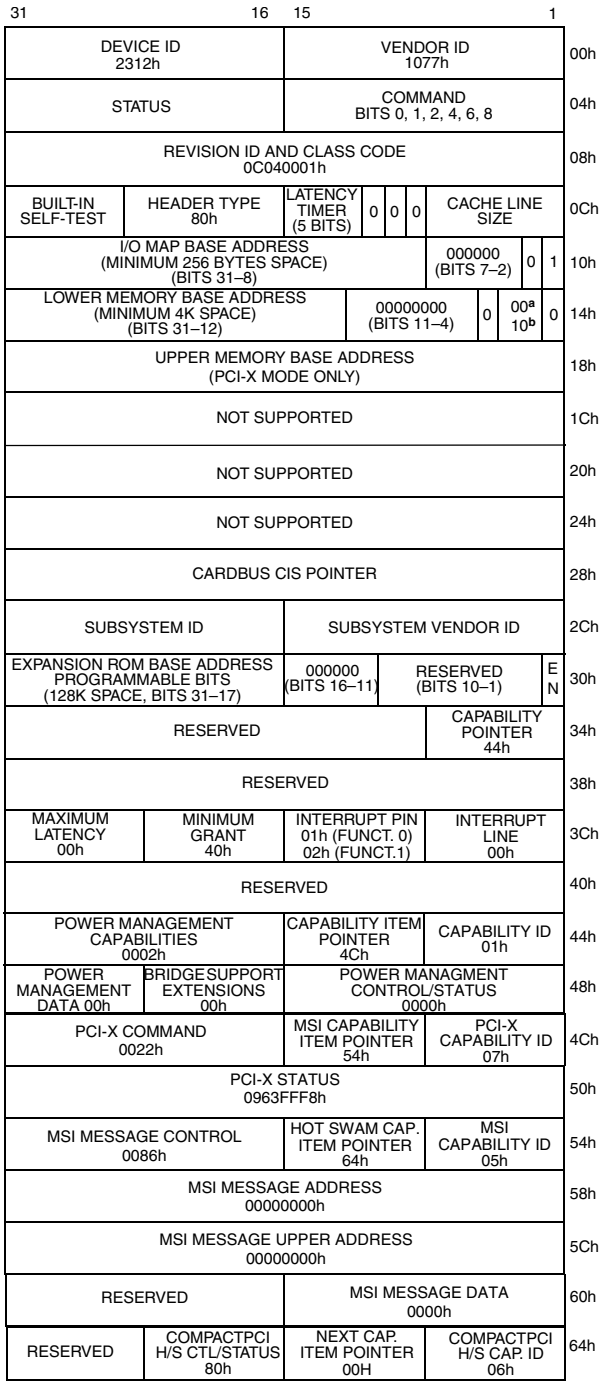
[a]The conventional PCI reset value is 00h; the PCI-X reset value is 40h.

6.6.8
PCI Header Type Register

This register contains the hardwired value of 80h to indicate to the host system that the ISP2312 is a multifunction device. The configuration space header for the ISP2312 is illustrated in figure 6-7. The register bits are shown in table 6-17.

Table 6-17. PCI Header Type Register

Configuration Address Space 0E (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Header Type	80



NOTE a: PCI 2.2
NOTE b: PCI-X

Figure 6-7. Configuration Space Header for ISP2312

6.6.9
PCI I/O Base Address Register

This register establishes the base address for the ISP2312 registers in I/O address space. The ISP2312 internal registers are relocated to an offset address relative to this base address register. Since the ISP2312 occupies an I/O address space of 256 bytes, only the upper 24 bits (bits 31–8) are programmable. The remaining lower eight bits (bits 7–0) are read only and hardwired to 01h. The register bits are shown in table 6-18.

Table 6-18. PCI I/O Base Address Register

Configuration Address Space 10 (R/W)		
Bit	**Name**	**Reset (h)**
31–8	PCI I/O Base Address	000000
7–0	Reserved	01

6.6.10
PCI Memory Base Address Registers

These registers establish the base address for the ISP2312 registers in memory address space. When operating in PCI 2.2 mode, the ISP2312 implements a 32-bit memory base address register. When operating in PCI-X mode, the ISP2312 implements a 64-bit memory base address register. The ISP2312 internal registers are relocated at an offset address relative to the base address register. Since the ISP2312 occupies a memory address space of 4K bytes, only the high-order bits (bits 63–12 in PCI-X mode; bits 32–12 in PCI 2.2 mode) are programmable. The remaining low-order bits (bits 11–0) are read only and are hardwired to 000h in PCI 2.2 mode and 004h in PCI-X mode. The ISP2312 registers occupy only 256 bytes of address space. The remaining address space (100h–1FFh through F00–FFFh) is aliased to address space 000h–0FFh. The register bits are shown in tables 6-19 and 6-20.

Table 6-19. PCI Lower Memory Base Address Register

Configuration Address Space 14 (R/W)		
Bit	**Name**	**Reset (h)**
31–12	PCI Lower Memory Base Address	00000
11–0	Reserved	Note a

Table Notes
[a]The conventional PCI reset value is 000h; the PCI-X reset value is 004h.

Table 6-20. PCI Upper Memory Base Address Register (PCI-X Mode Only)

Configuration Address Space 18 (R/W)		
Bit	**Name**	**Reset (h)**
31–0	PCI Upper Memory Base Address	00000000

6.6.11
PCI Subsystem Vendor ID Register

This read-only register is accessed by the system software to identify the subsystem vendor of a device on the PCI bus. Each subsystem vendor of the device loads a vendor specific ID value in this register. At power-up reset, the register is initialized to 0. After the reset is released, the PBIU automatically loads this register with a value at addresses 7Dh (function 0) and FDh (function 1) in an external serial EEPROM device when the IDENB pin of ISP2312 is tied to logic level 0 (most significant bit of the ID value is shifted in first). During this load process, any access to the ISP2312 registers from host is terminated with a retry response from ISP2312. Once the ISP2312 finishes register initialization, it allows the host to access its registers. The register bits are shown in table 6-21.

Table 6-21. PCI Subsystem Vendor ID Register

Configuration Address Space 2C (R)		
Bit	**Name**	**Reset (h)[a]**
15–0	PCI Subsystem Vendor ID	0000

Table Notes
[a]The reset value may also be accessed from the serial EEPROM.

6.6.12
PCI Subsystem Device ID Register

This read-only register is accessed by the system software to identify the subsystem device number on the PCI bus. The subsystem vendor of the device loads the device number in this register. At power-up reset, the register is initialized to 0. After the reset is released, the PBIU automatically loads this register with a value at addresses 7Eh (function 0) and FEh (function 1) in an external serial EEPROM device when the IDENB pin of ISP2312 is tied to logic level 1 (most significant bit of the ID value is shifted in first). During this load process, any access to the ISP2312 registers from the host is terminated with a retry response from the ISP2312. Once the ISP2312

finishes register initialization, it allows the host to access its registers. The register bits are shown in table 6-22.

Table 6-22. PCI Subsystem Device ID Register

Configuration Address Space 2E (R)		
Bit	**Name**	**Reset (h)[a]**
15–0	PCI Subsystem Device ID	0000

Table Notes
[a]The reset value may also be accessed from the serial EEPROM.

6.6.13
PCI Expansion ROM Base Address Register

This register establishes the base address for the expansion ROM (BIOS PROM). The ISP2312 external BIOS PROM is relocated at an offset address relative to this base address register. The register bits are shown in table 6-23 and described in the following paragraphs.

Table 6-23. PCI Expansion ROM Base Address Register

Configuration Address Space 30 (R/W)		
Bit	**Name**	**Reset (h)**
31–17	PCI Expansion ROM Base Address	0000
16–1	Reserved	0000
0	BIOS Enable	0

- **Bits 31–17 (PCI Expansion ROM Base Address).** Since the ISP2312 supports a minimum BIOS PROM address space of 128K bytes, only these high-order bits are programmable.
- **Bits 16–1 (Reserved).** These low-order bits are read only and hardwired to 0000h.
- **Bit 0 (BIOS Enable).** When this bit is set, the BIOS PROM is accessible. The RISC is also held in reset, since the RISC memory address bus accesses the BIOS PROM.

6.6.14
PCI Capability Pointer Register

This read-only register points to the PCI configuration address space where the remaining power management registers reside. The remaining registers are at address 44h; consequently, the ISP2312 PCI Capability Pointer register is hardwired to 44h (see table 6-24).

Table 6-24. PCI Capability Pointer Register

Configuration Address Space 34 (R)		
Bit	**Name**	**Reset (h)**
31–8	Reserved	000000
7–0	Capability Pointer	44

6.6.15
PCI Interrupt Line Register

This register contains interrupt routing information. It specifies the connection between the ISP2312 interrupt pin and a specific input from the system interrupt controller. The register is initialized by system software during power up. The register bits are shown in table 6-25.

Table 6-25. PCI Interrupt Line Register

Configuration Address Space 3C (R/W)		
Bit	**Name**	**Reset (h)**
7–0	PCI Interrupt Line	00

6.6.16
PCI Interrupt Pin Register

This register contains a hardwired value of 01h for the function 0 configuration space, indicating that INTA generates an interrupt to the host on the PCI bus. This register contains a hardwired value of 02h for the function 1 configuration space, indicating that INTB generates an interrupt to the host on the PCI bus. The register bits are shown in table 6-26.

Table 6-26. PCI Interrupt Pin Register

Configuration Address Space 3D (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Interrupt Pin	Note a

Table Notes
[a]This register is reset to 01h for function 0 configuration space or to 02h for function 1 configuration space.

6.6.17
PCI Minimum Grant Register

The ISP2312 PCI Minimum Grant register contains a hardwired value of 40h, indicating that the ISP2312 needs a minimum burst period of 16 µsec (64 × 0.25 µsec). The register bits are shown in table 6-27.

Table 6-27. PCI Minimum Grant Register

Configuration Address Space 3E (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Minimum Grant	40

6.6.18
PCI Maximum Latency Register

This register contains a hardwired value of 00h, indicating that the ISP2312 has no major requirements for the latency timer setting. The register bits are shown in table 6-28.

Table 6-28. PCI Maximum Latency Register

Configuration Address Space 3F (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Maximum Latency	00

6.6.19
PCI Power Management Capability Data Structure

The PCI power management capability data structure consists of following registers:

- PCI Capability ID
- PCI-X Capability Item Pointer
- PCI Power Management Capabilities
- PCI Power Management Control/Status
- PCI Power Management Bridge Support Extensions
- PCI Power Management Data

6.6.19.1
PCI Capability ID Register

This read-only register is hardwired to 01h to indicate the PCI power management data structure type (see table 6-29).

Table 6-29. PCI Capability ID Register

Configuration Address Space 44 (R)		
Bit	**Name**	**Reset (h)**
7–0	Capability Identifier	01

6.6.19.2
PCI-X Capability Item Pointer

This read-only register is hardwired to 4Ch, which is the address for the PCI-X next capability data structure (see table 6-30).

Table 6-30. PCI-X Capability Item Pointer Register

Configuration Address Space 45 (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI-X Capability Item Pointer	4C

6.6.19.3
PCI Power Management Capabilities Register

This register provides information about the ISP2312 power management capabilities. Since the ISP2312 does not support power state D1 or D2, the power management event function, or reporting power values through the data register, the related fields in this register (bits 15–3) are hardwired to 0. Bits 2–0 are hardwired to 2h, indicating that the ISP2312 supports version 1.1 of the *PCI Bus Power Management Interface Specification* (see table 6-31).

Table 6-31. PCI Power Management Capabilities Register

Configuration Address Space 46 (R)		
Bit	**Name**	**Reset (h)**
15–11	Power Management Event Support	00
10	D2 Support	0
9	D1 Support	0
8	Dynamic Data Support	0
7–6	Reserved	0
5	Device Specific Initialization	0

Table 6-31. PCI Power Management Capabilities Register (Continued)

Configuration Address Space 46 (R)		
Bit	**Name**	**Reset (h)**
4	Auxiliary Power Source	0
3	Power Management Event Clock	0
2–0	PCI Power Management Specification Version	2

6.6.19.4
PCI Power Management Control/Status Register

The PCI Power Management Control/Status register bits are listed in table 6-32.

Table 6-32. PCI Power Management Control/Status Register

Configuration Address Space 48 (R/W)		
Bit	**Name**	**Reset (h)**
15	Power Management Event Status (R)	0
14–13	Data Scale (R)	0
12–9	Data Select	0
8	Power Management Event Enable (R)	0
7–5	Reserved	0
4	Dynamic Data Power Management Enable (R)	0
3–2	Reserved	0
1–0	Power State	0

Table Notes
The (R) indicates a read-only bit.

Since the ISP2312 does not support the power management event function or reporting power data to the host, bits 15–2 of this register are hardwired to 0. Bits 1–0 (Power State) of this register allow the host or system software to control and monitor the power state of the ISP2312. When bits 1–0 are set to 1, the ISP2312 is in D3 hot state (minimum power). When bits 1–0 are reset to 0, the ISP2312 is in D0 state (maximum power). When the host tries to place the chip in an unsupported D1 or D2 state by writing 1h or 2h to bits 1–0 when the ISP2312 is in the D3 hot or the D0 state, no power state change is made.

6.6.19.5
PCI Power Management Bridge Support Extensions Register

This ISP2312 power management register is a place holder for PCI bridge functions, which are not supported in this chip. This register is hardwired to 00h (see table 6-33).

Table 6-33. PCI Power Management Bridge Support Extensions Register

Configuration Address Space 4A (R)		
Bit	**Name**	**Reset (h)**
7–0	Reserved	00

6.6.19.6
PCI Power Management Data Register

This ISP2312 power management register is a place holder for reading power values, which are not supported in this chip. This register is hardwired to 00h (see table 6-34).

Table 6-34. PCI Power Management Data Register

Configuration Address Space 4B (R)		
Bit	**Name**	**Reset (h)**
7–0	Reserved	00

6.6.20
PCI-X Capability Data Structure

The PCI-X capability data structure consists of following registers:

- PCI-X Capability ID
- PCI MSI Capability Item Pointer
- PCI-X Command
- PCI-X Status

6.6.20.1
PCI-X Capability ID Register

This register is hardwired to 07h to indicate support for the PCI-X capability data structure (see table 6-35).

Table 6-35. PCI-X Capability ID Register

Configuration Address Space 4C (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI-X Capability ID	07

6.6.20.2
PCI MSI Capability Item Pointer Register

This register is hardwired to 54h, which is the address for the next capability data structure (see table 6-36).

Table 6-36. PCI MSI Capability Item Pointer Register

Configuration Address Space 4D (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI MSI Capability Item Pointer	54

6.6.20.3
PCI-X Command Register

The PCI-X Command register bits are shown in table 6-37 and described in the following paragraphs. This register can be written to only when the chip is operating in PCI-X bus mode.

Table 6-37. PCI-X Command Register

Configuration Address Space 4E (R/W)		
Bit	**Name**	**Reset (h)**
15–7	Reserved	000
6–4	Maximum Outstanding Split Transactions	2
3–2	Maximum Memory Read Byte Count	0
1	Enable Relaxed Ordering	1
0	Data Parity Error Recoverable Enable	0

- **Bits 15–7 (Reserved)**
- **Bits 6–4 (Maximum Outstanding Split Transactions).** These bits set the maximum number of split transactions that the ISP2312 can have outstanding at one time (see table 6-38).

Table 6-38. Outstanding Split Transactions

Bits 6–4 (h)	Maximum Number of Outstanding Split Transactions
0	1
1	2
2	3
3	4
4	8

Table 6-38. Outstanding Split Transactions (Continued)

Bits 6–4 (h)	Maximum Number of Outstanding Split Transactions
5	12
6	16
7	32

- **Bits 3–2 (Maximum Memory Read Byte Count).** These bits set the maximum byte count that the ISP2312 can specify in the attribute phase of initiated burst memory read commands (see table 6-39).

Table 6-39. Maximum Memory Read Byte Count

Bits 3–2 (h)	Maximum Byte Count
0	512
1	1024
2	2048
3	4096

- **Bit 1 (Enable Relax Ordering).** When this bit is set, the ISP2312 can set relax ordering in the requester attributes of transactions it initiates that do not require strong-write ordering. At power up, this feature is enabled.
- **Bit 0 (Data Parity Error Recoverable Enable).** This bit is set by host driver to enable the ISP2312 to attempt recovery from data parity errors. When this bit is 0, the ISP2312 is acting as a PCI-X bus master, and a data parity error is detected (the Data Parity Detected bit (PCI Status register bit 8) is set), SERR is asserted when the System Error Enable bit (PCI Command register bit 8) is set.

6.6.20.4
PCI-X Status Register

The PCI-X Status register bits are shown in table 6-40 and described in the following paragraphs. This register can be written to only when the chip is operating in PCI-X bus mode.

Table 6-40. PCI-X Status Register

Configuration Address Space 50 (R/W)		
Bit	**Name**	**Reset (h)**
31–29	Reserved	0
28–26	Designed Maximum Cumulative Read Size (R)	2
25–23	Designed Maximum Outstanding Split Transactions (R)	2
22–21	Designed Maximum Memory Read Byte Count (R)	3
20	Device Complexity (R)	0
19	Unexpected Split Completion	0
18	Split Completion Discarded	0
17	133 MHz Capable (R)	1
16	64-bit Device (R)	1
15–8	Bus Number (R)	FF
7–3	Device Number (R)	1F
2–0	Function Number (R)	0

Table Notes
The (R) indicates a read-only bit.

- **Bits 31–29 (Reserved)**
- **Bits 28–26 (Designed Maximum Cumulative Read Size).** This read-only field indicates the maximum cumulative size of all burst memory read transactions that the ISP2312 can have outstanding at one time. Since the ISP2312 can request 2112 bytes for the transmit DMA channel, 128 bytes for the command DMA channel, and 128 bytes for the auto-request DMA channel, the maximum value for these bits is 2h (4K bytes maximum outstanding).
- **Bits 25–23 (Designed Maximum Outstanding Split Transactions).** Since the ISP2312 can generate memory burst read requests from three different DMA channels: transmit, auto-request, and command, this field is set to 2h, indicating to host that the ISP2312 can have a maximum of three outstanding split requests.
- **Bits 22–21 (Designed Maximum Memory Read Byte Count).** Since the ISP2312 can generate memory burst read requests with a maximum byte count of 2112, this read-only field is set to 3h (equal to 4096 bytes, which is greater than 2112 bytes).
- **Bit 20 (Device Complexity).** This bit is reset to 0 to indicate that the ISP2312 is a simple device rather than a bridge device.
- **Bit 19 (Unexpected Split Completion).** This bit is set by ISP2312 when it receives an unexpected split completion with its requester ID. When the host writes 1 to this bit, it is cleared.
- **Bit 18 (Split Completion Discarded).** This bit is set by the ISP2312 to indicate that the split completion is discarded because the requester would not accept it. Since the ISP2312 does not initiate split completion requests, this bit is not set. When the host writes 1 to this bit, it is cleared.
- **Bit 17 (133 MHz Capable).** This bit is set to 1 to indicate that the ISP2312 can operate at 133 MHz in PCI-X bus mode.
- **Bit 16 (64-bit Device).** This read-only bit is hardwired to 1 to indicate that the ISP2312 is a 64-bit PCI-X device.
- **Bits 15–8 (Bus Number).** This read-only, eight-bit field indicates the number of the bus segment where the ISP2312 is connected on the PCI bus. The ISP2312 updates this register from the bus number field (AD7–0) of the attribute phase of a type 0 configuration write cycle every time the chip is accessed. The host system reads these bits only for diagnostic purposes. The ISP2312 uses this information as part of the requester ID during PCI DMA transactions.
- **Bits 7–3 (Device Number).** This read-only, five-bit field indicates the device number for the ISP2312. The device number is assigned by the system hardware. The ISP2312 updates this register from the device number field (AD15–11) of the address of a type 0 configuration write cycle every time the chip is

accessed. The host system reads these bits only for diagnostic purposes. The ISP2312 uses this information as part of the requester ID during PCI DMA transactions.

- **Bits 2–0 (Function Number).** This read-only, three-bit field indicates the function number of the ISP2312. This field is hardwired to 0 for function 0 and 1 for function 1. The host system reads these bits only for diagnostic purposes. The ISP2312 uses this information as part of the requester ID during PCI DMA transactions.

6.6.21
PCI MSI Capability Data Structure

The PCI Message Signaled Interrupt (MSI) feature allows the ISP2312 to request interrupt service by writing a system specified message to a system specified address (PCI dword memory write transaction). MSI eliminates using the PCI INTA and INTB signals to request interrupt service. When MSI is enabled, INTA and INTB cannot request interrupt service.

The PCI MSI capability data structure consists of following registers:

- PCI MSI Capability ID
- PCI MSI Message Control
- PCI MSI Message Address
- PCI MSI Message Upper Address
- PCI MSI Message Data
- PCI Next Capability Item Pointer

These registers are initialized by system software at power up.

6.6.21.1
PCI MSI Capability ID Register

The PCI MSI Capability ID register is hardwired to 05h to indicate PCI MSI capability (see table 6-41).

Table 6-41. PCI MSI Capability ID Register

Configuration Address Space 54 (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI MSI Capability ID	05

6.6.21.2
PCI MSI Message Control Register

The PCI MSI Message Control register bits are shown in table 6-42 and described in the following paragraphs.

Table 6-42. PCI MSI Message Control Register

Configuration Address Space 56 (R/W)		
Bit	**Name**	**Reset (h)**
15–8	Reserved	00
7	64-bit Address Capable (R)	1
6–4	Multiple Message Enable	0
3–1	Multiple Message Capable (R)	3
0	MSI Enable	0

Table Notes
The (R) indicates a read-only bit.

- **Bits 15–8 (Reserved)**
- **Bit 7 (64-bit Address Capable).** This read-only bit is hardwired to 1 to notify the host that the ISP2312 is capable of generating a 64-bit message address.
- **Bits 6–4 (Multiple Message Enable).** This field is set by host (system software) to indicate the maximum number of interrupt message codes generated by the ISP2312. The RISC processor must check this field so that the RISC can limit the number of interrupt message codes.
- **Bits 3–1 (Multiple Message Capable).** This read-only field is hardwired to 3h to notify the host that the ISP2312 can generate eight different interrupt message codes.
- **Bit 0 (MSI Enable).** When this bit is set, the ISP2312 uses MSI instead of the INTA or INTB signal to request interrupt service from the host. When this bit is reset, the ISP2312 uses the INTA or INTB signal to request interrupt service from the host. The RISC processor must check this bit before initiating an interrupt request through MSI.

6.6.21.3
PCI MSI Message Address Register

The Message Address bits (PCI MSI Message Address register bits 31–2) specify the dword-aligned address used for the address phase of the PCI MSI dword memory write transaction (see table 6-43). The AD0–1 signals must be driven to zero during the address phase.

Table 6-43. PCI MSI Message Address Register

Configuration Address Space 58 (R/W)		
Bit	**Name**	**Reset (h)**
31–2	Message Address	00000000
1–0	Reserved	0

6.6.21.4
PCI MSI Message Upper Address Register

A nonzero value in this register specifies the upper 32 bits of a 64-bit message address (AD32–63) used for the address phase of the PCI MSI dword memory write transaction (see table 6-44).

Table 6-44. PCI MSI Message Upper Address Register

Configuration Address Space 5C (R/W)		
Bit	**Name**	**Reset (h)**
31–0	Message Address	00000000

6.6.21.5
PCI MSI Message Data Register

This register contains the interrupt message code written by the ISP2312 during a PCI MSI dword memory write transaction. During the data phase of the memory write transaction, the ISP2312 drives message data on AD0–15 and zero on AD16–31 with CBE0–3 asserted.

The RISC processor writes the PCI MSI Message Data register at address 89h in the command DMA channel. The hardware allows the RISC processor to modify a maximum of the lower three bits of this register (the ISP2312 can generate a maximum of eight message codes).

- When the host allows eight message codes, the hardware unmasks the lower three bits.
- When the host allows four message codes, the hardware unmasks the lower two bits.
- When the host allows two message codes, the hardware unmasks the least significant bit.

The PCI MSI Message Data register bits are shown in table 6-45.

Table 6-45. PCI MSI Message Data Register

Configuration Address Space 60 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Message Data	0000

6.6.21.6
PCI Next Capability Item Pointer Register

The PCI Next Capability Item Pointer register is hardwired to 64h, which is the address of the next capability data structure. This structure is referred to as *hot swap* capability (see table 6-46).

Table 6-46. PCI Next Capability Item Pointer Register

Configuration Address Space 65 (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Next Capability Item Pointer	64

6.6.22
CompactPCI Hot Swap Capability ID Register

This register is hardwired to 06h to identify this group of registers as CompactPCI Hot Swap capability data structure registers (see table 6-47).

Table 6-47. CompactPCI Hot Swap Capability ID Register

Configuration Address Space 64 (R/W)		
Bit	**Name**	**Reset (h)**
7–0	CompactPCI Hot Swap Capability ID	06

6.6.23
CompactPCI Hot Swap Control and Status Register

This register provides software connection controls for the CompactPCI Hot Swap feature. The register bits are listed in table 6-48 and described in the following paragraphs.

Table 6-48. CompactPCI Hot Swap Control and Status Register

Configuration Address Space 66 (R/W)		
Bit	**Name**	**Reset (h)**
7	Hot Swap Insertion Event	1
6	Hot Swap Extraction Event	0
5–4	Reserved	0
3	Hot Swap LED On/Off	0
2	Reserved	0
1	Hot Swap Event Interrupt Mask	0
0	Reserved	0

- **Bit 7 (Hot Swap Insertion Event).** The ISP2312 sets this bit to 1 when L_STAT is sampled low in response to the operator closing the ejector handle after inserting a board and loading a system and subsystem ID from the serial EPROM. When this bit is set, ENUM is asserted on the PCI bus when the Host Swap Event Interrupt Mask bit (bit 1) is reset, indicating to the host that the board is ready for host initialization. Writing 1 to the Hot Swap Insertion Event bit clears the bit. Writing 0 to this bit has no effect.
- **Bit 6 (Hot Swap Extraction Event).** The ISP2312 sets this bit to 1 when L_STAT is sampled high in response to the operator opening the ejector handle to remove a board. When this bit is set, the L_STAT pin is driven and controlled by the Hot Swap LED On/Off bit (bit 3); ENUM is asserted on the PCI bus when the Hot Swap Event Interrupt Mask (bit 1) of this register is set. Writing 1 to the Hot Swap Extraction Event bit clears the bit. When this bit is cleared, the ISP2312 tristates the L_STAT pin so it can resume sampling the ejector handle status. Writing 0 to this bit has no effect.
- **Bits 5–4 (Reserved)**
- **Bit 3 (Hot Swap LED On/Off).** This bit allows software control of the L_STAT pin (hot swap LED). When this bit and the Hot Swap Extraction Event bit (bit 6) are reset, the ISP2312 tristates L_STAT and allows the status of the ejector switch to be sampled as an input. When the ISP2312 detects an extraction event and sets the Hot Swap Extraction Event bit, L_STAT is driven low by this bit. When the Hot Swap LED On/Off bit is set, L_STAT is driven high, forcing an LED ON condition.
- **Bit 2 (Reserved)**
- **Bit 1 (Hot Swap Event Interrupt Mask).** When this bit is reset, the ISP2312 allows an ENUM interrupt on the PCI bus when an insertion or removal event occurs. When this bit is set, the ISP2312 masks the ENUM interrupt.
- **Bit 0 (Reserved)**

6.7
PCI Bus Interface Registers

The PCI bus interface registers consist of the ISP control status, interrupt control, interrupt status, and other special function registers. They are mapped into the I/O, memory, or both address spaces of the PCI from the host processor and the RISC I/O bus from the RISC processor.

The PCI bus interface registers are duplicated in the ISP2312 for the two functions. This includes all ISP to PCI control and status registers, mailbox in and out registers, and the RISC Host Command and Control (HCCR) and GPIO registers. The PCI bus interface registers for function 0 can be accessed using the PCI I/O Base Address register or the PCI Lower and Upper Memory Base Address registers in function 0 configuration space. Similarly, the PCI bus interface registers for function 1 can be accessed using the PCI I/O Base Address register or the PCI Lower and Upper Memory Base Address registers in function 1 configuration space.

The PCI bus interface registers are listed in table 6-49 and described in the following sections. The ISP2312 registers are 16 bits wide and can be accessed as an 8-bit byte, a 16-bit halfword, or a 32-bit dword from the PCI bus.

Note the following:

- Reserved bits are reset to 0 unless otherwise noted. Register bits are set to 1 and reset or cleared to 0 unless otherwise noted. A reset value of X indicates an indeterminate value.
- Register bits allow read and write access unless otherwise noted.

Table 6-49. PCI Bus Interface Registers

RISC[a]		PCI[b]			
I/O Address	**Access[c]**	**Offset from Base Address (h)**	**Access[c]**	**Register Name**	**Reset Value (h)**
—	—	000	R/W	Flash BIOS Address	0000
—	—	002	R/W	Flash BIOS Data	X
—	—	006	R/W	ISP Control/Status	X
003	R	008	R/W	ISP to PCI Interrupt Control	0000
—	—	00A	R	ISP to PCI Interrupt Status	0000
006	R/W	00C	R/W	ISP Semaphore	0000
007	R/W	00E	R/W	ISP Nonvolatile RAM Interface	0000
00E	R/W	—	—	RISC to RISC Semaphore	0000
—	—	010	R/W	Request Queue In Pointer[d]	0000
—	—	012	R	Request Queue Out Pointer[d]	0000
—	—	014	R	Response Queue In Pointer[d]	0000
—	—	016	R/W	Response Queue Out Pointer[d]	0000
—	—	018	R	RISC to Host Status Low	0000
—	—	01A	R	RISC to Host Status High	0000
—	—	01C	R/W	Host to Host Semaphore	0000
—	—	0C0	R/W	RISC Host Command and Control	0000
—	—	0CC	R	GPIOD	000
—	—	0CE	R	GPIOE	000
—	—	040–07E	W	Incoming Mailbox	X
—	—	040–07E	R	Outgoing Mailbox	X

Table Notes

[a] "—" in these columns indicates that the register is not accessible from the RISC.

[b] "—" in these columns indicates that the register is not accessible from the PCI.

[c] R = read, R/W = read/write

[d] These registers are updated/incremented by auto-DMA channel hardware (not the RISC processor) when auto-DMA is enabled. When auto-DMA is disabled (the command DMA channel fetches the IOCB and posts status), the RISC processor updates these pointers.

6.7.1
Flash BIOS Address Register

This register allows the host to program and read the flash BIOS PROM through PCI I/O or memory space. The location (byte address) of the flash BIOS EPROM to be programmed and read is provided through this register. The PBIU drives the address value in this register onto the ISP2312 RADDR_1[0–20] and RADDR_2[0–20] pins when the Flash BIOS Read/Write Enable bit (ISP Control/Status register bit 1) is set. The register bits are shown in table 6-50.

Table 6-50. Flash BIOS Address Register

PCI Offset from Base Address 000 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Flash BIOS Byte Address	0000

6.7.2
Flash BIOS Data Register

This register allows the host to program and read the flash BIOS PROM through PCI I/O or memory space. The location (byte address) of the flash BIOS EPROM to be programmed and read is provided through the Flash BIOS Address register while the BIOS PROM data is accessed through the Flash BIOS Data register. For writes to flash BIOS, the byte value programmed into the flash BIOS is loaded in this register. The PBIU drives the flash BIOS data onto the ISP2312 PDATA pins only when the Flash BIOS Read/Write Enable bit (ISP Control/Status register bit 1) is set. For reads from flash BIOS, the access data is available through this register. The register bits are shown in table 6-51.

Table 6-51. Flash BIOS Data Register

PCI Offset from Base Address 002 (R/W)		
Bit	**Name**	**Reset (h)**
15–8	Reserved	X
7–0	Flash BIOS Data	X

6.7.3
ISP Control/Status Register

This register allows the host to control the operation of the ISP2312 and to read internal status. The register bits are shown in table 6-52 and described in the following paragraphs.

Table 6-52. ISP Control/Status Register

Addresses and Access		
RISC I/O address (R)		003
PCI offset from base address (R/W)		006
Bit	**Name**	**Reset (h)**
15–14	Function Number	Note a
13	System ID Write Enable	0
12–11	Reserved	0
10–9	PCI-X Bus Mode	Note b
8	PCI 66-MHz Enable Status	Note c
7	Reserved	0
6–4	Module Select	0
3	Flash Upper 64K Bank Select	0
2	PCI 64-Bit Bus Slot (R)	Note d
1	Flash BIOS Read/Write Enable	0
0	ISP2312 Soft Reset	0

Table Notes
The (R) indicates a read-only bit.
[a]These bits are reset to 0h for function 0 or to 1h for function 1.
[b]At power-up reset, this field is 0, 1, 2, or 3.
[c]For 66-MHz PCI bus operation, this bit is 1. For 33-MHz PCI bus operation, this bit is 0.
[d]For a 64-bit PCI bus slot, this bit is 1. For a 32-bit PCI bus slot, this bit is 0.

- **Bits 15–14 (Function Number).** This two bit field indicates the function number. For the function 0 register, these bits are set to 0h. For the function 1 register, they are set to 1h. The values 10h and 11h are reserved. These bits are hardwired to 0h for port 1 or to 1h for port 2.
- **Bit 13 (System ID Write Enable).** When this bit is set, the host can write to the device ID in the PCI Device ID register at PCI configuration address space 02h. When this bit is reset, the PCI Device ID register is read only.
- **Bits 12–11 (Reserved)**

- **Bits 10–9 (PCI-X Bus Mode).** These bits determine the PCI bus mode (conventional PCI or PCI-X), as shown in table 6-53. The pins are driven on the rising edge of RESET.

Table 6-53. PCI Bus Mode

Bits 10–9 (h)	DEVSEL	STOP	TRDY	PCI Bus Mode
0	Deasserted	Deasserted	Deasserted	PCI[a]
1	Deasserted	Deasserted	Asserted	PCI-X 66 MHz
2	Deasserted	Asserted	Deasserted	PCI-X 100 MHz
3	Deasserted	Asserted	Asserted	PCI-X 133 MHz

Table Notes
FRAME and IRDY must also be deasserted.
[a]The chip is operating in 33-MHz mode when M66EN is deasserted. The chip is operating in 66-MHz mode when M66EN is asserted.

- **Bit 8 (PCI 66-MHz Enable Status).** This bit reflects the status of the M66EN signal on the PCI bus. The M66EN pin is available on all PCI connectors that support 66 MHz. When this bit is set to 1, M66EN is asserted and the PCI bus clock frequency is in the range of 33 to 66 MHz. When this bit is 0, M66EN is deasserted and the PCI bus clock frequency is in the range of 0 to 33 MHz.
- **Bit 7 (Reserved)**
- **Bits 6–4 (Module Select).** This field allows the host to select the ISP2312 for register access. The ISP2312 internal registers for RISC, frame buffer, fibre protocol module, and DMA channels are mapped in the overlapping address space at the PCI address offset from 80h–FFh. This field allows the host to switch among the different register sets shown in table 6-54.

Table 6-54. Module Select Field

Module Select Bits (h)	Module Selected for Access by Host
0	RISC registers
1	Frame buffer registers[a]
2	Fibre protocol module registers[a, b]
3	Fibre protocol module registers[a, c]
4	Auto-DMA channels[a]
5	Command, transmit, and receive DMA channels[a]

Table Notes
[a]These module registers are accessible only by the host (PCI) when the RISC is in pause mode.
[b]RISC I/O addresses 100h–13Fh
[c]RISC I/O addresses 140h–17Fh

- **Bit 3 (Flash Upper 64K Bank Select).** When this bit and the Flash BIOS Read/Write Enable bit (bit 1) are set, the host can access the upper 64K of the 128K flash memory through the RADDR_1[16] or RADDR_2[16] pin (see section 3.2.2). When the Flash Upper 64K Bank Select bit is reset, the host access to flash memory is limited to 64K of memory.

  NOTE: Use this bit only when the host accesses the BIOS through the Flash Address and Flash Data registers. This bit is not used when the host accesses the BIOS through the Expansion ROM Base Address register.
- **Bit 2 (PCI 64-Bit Bus Slot).** This read-only bit provides information regarding the ISP2312 connection on the PCI bus. The bit is set when the ISP2312 is connected to a 64-bit PCI slot on the PCI bus and cleared when the ISP2312 is in a 32-bit slot.
- **Bit 1 (Flash BIOS Read/Write Enable).** This bit allows the flash BIOS PROM to be programmed from the host processor. When this bit is set, the RISC is held in reset and the RISC memory address bus drives the BIOS address from the Flash BIOS Address register. The data for the flash BIOS is accessed from the Flash BIOS Data register.

  NOTE: When all accesses are complete, the Flash BIOS Read/Write Enable bit must be reset and the RISC must be restarted and re-initialized.

  - ❒ All special sequences required to enable the PROM for writing are left to the programmer to implement.
  - ❒ All accesses to the I/O space in the ISP2312 are 16 bits wide. However, for this new data port, only the least significant eight bits are read or written.

WARNING!! Setting this bit resets the RISC processor.

- **Bit 0 (ISP2312 Soft Reset).** This bit allows the host to apply a soft reset to the ISP2312. Setting this bit resets the ISP2312. When the DMA controller is enabled for transfers and the request on the PCI bus is active, the reset condition occurs after the current bus cycle completes. The bit is cleared by hardware when a reset command is executed. Upon reset, all internal ISP2312 registers, except those in the PCI configuration address space, are initialized to their power-on reset values.

6.7.4
ISP to PCI Interrupt Control Register

The ISP to PCI Interrupt Control register allows the host to enable interrupts from the RISC processor, frame buffer, fibre protocol module, and DMA controller channels. The register bits are shown in table 6-55 and described in the following paragraphs.

Table 6-55. ISP to PCI Interrupt Control Register

PCI Offset from Base Address 008 (R/W)		
Bit	**Name**	**Reset (h)**
15	Enable ISP2312 Interrupts on PCI	0
14–4	Reserved	000
3	Enable RISC Interrupt on PCI	0
2–0	Reserved	0

- **Bit 15 (Enable ISP2312 Interrupts on PCI).** This bit is a global interrupt enable and disable bit for the host. Setting this bit enables interrupt requests from the RISC, frame buffer, fibre protocol module, and DMA controller channels when their associated interrupt enable bits are set. The PCI interrupt request signal INTA or INTB is driven only when an interrupt is active. Alternatively, the host can mask all interrupts from the ISP2312 by clearing this bit.
- **Bits 14–4 (Reserved)**
- **Bit 3 (Enable RISC Interrupt on PCI).** Setting this bit enables the interrupt request from the RISC to the host on the PCI INTA or INTB signal when the Enable ISP2312 Interrupts on PCI bit (bit 15) is set. Alternatively, the host can mask the PCI interrupt request INTA or INTB from the RISC by clearing this bit without changing the state of the RISC to PCI Interrupt Request bit (ISP to PCI Interrupt Status register bit 3).
- **Bits 2–0 (Reserved)**

6.7.5
ISP to PCI Interrupt Status Register

The ISP to PCI Interrupt Status register allows the host to monitor the status of interrupts from the processor, frame buffer, fibre protocol module, and DMA controller channels. This register can be read from the host only and is not accessible from the RISC processor. The register bits are shown in table 6-56 and described in the following paragraphs.

Table 6-56. ISP to PCI Interrupt Status Register

PCI Offset from Base Address 00A (R)		
Bit	**Name**	**Reset (h)**
15	ISP2312 to PCI Interrupt Request	0
14–4	Reserved	000
3	RISC to PCI Interrupt Request	0
2–0	Reserved	0

- **Bit 15 (ISP2312 to PCI Interrupt Request).** This bit is an unmasked global interrupt status bit (logical **OR** of unmasked ISP to PCI Interrupt Status register bits 5–0) for the host. It is set by active interrupt requests from the RISC processor, frame buffer, fibre protocol module, or DMA controller channels regardless of the state of interrupt enable bits in the ISP to PCI Interrupt Control register. The interrupt is driven onto the PCI INTA or INTB signal only when the corresponding interrupt enable bit and the Enable ISP2312 Interrupts on PCI bit (ISP to PCI Interrupt Control register bit 15) are set.
- **Bits 14–4 (Reserved)**
- **Bit 3 (RISC to PCI Interrupt Request).** This bit is set in response to the interrupt request from the RISC processor. The interrupt is driven onto the PCI INTA or INTB signal only when the Enable ISP2312 Interrupts on PCI bit and the Enable RISC Interrupt on PCI bit (ISP to PCI Interrupt Control register bits 15 and 3) are set.
- **Bits 2–0 (Reserved)**

6.7.6
ISP Semaphore Register

The PBIU supports a local semaphore port used by the host and RISC processor to implement the host protocol. The PBIU internally arbitrates between host and RISC processor writes, and the Semaphore Status bit (bit 1) provides appropriate semaphore status information to the winning and losing processor.

The Semaphore Lock bit is not associated with a particular hardware resource. It synchronizes the communication protocol between the host and the RISC processor when using shared resources. The local semaphore port eliminates the need for locked transfers on the PCI. The PCI Semaphore register bits are shown in table 6-57 and described in the following paragraphs.

Table 6-57. ISP Semaphore Register

Access (R/W)		
RISC I/O address		006
PCI offset from base address		00C
Bit	**Name**	**Reset (h)**
15–2	Reserved	0000
1	Semaphore Status (R)	0
0	Semaphore Lock	0

Table Notes
The (R) indicates a read-only bit.

- **Bits 15–2 (Reserved)**
- **Bit 1 (Semaphore Status).** This read-only bit is used by the processors to check the lock status of a resource. A value of 0 in this bit indicates a successful lock. A value of 1 in this bit indicates that the resource is already locked by another processor. The locked resource can be released by writing 0 to bit 0.
- **Bit 0 (Semaphore Lock).** The processor requesting the lock writes 1 to this bit, then examines the Semaphore Status bit (bit 1). A value of 0 in bit 1 indicates a successful lock. A value of 1 in bit 1 indicates that the resource was already locked by another processor. The locked resource can be released by writing 0 to the Semaphore Lock bit.

6.7.7
ISP Nonvolatile RAM Interface Register

The ISP2312 provides a four-bit serial interface to nonvolatile RAM through the ISP Nonvolatile RAM Interface register. Software drivers use this feature to save and retrieve information related to the ISP2312 configuration between power ups. The register bits are shown in table 6-58 and described in the following paragraphs.

Table 6-58. ISP Nonvolatile RAM Interface Register

Access (R/W)		
RISC I/O address		007
PCI offset from base address		00E
Bit	**Name**	**Reset (h)**
15	NVRAM Busy	0
14–4	Reserved	000
3	NVRAM Data In	X
2	NVRAM Data Out	0
1	NVRAM Chip Select	0
0	NVRAM Clock	0

- **Bit 15 (NVRAM Busy).** This bit indicates status of the NVRAM. In the ISP2312, a single NVRAM is shared by both functions. Consequently, this bit communicates the status of the NVRAM to the host or RISC processors. This bit is set to indicate that the other function is currently accessing the NVRAM. This bit is reset to indicate that the NVRAM is available for access. Once the NVRAM is available for access, the host or RISC processors need to lock the resource using semaphores.
- **Bits 14–4 (Reserved)**
- **Bit 3 (NVRAM Data In).** This bit is part of the four-bit NVRAM interface; it reads data from the NVRAM to the ISP2312. The data is read serially from the NVRAM one bit at a time.
- **Bit 2 (NVRAM Data Out).** This bit is part of the four-bit NVRAM interface; it writes data to the NVRAM from the ISP2312. The data is written serially to the NVRAM one bit at a time.

- **Bit 1 (NVRAM Chip Select).** This bit is part of the four-bit NVRAM interface; it selects the NVRAM for data read and write operations.
- **Bit 0 (NVRAM Clock).** This bit is part of the four-bit NVRAM interface; it provides the clock that shifts data in and out of the NVRAM.

6.7.8
RISC to RISC Semaphore Register

This register allows two RISC processors to share a common resource through the use of semaphores. This register is read/write only from the RISC processor; it is not accessible from the host over the PCI bus.

The RISC Semaphore Lock/Status bit (bit 0) is used by the RISC processors to lock shared a resource, for example, the NVRAM. To lock a resource, the RISC processor sets this bit to 1 and checks the status. When the status is set to 1, then the RISC processor has successfully locked the resource. When the status is 0, then the lock was unsuccessful. The RISC to RISC Semaphore register is shown in table 6-59.

Table 6-59. RISC to RISC Semaphore Register

RISC I/O Address 00E (R/W)		
Bit	**Name**	**Reset (h)**
15–1	Reserved	0000
0	RISC Semaphore Lock/Status	0

6.7.9
Auto-Request Registers

The auto-request DMA channel automatically moves IOCBs that are queued in host memory into the RISC RAM. Once initialized, the DMA channel monitors the Request Queue In-Pointer register to determine when there are IOCBs queued to be processed. The DMA channel then starts a DMA operation and moves the IOCBs into an internal FIFO. The IOCBs are then moved into RISC memory utilizing a RISC memory DMA interface.

The auto-response DMA channel automatically moves I/O status information from RISC memory to host memory.

6.7.9.1
Request Queue In-Pointer Register

The Request Queue In-Pointer register is written/incremented by the host to indicate that an IOCB has been placed on the request queue.

The Request Queue In-Pointer register is read by the ISP2312 hardware to determine when an IOCB from the host memory needs to be fetched (see table 6-60).

Table 6-60. Request Queue In-Pointer Register

PCI Offset from Base Address 010 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Request Queue In-Pointer	0000

6.7.9.2
Request Queue Out-Pointer Register

The Request Queue Out-Pointer register is updated/incremented by hardware after each IOCB is fetched from the request queue. This register is also read by the host to determine when the request queue is full (see table 6-61).

Table 6-61. Request Queue Out-Pointer Register

PCI Offset from Base Address 012 (R)		
Bit	**Name**	**Reset (h)**
15–0	Request Queue Out-Pointer	0000

6.7.9.3
Response Queue In-Pointer Register

The Response Queue In-Pointer register is updated/incremented by the ISP2312 hardware as a DMA channel posts I/O status information in host memory. The host determines that there is a new entry in the response queue by comparing the Response Queue In-Pointer register with the Response Queue Out-Pointer register (see table 6-62).

Table 6-62. Response Queue In-Pointer Register

PCI Offset from Base Address 014 (R)		
Bit	**Name**	**Reset (h)**
15–0	Response Queue In-Pointer	0000

6.7.9.4
Response Queue Out-Pointer Register

The Response Queue Out-Pointer register is updated/incremented by the host and used by the ISP2312 hardware to determine when there is queue space available to post more I/O status information in host memory (see table 6-63).

Table 6-63. Response Queue Out-Pointer Register

PCI Offset from Base Address 016 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Response Queue Out-Pointer	0000

6.7.10
RISC to Host Status Low and High Registers

The RISC to Host Status Low and High registers provide I/O completion and interrupt-related information to the host. These registers are write-only from the RISC processor and read only from the host. The register bits are shown in table 6-64 and described in the following paragraphs.

Table 6-64. RISC to Host Status Low and High Registers

PCI Offset from Base Address		
Access	**Low**	**High**
(R)	018	01A

Bit	Name	Reset (h)
31–16	Interrupt Information (firmware defined)	0000
15	RISC to Host Interrupt Request	0
14–10	Reserved	00
9	Semaphore Status	0
8	RISC Paused	0
7–0	Interrupt Status (firmware defined)	00

- **Bits 31–16 (Interrupt Information).** This 16-bit field is used by the RISC processor to post firmware-defined interrupt information to the host.
- **Bit 15 (RISC to Host Interrupt Request).** This bit is a copy of the RISC to PCI Interrupt Request bit (ISP to PCI Interrupt Status register bit 3). The RISC to Host Interrupt Request bit is set in response to an interrupt request from the RISC processor. The RISC interrupt condition is cleared when the host reads this register.
- **Bits 14–10 (Reserved)**
- **Bit 9 (Semaphore Status).** This bit is a copy of the Semaphore Status bit (ISP Semaphore register bit 1). A value of 0 in this bit indicates a successful lock. A value of 1 in this bit indicates that the resource is already locked by another processor.
- **Bit 8 (RISC Paused).** When this bit is set, the RISC processor is in pause mode. When this bit is reset, the RISC processor is running.
- **Bits 7–0 (Interrupt Status).** This eight-bit field is used by the RISC processor to post firmware-defined interrupt status information to the host.

6.7.11
Host to Host Semaphore Register

This register allows two host processes to share a common resource through the use of semaphores. This register is read/write only from the host.

The Host Semaphore Lock/Status bit (bit 0) is used by the host for functions 0 and 1 to lock a shared resource, for example, the NVRAM. To lock a resource, the host sets this bit to 1 and checks the status. When the status is set to 1, then the host has successfully locked the resource. When the status is 0, then the lock was unsuccessful. The Host to Host Semaphore register is shown in table 6-65.

Table 6-65. Host to Host Semaphore Register

PCI Offset from Base Address 01C (R/W)		
Bit	**Name**	**Reset (h)**
15–1	Reserved	0000
0	Host Semaphore Lock/Status	0

6.7.12
RISC Host Command and Control Register

The Host Command and Control register (HCCR) controls hardware operating modes and conditions within the RISC processor. The HCCR is initialized to 0 at power up.

HCCR register bits are shown in table 6-66 and described in the following paragraphs.

Table 6-66. Host Command and Control Register

PCI Offset from Base Address 0C0 (R/W)		
Bit	**Name**	**Reset (h)**
15–12	HCCR Command Field	0
11	External Parity Error (R)	0
10	External RAM Parity Enable (R)	0
9	Frame Buffer Parity Error Mask Status (R)	0
8	Frame Buffer Parity Error (R)	0
7	Host Interrupt (R)	0
6	PCI to RISC Reset (R)	0
5	RISC Pause (R)	0
4–0	Reserved	00

Table Notes
The (R) indicates a read-only bit.

- **Bits 15–12 (HCCR Command Field).** The host controls the RISC processor through these bits by setting or resetting individual control bits and modes. Table 6-67 defines the HCCR command field codes.

Table 6-67. HCCR Command Field Codes

Bits 15–12 (h)	Command	Operation	Register Bits Affected
0	NOP	Performs no function	—
1	Reset RISC	Toggles (sets, then resets) the hard reset to the RISC processor.	—
2	Pause RISC	Sets pause mode in the RISC processor. The RISC processor sets the RISC Pause bit in the HCCR at the end of the current instruction.	HCCR bit 5
3	Release RISC	Releases the RISC processor from either reset or pause mode. The Reset or RISC Pause bit is cleared after this command completes.	HCCR bit 5
4	Mask Frame Buffer Parity	When bit 0 is set, the RISC processor is not paused on a frame buffer parity error.	HCCR bit 9
5	Set Host Interrupt	Sets the interrupt from the host to the RISC processor. The status of the host interrupt is reflected in the Host Interrupt bit (HCCR bit 7).	HCCR bit 7
6	Clear Host Interrupt	Clears the interrupt from the host to the RISC processor. The status of the host interrupt is reflected in the Host Interrupt bit (HCCR bit 7). This bit may also be cleared by the RISC processor.	HCCR bit 7
7	Clear RISC Interrupt	Clears the RISC interrupt to the host	PSR bit 13
A	Parity Enable	Enables parity when bit 0 is set; disables parity when bit 0 is reset.	HCCR bit 10
E	Force Parity Error	Generates wrong parity on write data to memory for test purposes	—

- **Bit 11 (External Parity Error).** When this bit is set, a parity error was captured from the external RAM read cycle. This bit pauses the RISC processor. This bit is active only when parity checking is set through the PCR (PCR Command Field bits (bits 15–12) equal 9) or bit 10 (External RAM Parity Enable) of this register.
- **Bit 10 (External RAM Parity Enable).** When this bit is set, parity checking is enabled.
- **Bit 9 (Frame Buffer Parity Error Mask Status).** This bit indicates when the parity error from frame buffer has been masked from RISC processor.
- **Bit 8 (Frame Buffer Parity Error).** When this bit is set, the RISC processor received bad parity from the frame buffer. When the Frame Buffer Parity Error Mask Status bit (bit 9) is reset, the RISC processor is paused.
- **Bit 7 (Host Interrupt).** This bit indicates the current status of the host interrupt to the RISC processor. The interrupt is active when the bit is set and inactive when the bit is cleared. The Host Interrupt bit is set or cleared by the HCCR Command Field bits (bits 15–12); it cannot be written to directly. This bit may also be cleared by the RISC processor in response to the interrupt.

  This bit implements an interlocked communication protocol between the host and the RISC processor.

- **Bit 6 (PCI to RISC Reset).** When this bit is set, the RISC processor is in reset mode. The PCI to RISC Reset bit is set by the PCI module; it cannot be written to directly. When the RISC processor is reset, all control and status bits are cleared.
- **Bit 5 (RISC Pause).** This bit indicates the RISC processor pause mode status. This bit is set under one of the following conditions:
  - The HCCR issues a command to pause the RISC processor.
  - Parity checking is enabled and the RISC processor receives a parity error.
  - The frame buffer parity error is not masked (the HCCR Command Field bits (bits 15–12) equal 4), and the RISC processor receives a parity error from the frame buffer.
- **Bits 4–0 (Reserved)**

6.7.13 GPIOD Register

The GPIO pins (see table 6-68) can be accessed through the General Purpose I/O Data (GPIOD) register. It is not necessary to pause the RISC processor for host access to this register. However, the host driver and the RISC firmware must coordinate the use of this register. At power-up reset, the RISC firmware controls the GPIO pins. The host driver can take control of these pins by issuing the Set Firmware Options (0038h) mailbox command to the RISC firmware. See the *2300 Series Firmware Interface Specification* (83230-660-00) for more information.

Table 6-68. Corresponding GPIO Pins and Registers

Pin Name	GPIOD Register	GPIOE Register
GPIO7	Bit 7	Bit 7
GPIO6	Bit 6	Bit 6
GPIO5	Bit 5	Bit 7
GPIO4	Bit 4	Bit 4
GPIO3	Bit 3	Bit 3
GPIO2	Bit 2	Bit 2
GPIO1	Bit 1	Bit 1
GPIO0	Bit 0	Bit 0

The GPIOD register bits are shown in table 6-69.

Table 6-69. GPIOD Register

PCI Offset from Base Address 0CC (R)		
Bit	**Name**	**Reset (h)**
15–6	Reserved	000
7–0	GIOD Data In (R), GPIO Data Out (W)	X

NOTE: For QLogic HBA designs, the GPIO_1[0, 7–6] and GPIO_2[0, 7–6] pins are programmed to control the LEDs on the HBA. These pins are controlled by the RISC firmware to indicate I/O activity and status information. They cannot be used for any other purpose.

6.7.14
GPIOE Register

The GPIOE register sets the direction of the GPIO pins as input or output. Setting the GPIO Enables bits (bits 7–0) changes the direction of the corresponding GPIO pins to output data.

The GPIO pins (see table 6-68) can be accessed through the GPIOE register (see table 6-70). It is not necessary to pause the RISC processor for host access to this register.

Table 6-70. GPIOE Register

PCI Offset from Base Address 0CE (R)		
Bit	**Name**	**Reset (h)**
15–6	Reserved	000
7–0	GPIO Enables	00

6.7.15
Mailbox Registers

The mailbox 0–31 registers are special function registers that allow communication between the host and the processor. The mailbox registers are listed in table 6-71. The operation of the registers is described in the following paragraphs, but the protocol for their use is defined strictly by the programmer.

Table 6-71. Mailbox Registers

PCI Offset from Base Addr (h)	PCI Access[a]	Mailbox Number	Reset Value (h)[b]
Incoming Mailbox Registers			
040	W	0	X
042	W	1	X
044	W	2	X
046	W	3	X
048	W	4	X
04A	W	5	X
04C	W	6	X
04E	W	7	X
050	W	8	X
052	W	9	X
054	W	10	X
056	W	11	X
058	W	12	X
05A	W	13	X
05C	W	14	X
05E	W	15	X
060	W	16	X
062	W	17	X
064	W	18	X
066	W	19	X
068	W	20	X
06A	W	21	X
06C	W	22	X
06E	W	23	X
070	W	24	X
072	W	25	X
074	W	26	X
076	W	27	X
078	W	28	X
07A	W	29	X
07C	W	30	X
07E	W	31	X
Outgoing Mailbox Registers			
040	R	0	X
042	R	1	X
044	R	2	X
046	R	3	X
048	R	4	X
04A	R	5	X
04C	R	6	X
04E	R	7	X
050	R	8	X
052	R	9	X
054	R	10	X
056	R	11	X
058	R	12	X
05A	R	13	X
05C	R	14	X
05E	R	15	X
060	R	16	X

Table 6-71. Mailbox Registers (Continued)

Table 6-71. Mailbox Registers (Continued)

PCI Offset from Base Addr (h)	Access[a]	Mailbox Number	Reset Value (h)[b]
062	R	17	X
064	R	18	X
066	R	19	X
068	R	20	X
06A	R	21	X
06C	R	22	X
06E	R	23	X
070	R	24	X
072	R	25	X
074	R	26	X
076	R	27	X
078	R	28	X
07A	R	29	X
07C	R	30	X
07E	R	31	X

Table Notes
[a]R = read, W = write
[b]A rest value of X indicates an indeterminate value.

The mailbox registers may be written by the RISC processor or the host. The 32 registers are actually two banks of 32 registers each. Although the hardware consists of 64 registers, the registers are mapped to appear as 32 register locations. To reduce the chances of conflict, each of the two register banks is unidirectional. The host writes information to bank 0 and reads information from bank 1. The RISC processor access is exactly the opposite. This bank switching occurs automatically and is transparent to the programmer, but must be understood to use the registers effectively. The mailbox register data paths are illustrated in figure 6-8.

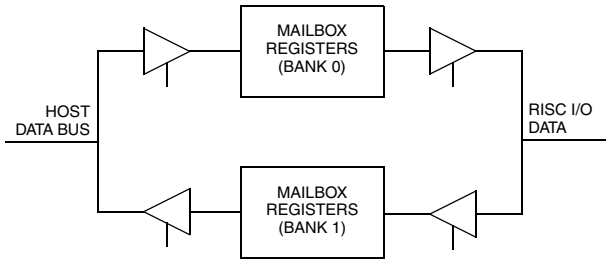


Figure 6-8. Mailbox Register Data Paths

Section 7
RISC Interface

7.1 Introduction

The RISC interface connects the ISP2312's internal RISC processor to external synchronous Static RAM (SRAM). The RADDR_1[0–20] and RADDR_2[0–20] signals also provide an address to the flash ROM during BIOS accesses. The RISC interface can be implemented using SRAMs configured as 128K x 18, 256K x 18, 512K x 18, 1M × 18, or 2M × 18.

7.2 RISC Signal Connections

The RISC interface signals are listed in table 7-1.

Table 7-1. RISC Interface Pins

Pin Name	Type	Description	Mandatory
$\overline{\text{RADDR20\_1}}$ $\overline{\text{RADDR20\_2}}$	O O	Inverted RISC memory address bus bit 20	No
$\overline{\text{RADDR19\_1}}$ $\overline{\text{RADDR19\_2}}$	O O	Inverted RISC memory address bus bit 19	No
RADDR_1[18] RADDR_2[18]	O O	Inverted RISC memory address bus bit 18	No
RDPAR_1 RDPAR_2	I/O I/O	RISC parity bit (odd)	No
IF_1 IF_2	O O	Instruction fetch	No
RADDR_1[0–16] RADDR_2[16–20]	O O	RISC memory address bus	Yes
RADDR_1[17–20] RADDR_2[17–20]	O O	RISC memory address bus	No
RDATA_1[0–15] RDATA_2[0–15]	I/O I/O	RISC data bus	Yes
RISCSTB_1 RISCSTB_2	O O	RISC strobe	No
CLKOUT_1 CLKOUT_2	O O	RISC clock to external SRAM	Yes
$\overline{\text{ROE\_1}}$ $\overline{\text{ROE\_2}}$	O O	Output enable (SRAM)	Yes
$\overline{\text{WE\_1}}$ $\overline{\text{WE\_2}}$	O O	Write enable (SRAM)	Yes

7.2.1 Basic RISC Interface Connections

The RISC interface is a simple, synchronous SRAM interface. Output pins RADDR_1[0–20] and RADDR_2[0–20] provide the SRAM address and bidirectional pins RDATA_1[0–15] and RDATA_2[0–15] move data into or out of the SRAM.

The bidirectional RDPAR_1 and RDPAR_2 pins provide optional parity protection on the external SRAM. RDPAR_1 and RDPAR_2 are the parity bits for data on the RDATA_1[0–15] and RDATA_2[0–15] buses. Parity is disabled by default and must be enabled when initializing the firmware when parity protection is desired. The RDPAR_1 and RDPAR_2 pins always drive correct odd parity on write cycles, whether or not parity has been enabled. Parity is checked only on reads when it has been enabled.

The ISP2312's 16-bit RISC processor requires a 16-bit wide memory interface. The RISC instruction code occupies the SRAM address space from 0800h to 0FFFh. RISC SRAM memory allocation is shown in figure 7-1.

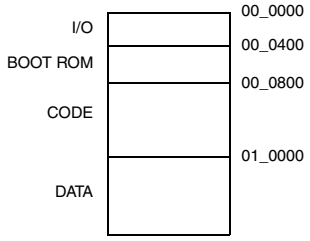


Figure 7-1. RISC External SRAM Map

For most configurations, a RISC SRAM size of 128K×18 is sufficient. Using a 256K×18 size may improve performance in some high-activity applications. For virtual interface (VI) protocol support, QLogic recommends a minimum SRAM size of 2M bytes.

The ISP2312 supports the following SRAM device sizes:

- 128K×18
- 256×18
- 512K×18
- 1M×18
- 2M×18

The common signals are address (ADDR), data (RDATA_1[0–15] and RDATA_2[0–15]), clock (CLKOUT_1 and CLKOUT_2), output enable (ROE_1 and ROE_2) and write enable (WE_1 and WE_2). These signals must be connected to each of the SRAM devices (see figure 7-2).

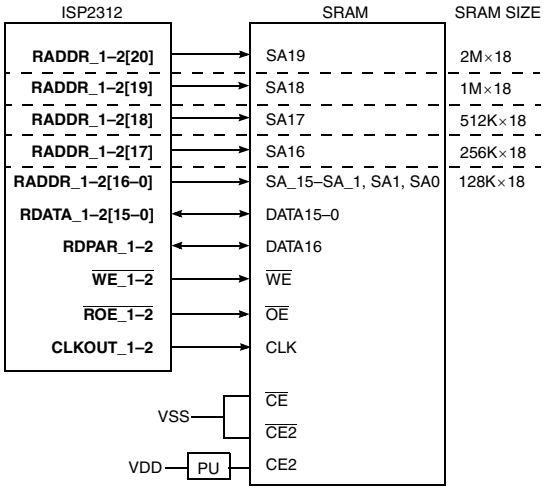


Figure 7-2. SRAM Connections

The maximum access time requirements for the external SRAMs is 6.8 nsec. The trace length requirement for connection between the SRAM and ISP2312 is determined by the following equation:

$$CLKOUT_{length} + RDATA[15–0]_{length} < 4 \text{ inches}$$
$$CLKOUT_{length} + RDPAR_{length} < 4 \text{ inches AND}$$
$$RDPAR_{length} – CLKOUT_{length} < 1.7 \text{ inches}$$

Table 7-2 lists the SRAM devices recommended for use with the ISP2312. The SRAM device I/O pad voltage must be 3.3 volts (the ISP2300/2310 I/O pads run at 3.3 volts).

Table 7-2. Recommended SRAM Devices

Manufacturer	Part Number
Cypress	CY7C1363B-133AC
GSI	GS880F18BT-6.5
GSI	GS816018T-200
GSI	GS88018BT-200
IDT	IDT71V3579S65PF
Micron	MT58L128L18FT-6.8
Samsung	K7B401825B-QC65
Samsung	K7B801825B-QC65

NOTE: The RISC SRAM interface supports loading for only one SRAM device. Stacking multiple smaller configuration SRAMs to obtain a large SRAM size is not supported.

7.2.2
Debug Connections

The RISC processor is an integral part of the ISP2312 design. Consequently, it is important to be able to trace its activity during debugging.

NOTE: QLogic strongly recommends that boards designed using the ISP2312 add test points to the signals listed below. If these signals are not accessible, debugging certain types of problems can be difficult or impossible.

Test points must be added to the following signals; doing so meets the minimum requirements to trace the RISC processor.

- CLKOUT_1/CLKOUT_2
- IF_1/IF_2
- RADDR_1[0–20]/RADDR_2[0–20] (depends on SRAM size)
- RDPAR_1/RDPAR_2
- RISCSTB_1/RISCSTB_2
- $\overline{\text{WE\_1}}$/$\overline{\text{WE\_2}}$
- $\overline{\text{ROE\_1}}$/$\overline{\text{ROE\_2}}$

Test points must also be added to the following signals to meet all the requirements to trace the RISC processor:

- RDATA_1[0–15]/RDATA_2[0–15]
- PDATA9–0

The RISCSTB_1/RISCSTB_2 and IF_1/IF_2 interface pins implement optional features and are not required for the ISP2312 to operate. These signals are described in the following paragraphs.

The RISCSTB_1/RISCSTB_2 and IF_1/IF_2 signals work together to indicate the status and type of memory access taking place at any given time on the RISC interface. These signals are valid only on the rising edge of CLK.

There are two kinds of memory accesses made by the RISC: instruction fetches and data fetches. When the RISCSTB_1/RISCSTB_2 signals are active on the rising edge of the CLK signal, a read access is finishing and the contents of the RDATA bus is clocked into internal registers. On the same clock edge, the IF_1/IF_2 signals indicate whether the access is for a data fetch or an instruction fetch.

Knowing the access type is useful for tracing RISC program execution with a logic analyzer. Accesses can be decoded according to table 7-3.

Table 7-3. RISC Memory Access Decoding

RISCSTB_1/ RISCSTB_2	IF_1/IF_2	Access Type
0	0	None
0	1	None
1	0	Data fetch
1	1	Instruction fetch

Section 8
NVRAM Interface

8.1 Introduction

Nonvolatile RAM (NVRAM) is also referred to as the serial EPROM. The NVRAM interface accesses nonvolatile storage through the ISP2312 with no external support logic. The NVRAM is used for two purposes:

- To update and store system configuration parameters when the ISP2312 is used in a host adapter application
- To store the PCI subsystem ID and the PCI subsystem vendor ID

The ISP2312 supports only NVRAM devices configured as 256 x 16 (4K bits). The first 128 locations (00h–7Fh) are used by function 0 to store parameters specific to port 1. The upper 128 locations (80h–FFh) are used by function 1 to store parameters specific to port 2. These parameters include subsystem ID values for the PCI configuration registers. The following EPROM locations are used for subsystem IDs for each function.

- Function 0/port 1
  - Subsystem vendor ID (location 7Dh)
  - Subsystem ID (location 7Eh)
- Function 1/port 2
  - Subsystem vendor ID (location FDh)
  - Subsystem ID (location FEh)

Implementing the NVRAM interface is optional and depends on the chip's operating environment. **Regardless of the environment, the NVRAM is required when standard QLogic software drivers are used.**

When custom drivers are used, then the NVRAM is not required (but it may be desirable). Host adapter applications often use this interface; motherboard or dedicated applications may not. The NVRAM is not required for the ISP2312 to operate; however, it is required to implement the PCI subsystem ID and PCI subsystem vendor ID.

> ***NOTE:*** When NVRAM is not used, pull up NVDATI through a 10k-ohm resistor or pull it down to ground.

For details on how to control this interface, see section 6.7.7.

8.2 NVRAM Signal Connections

The NVRAM interface signals are listed in table 8-1.

Table 8-1. NVRAM Interface Pins

Pin Name	Type	Description
$\overline{\text{IDENB}}$	I	Subsystem ID enable
NVCLK	O	NVRAM clock
NVCS	O	NVRAM chip select
NVDATI	I	NVRAM data in
NVDATO	O	NVRAM data out

Connecting the NVRAM interface pins to the NVRAM device is straightforward. Each of the pins listed in table 8-1 is connected directly to the corresponding pin on the NVRAM device (see figure 8-1). Table 8-2 lists the NVRAM device recommended for use with the ISP2312.

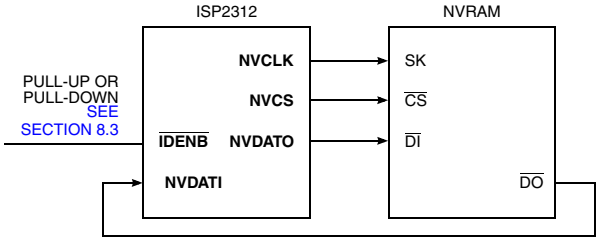


Figure 8-1. ISP2312 NVRAM Connections

Table 8-2. Recommended NVRAM Devices

Manufacturer	Part Number
Fairchild	FM93C66ALM8
Microchip	93LC66B-SN
ST Microelectronics	M93C66-WMN1
Atmel	AT93C66-10SC-2.7

8.3 Subsystem ID and Subsystem Vendor ID

The ISP2312 can automatically load a PCI subsystem ID and PCI subsystem vendor ID from the external NVRAM after any PCI reset. The values loaded then appear in PCI configuration space in the corresponding fields. Since the loading is done by hardware, the location of the IDs in the NVRAM must be fixed, as shown in table 8-3.

Table 8-3. PCI Subsystem ID and Subsystem Vendor ID Locations

Function/ Port	ID Name	NVRAM Location	PCI Configuration Space Location
0/1	PCI subsystem vendor ID	7Dh	2Ch
	PCI subsystem ID	7Eh	2Eh
1/2	PCI subsystem vendor ID	FDh	2Ch
	PCI subsystem ID	FEh	2Eh

Automatically loading the IDs can be enabled or disabled using the IDENB input pin. When IDENB is pulled down, the automatic loading function is enabled. Any PCI accesses to the ISP2312 while the IDs are being loaded are terminated with a retry. When IDENB is pulled up, the automatic loading function is disabled and the corresponding values in the PCI configuration space are zeroes.

8.4 Host Adapter Applications

In host adapter applications, it is useful to store system configuration and operating parameters in nonvolatile storage. QLogic host adapters use the NVRAM for this purpose. These parameters can include device specific information, system parameters, and/or firmware initialization parameters. Only the software driver has access to the NVRAM interface through a special register in the ISP2312 (see section 6.7.7).

The software driver reads the data from the NVRAM at power up and uses the data to format initialization commands to the RISC firmware.

The NVRAM is required when using QLogic drivers.

The world wide name (WWN) is stored in the ISP2312 NVRAM.

Section 9
Flash ROM Interface

9.1 Introduction

The flash ROM interface allows PCI BIOS read access to a BIOS ROM. The BIOS is accessed through the PCI memory address space and is programmed in the PCI Expansion ROM Base Address register (see section 6.6.13). The ISP2312 supports eight-bit flash ROM devices up to 128K bytes deep. This interface is required only in a host adapter application. The RISC address bus RADDR_1[0–16]/RADDR_2[0–16] pins provide the BIOS address to the ROM. The eight-bit flash ROM data bus is connected to the PDATA0–7 pins.

The flash BIOS may also be accessed through the Flash BIOS Address register and the Flash BIOS Data register (see sections 6.7.1 and 6.7.2). The utility software that programs and verifies the flash BIOS uses these interfaces.

The RISC cannot execute while the BIOS ROM path is being used; when the BIOS enable bit in the PCI configuration space is active, the RISC is reset.The RISC must be re-initialized after the BIOS accesses are complete and the BIOS enable bit has been cleared.

Flash ROM is required when using QLogic drivers.

9.2 Flash ROM Signal Connections

A special register interface in the PCI section allows writes to the flash ROM (see sections 6.7.1 and 6.7.2). This interface automatically generates all of the correct control signals and timing for writing data to the flash ROM.

To connect the flash BIOS to port 1, use RADDR_1[0–16], FLASHCS_1, FLASHOE, FLASHWR, and PDATA0–7.

To connect the flash BIOS to port 2, use RADDR_2[0–16], FLASHCS_2, FLASHOE, FLASHWR, and PDATA0–7.

FLASHOE, FLASHWR, and PDATA0–7 are shared between the two ports.

Table 9-1 lists the pins used in the flash ROM interface.

Table 9-1. Flash ROM Interface Pins

Pin Name	Type	Function
FLASHCS_1	I/O	Flash chip select
FLASHCS_2	I/O	Flash chip select
FLASHOE	O	Flash output enable
FLASHWR	O	Flash write
PDATA0–7	I/O	BIOS PROM data bus
RADDR_1[0–16] RADDR_2[0–16]	O O	Flash address bus (bits 0–16)

Figure 9-1 shows how the flash ROM is connected to the ISP2312. If writing to the flash ROM is not required, an EPROM can be used instead with its output enable pulled down.

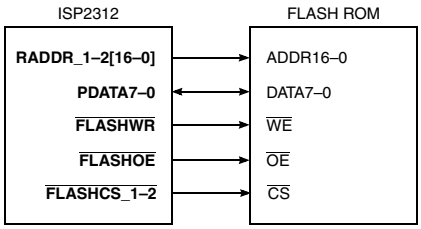


Figure 9-1. Flash ROM Connection

The maximum access time for the BIOS ROM is 120 ns.

Table 9-2 lists the recommended flash ROM devices.

Table 9-2. Recommended Flash ROM Devices

Manufacturer	Part Number
AMD	AM29LV010B-90EC
ST Microelectronics	M29W010B90N1

Section 10
Fibre Channel Interface

10.1 Introduction

This section describes the Fibre Channel copper and optical serial interfaces to the ISP2312.

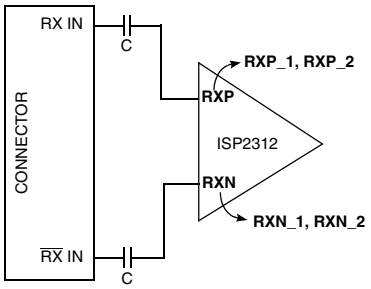
10.2 Fibre Channel Copper Interface Signal Connections

Table 10-1 lists the ISP2312 pins used in the copper serial transceiver interface.

Table 10-1. Serial Interface Pins (Copper)

Pin Name	Type	Description
REFCLK1	I	106.25-MHz reference clock
RXP_1/RXP_2	I	Receive serial data in pair
RXN_1/RXN 2	I	
TXP_1/TXP_2	O	Transmit serial data out pair
TXN_1/TXN_2	O	

The connections for the receiver are illustrated in figure 10-1.



C = DIELECTRIC LABS,
PART NUMBER C08BLBB1X5UX

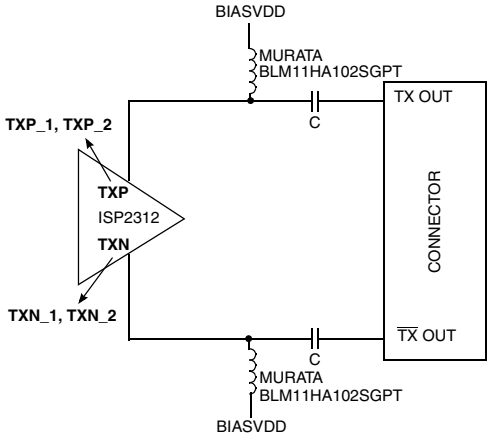
Figure 10-1. Receiver Termination (Copper)

Figure 10-1 illustrates the positional layout of the components as well as the symmetry of each leg of the differential pair. An AC coupled topology is used; standard 0.01-µF capacitors give satisfactory results. Placement of the DC blockers is not critical; however, they must be located away from other discontinuities and opposite each other. Table 10-2 lists the connector recommended for use with the ISP2312.

Table 10-2. Recommended Connector

Manufacturer	Part Number
AMP	636181-1

The connections for the transmitter are illustrated in figure 10-2.



C = DIELECTRIC LABS,
PART NUMBER C08BLBB1X5UX

Figure 10-2. Transmitter Termination (Copper)

Figure 10-2 illustrates the positional layout of the components as well as the symmetry of each leg of the differential pair. An AC coupled topology is used; standard 0.01-µF capacitors give satisfactory results. Placement of the DC blockers is not critical; however, they must be located away from other discontinuities and opposite each other. Placement of the inductors is not critical; however, they must be located away from other discontinuities. Where possible, choose components that have the smallest possible footprint and still dissipate enough power. Locate the series resistors on the component side of the board, just ahead of the transmitter pins.

NOTE: The application or driver software must program the 50-ohm Termination bit (firmware initialization control block, Special Options field, bit 13), assuring that the transmitter and receiver termination values are set correctly for the respective interface types. When this bit is set to 1, 50-ohm termination is enabled; when this bit is reset to 0, 75-ohm termination is enabled. For more information, see the *ISP2300/2310/2312 Firmware Interface Specification*.

10.2.1
Trim Resistors

These pins provide the trimming circuit input to set the desired internal termination resistance. TRIMRES_1/TRIMRES_2 must be connected to RXVDD through a 2.74k-ohm (±1 percent) resistor.

NOTE: To accommodate future versions of the ISP2312 family, QLogic recommends that the PCB be designed such that the 2.74k-ohm resistors can be easily replaced with 750-ohm resistors.

10.3
Fibre Channel Optical Interface Signal Connections

Table 10-3 lists the ISP2312 pins used in the optical serial transceiver interface.

Table 10-3. Serial Interface Pins (Optical)

Pin Name	Type	Description
REFCLK1	I	106.25-MHz reference clock
RXP_1/RXP_2 RXN_1/RXN_2	I I	Receive serial data in pair
TXP_1/TXP_2 TXN_1/TXN_2	O O	Transmit serial data out pair

The connections for the receiver are illustrated in figure 10-3.

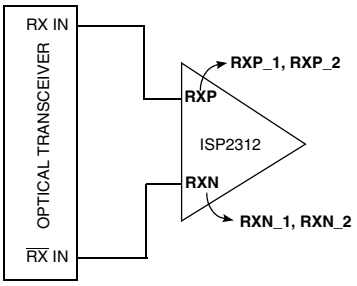


Figure 10-3. Receiver Termination (Optical)

Figure 10-3 illustrates the positional layout of the components as well as the symmetry of each leg of the differential pair. An internally terminated and decoupled optical transceiver module replaces the connector.

The connections for the transmitter are illustrated in figure 10-4.

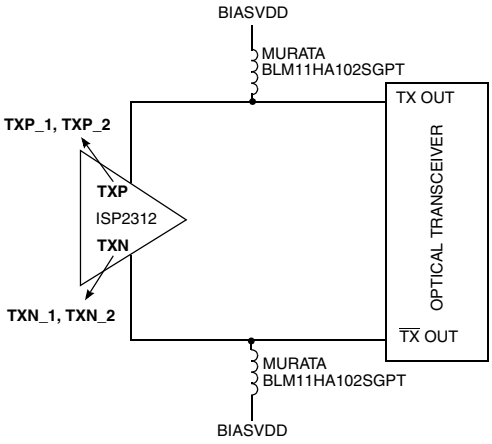


Figure 10-4. Transmitter Termination (Optical)

Figure 10-4 illustrates the positional layout of the components as well as the symmetry of each leg of the differential pair. As with the receiver, an internally terminated and decoupled optical transceiver module replaces the connector. Placement of the inductors is not critical; however, they must be located away from other discontinuities. Where possible, choose components that have the smallest possible footprint and still dissipate enough power. Locate the series resistors on the component side of the board, just ahead of the transmitter pins.

NOTE: The application or driver software must program the 50-ohm Termination bit (firmware initialization control block, Special Options field, bit 13), assuring that the transmitter and receiver termination values are set correctly for the respective interface types. When this bit is set to 1, 50-ohm termination is enabled; when this bit is reset to 0, 75-ohm termination is enabled. For more information, see the *ISP2300/2310/2312 Firmware Interface Specification.*

10.3.1
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NOTE: To accommodate future versions of the ISP2312 family, QLogic recommends that the PCB be designed such that the 2.74k-ohm resistors can be easily replaced with 750-ohm resistors.

Section 11
JTAG Boundary Scan Interface

11.1 Introduction

The ISP2312 implements a JTAG boundary scan function. This scan function verifies connectivity in a board manufacturing environment. The available test tools generate the patterns required and the JTAG control signals for this kind of testing.

11.2 JTAG Signal Connections

The JTAG interface signals are listed in table 11-1.

Table 11-1. JTAG Interface Pins

Pin Name	Type	Function
TCK	I	Test clock
TDI	I	Test data in
TDO	O	Test data out
TMS	I	Test mode select
$\overline{\text{TRST}}$	I	Test reset

In JTAG mode, TDO signals the JTAG boundary scan definition. When the ISP2312 is reset and $\overline{\text{TRST}}$ is reset, all I/Os are tristated. During JTAG test mode ($\overline{\text{TRST}}$ is deasserted), the $\overline{\text{RESET}}$ pin functions as described in section 3.2.7. The $\overline{\text{RESET}}$ pin is part of the JTAG chain.

The JTAG ID register bits are listed in table 11-2 and described in the following paragraphs. These pins are usually connected to a test connector of some type and driven by external test equipment. Unused inputs can be pulled down.

Table 11-2. JTAG ID Register

Bit	Name	Reset (h)
31–28	Version	1
27–12	JTAG Part Number	0F
11–1	Manufacturer Number	97
0	Reserved	1

- **Bits 31–28 (Version).** These bits contain the version number of the ISP2312.
- **Bits 27–12 (JTAG Part Number).** These bits contain the JTAG part number.
- **Bits 11–1 (Manufacturer Number).** These bits contain the manufacturer number, as registered with the JTAG committee.
- **Bit 0 (Reserved).** This bit is set to 1 per the JTAG standard.

11.3 BSDL File

A text file, commonly called a BSDL file, defines the I/Os of the chip. This file is input to the test software to describe the chip under test. QLogic provides a BSDL file for the ISP2312. It will be available for current customers through QLogic's protected web site. If you do not have access to the protected web site, please contact QLogic.

Section 12
Sense Pins

12.1 Introduction

During a PCI bus reset (RESET), the ISP2312 samples several sense pins to determine the following settings:

- PCI clock frequency
- RISC clock frequency
- PCI-X mode
- PCI bus width
- Test modes
- System and subsystem ID load
- The sense pins are programmed by placing an external 4.7k-ohm pull-up or pull-down resistor on each pin. (Each pin has a weak, internal pull-up or pull-down resistor to select the default mode when no external resistors are present.)

NOTE: To affect ISP2312 functionality, these pins must be pulled up or pulled down during a PCI bus reset.

12.2 PCI-X Mode

The FRAME, IRDY, DEVSEL, STOP, and TRDY pins are sampled at PCI bus reset to determine the ISP2312 PCI-X mode. The system compares the voltage levels of the ISP2312 M66EN pin (solder ball AD11) and the PCI bus PCI-X capability (PCIXCAP) pin (pin 38B) to determine the operating capabilities of various devices on the bus, and drives the appropriate initialization pattern to accommodate all of them. Table 12-1 lists the sense pin settings that determine the ISP2312 PCI-X mode.

Table 12-1. PCI Sense Pins

PCI Bus Interface Pins					PCI-X Mode
FRAME	IRDY	DEVSEL	STOP	TRDY	
1	1	1	0	0	133 MHz
1	1	1	0	1	100 MHz
1	1	1	1	0	66 MHz

Table Notes
All other settings indicate a non-PCI-X mode.

12.3 REQ64

The REQ64 pin is sampled at PCI bus reset to determine the ISP2312 PCI bus width. When REQ64 is sampled active at PCI bus reset, the ISP2312 comes up as a 64-bit device. For 64-bit PCI bus slots, the system asserts REQ64 during PCI bus reset, causing the ISP2312 to initialize as a 64-bit device.

12.4 Test Modes

The LPENB_1, LPENB_2, NVDATO, PDATA4–6, and PDATA0–1 pins are sampled at PCI bus reset to place the ISP2312 into either normal operating mode or various test modes. Table 12-2 lists the sense pin settings that determine the normal or test modes.

Table 12-2. Test Modes

LPENB_1, LPENB_2, NVDATO, PDATA4–6, PDATA0–1 (b)	Description
00000011	Normal operating mode (default)
Others	Reserved test modes

12.5 Subsystem ID Load

The ISP2312 can automatically load PCI subsystem IDs from the external NVRAM after a PCI reset. The values loaded appear in PCI configuration space in the corresponding fields. Automatic loading of the IDs can be enabled or disabled using IDENB as a power-up input sense pin. When IDENB is pulled down (default) during PCI bus reset, the automatic loading function is enabled. When IDENB is pulled up during PCI bus reset, the automatic loading function is disabled and the corresponding values in the PCI configuration space are set to zeroes.

12.6 PCI 2.2 Mode

The ISP2312 can be forced into PCI 2.2 mode depending on the state of the PDATA7 pin at PCI bus reset. When PDATA7 is sampled high at PCI bus reset, the ISP2312 powers up in PCI 2.2 mode. When PDATA7 is sampled low at PCI bus reset, the ISP2312 powers up in the PCI mode determined by the FRAME, IRDY, DEVSEL, STOP, and TRDY pins (see section 12.2).

Section 13
Layout Considerations

Layout recommendations are summarized in the following text and accompanying illustrations.

- Stack the layers so that all the signals reference a ground plane (see figure 13-1). Sandwich the power/ground plane pair close together, and do not route any traces between these layers.

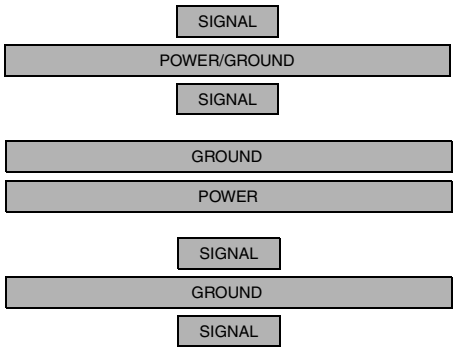


Figure 13-1. Eight-Layer Stack

- The characteristic impedance for the copper interface is 150 ohms differential. The characteristic impedance for the optical interface is 100 ohms differential.
- Route the transceiver traces as coupled microstrip. The geometry is illustrated in figure 13-2.

  Several computer programs are available to compute the differential impedance. One program is ApsimRLGC from Applied Simulation Technologies.

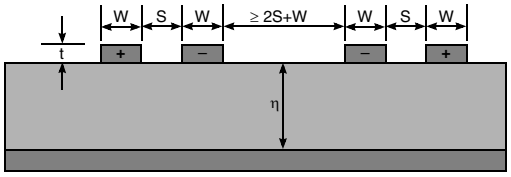


Figure 13-2. Coupled Microstrip

- Make the traces the same length within 0.1 in.
- Make the traces symmetrical.
- Route the traces over a solid plane.
- A trace must never cross a slot in an adjacent ground plane.
- Use RF vias. An RF via (a via built to pass RF frequencies without distortion) is a via with large anti-vias and no pads on the power and ground layers. This lack of pads reduces the capacitive coupling to the power and ground layers. Where possible, do not use pads on any layer other than on the signal layers.
- Use a ground via when jumping layers to provide a path for the return current.
- Follow the *10-w rule* when routing a trace near the differential pair. The 10-w rules states that the center-to-center distance between adjacent traces must be 10 times the width of the trace. In the case of the ISP2312, the concern is about flux from the adjacent trace; therefore, use the width of the adjacent trace to make the computation.
- Instead of forming a separate pad for the passives, lay one pad directly on the trace.
- Mount the DC blocker on its edge.
- Use round curves. Do not use 90 or 45 degree angles.
- The ISP2312 relies on cooling via convection from the case surface and also through the 36 VSS balls on the bottom of the package (L11–L16, M11–M16, N11–N16, P11–P16, R11–R16, T11–T16). To insure adequate cooling, these 36 pins must be connected to a large copper ground plane.

  Void the 36 VSS balls from the copper ground plane under the BGA on layer 1. Connect these balls to the solid plane on layer 1 with .010 mil traces. Make the .020 mil vias with no thermal relief. Add as many .020 mil vias with no thermal relief wherever possible under the BGA.

  Cover as much of the board surface as possible with copper connected to the internal ground plane, and make optimum thermal connections between the inner copper plane and this outer copper ground surface to assist in removing heat from the inner planes.

Section 14

Compatibility with Future ISP2312 Family Devices

The following paragraphs summarize the PCB design changes necessary to accommodate future ISP2312 devices:

- 2.5-V power supplies must be easily changed to 1.8-V power supplies. Current and voltage tolerances remain the same (see section 4.2).
- The 2.74k-ohm trim resistors must be easily replaced with 750-ohm trim resistors (see sections 10.2.1 and 10.3.1).

Section 15
Reference Schematics

15.1 Introduction

The following pages illustrate the reference schematics required to design the ISP2312 chip on a PCB.

The information provided hereunder is provided for reference purposes only, not as a manufacturing template. Reliance on the schematics is the sole responsibility of the recipient.

All information disclosed in the schematic is provided *as is*, without warranty of any kind, and QLogic hereby disclaims the implied warranties of merchantability and fitness for a particular purpose. QLogic accepts no responsibility for losses or expenses incurred as the result of the information received hereunder.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

PRELIMINARY

VERSION CHART		
DASH NO.	DESCRIPTION	REV
-01	FIBRE CHANNEL OPTICAL PCIX, ISP2312/133MHZ	00

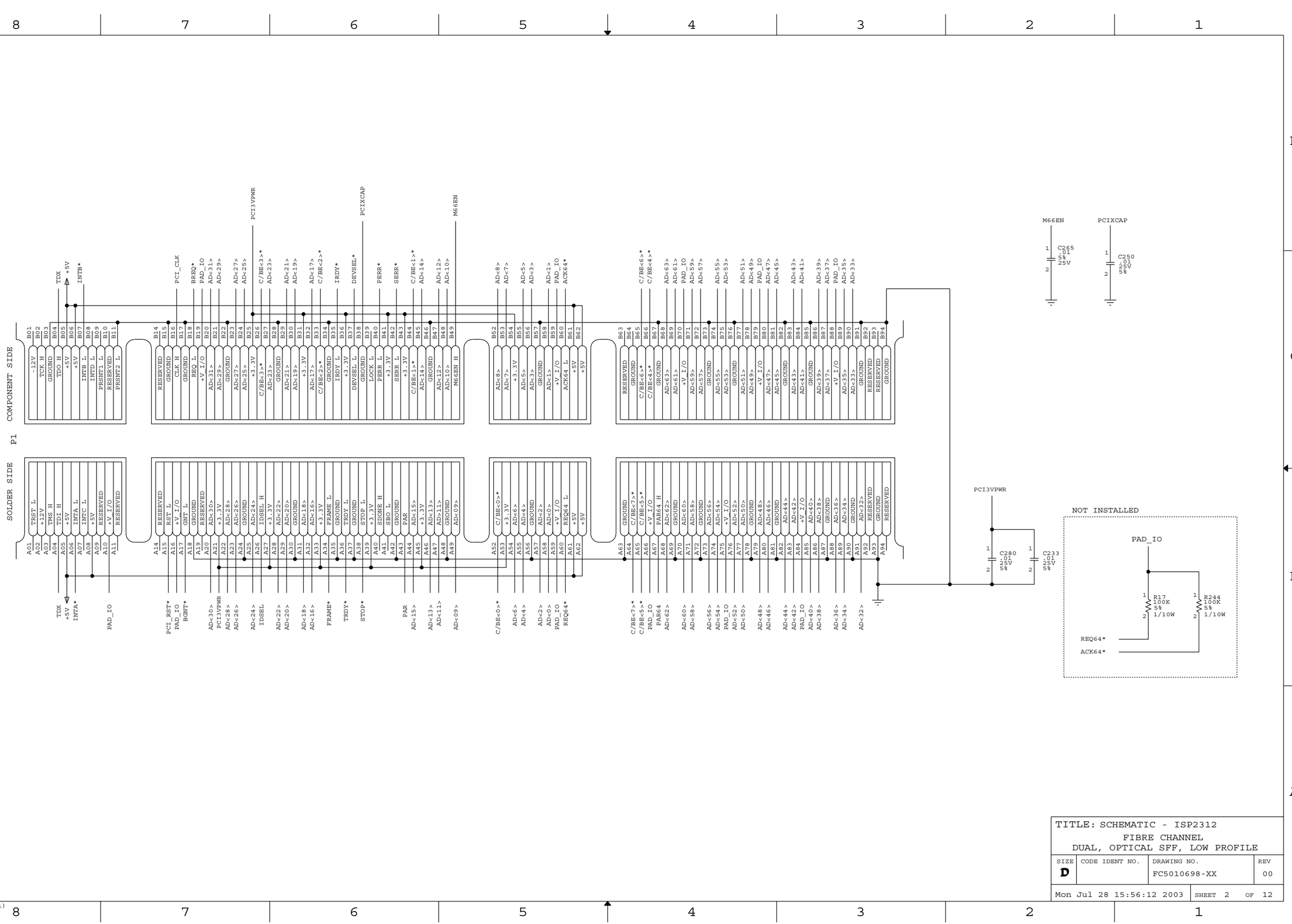
NOTES: UNLESS OTHERWISE SPECIFIED

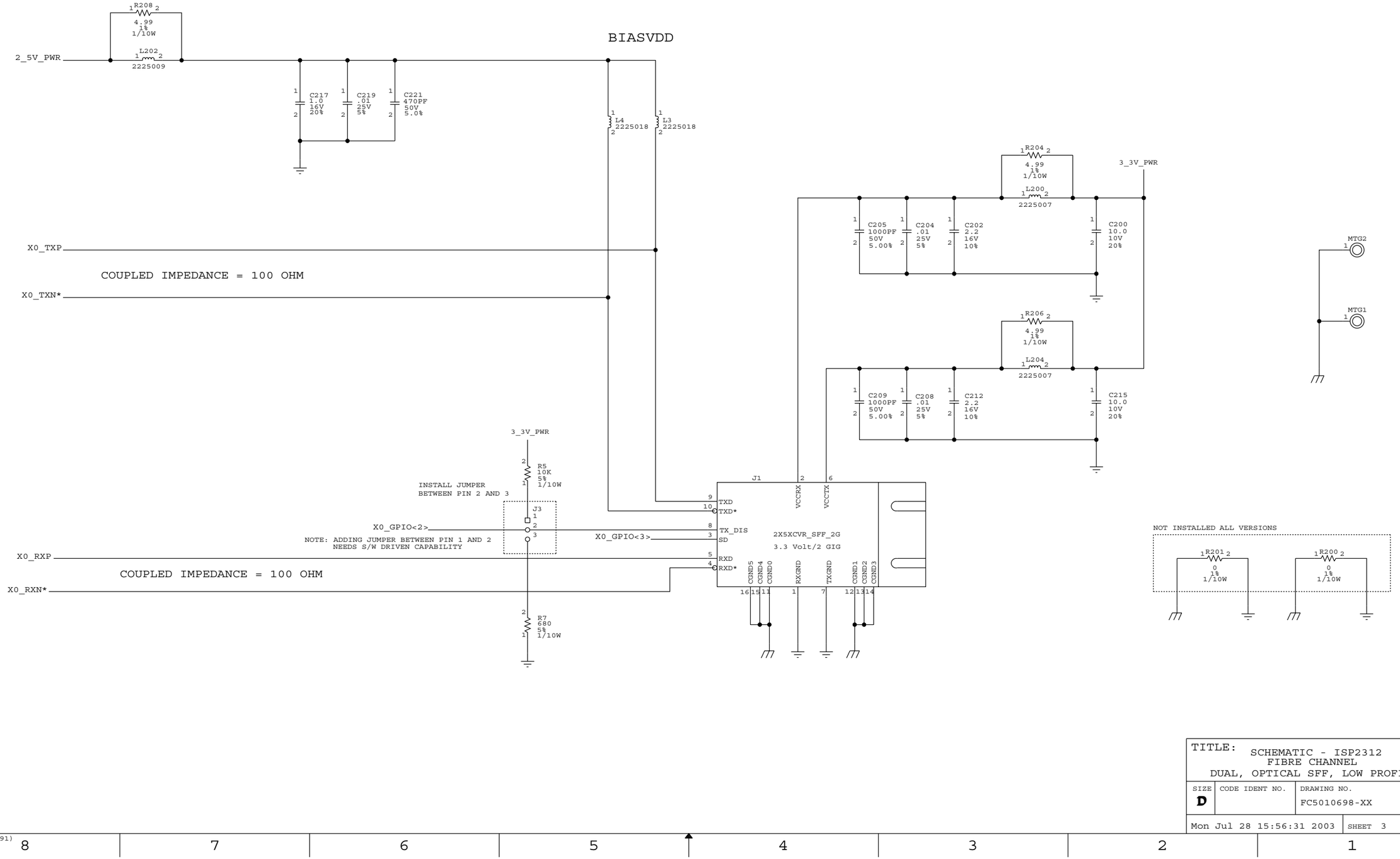
1. CAPACITORS ARE IN MICROFARADS.
2. RESISTORS ARE IN OHMS.
3. ALL VERSIONS OF THIS SCHEMATIC ARE QLOGIC'S STANDARD PRODUCT.
4. ALL CUSTOM OEMS ARE BASED ON QLOGIC'S STANDARD PRODUCT, FOR SPECIFIC DIFFERENCES SEE BILL OF MATERIALS.

DRAWN DANIEL TAO	QLOGIC CORPORATION ALISO VIEJO,CA
CHECKED	
ENGINEER DANIEL TAO	
APPROVED	TITLE: SCHEMATIC - ISP2312 FIBRE CHANNEL DUAL, OPTICAL SFF, LOW PROFILE
APPROVED	

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

Wed Jul 30 16:42:49 2003 SHEET 1 OF 12


P1
COMPONENT SIDE
SOLDER SIDE
TDX
+5V
INTB*
PCI_CLK
BREQ*
PAD_IO
PCI3VPWR
PCIXCAP
DEVSEL*
PERR*
SERR*
M66EN
IRDY*
TRDY*
STOP*
FRAME*
REQ64*
ACK64*
PCI_RST*
INTA*
BGNT*
IDSEL
PAR
PAR64
PCI3VPWR
NOT INSTALLED
C265 .01 5% 25V
C250 .01 25V 5%
C280 .01 25V 5%
C233 .01 25V 5%
R17 100K 5% 1/10W
R244 100K 5% 1/10W
TITLE: SCHEMATIC - ISP2312
FIBRE CHANNEL
DUAL, OPTICAL SFF, LOW PROFILE
SIZE D
CODE IDENT NO.
DRAWING NO. FC5010698-XX
REV 00
Mon Jul 28 15:56:12 2003
SHEET 2 OF 12
ESF1032GED (6/91)



TITLE: SCHEMATIC - ISP2312
FIBRE CHANNEL
DUAL, OPTICAL SFF, LOW PROFILE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

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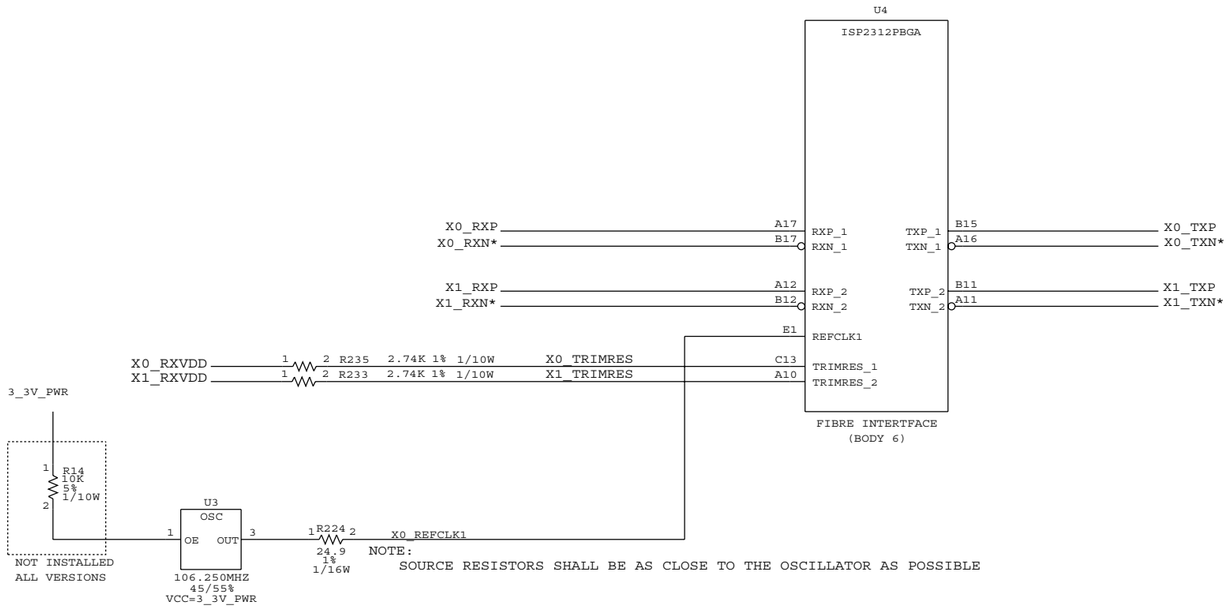
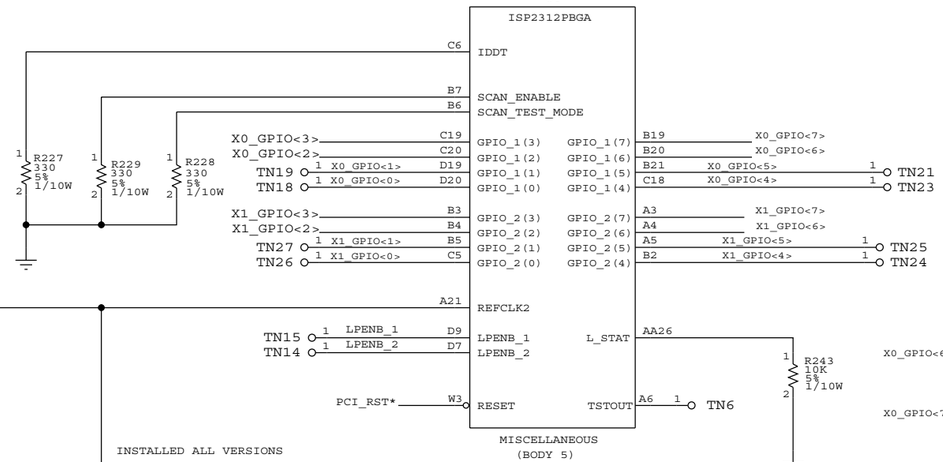
ISP2312 -6

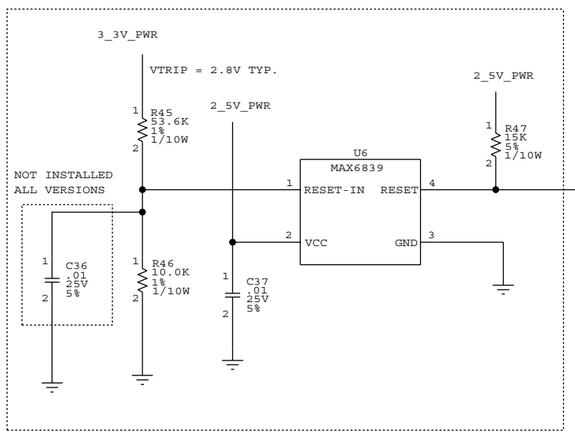


NOTE:
SOURCE RESISTORS SHALL BE AS CLOSE TO THE OSCILLATOR AS POSSIBLE

ISP2312 -5



POWER_ON_RESET CIRCUITRY



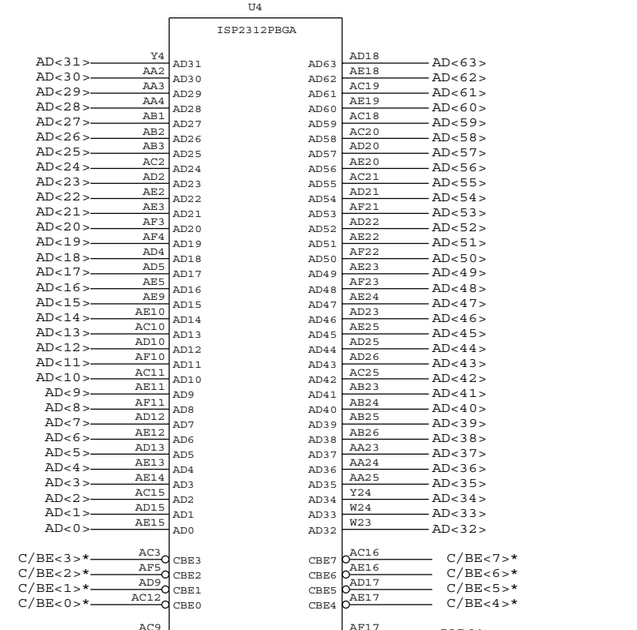
NOTE: INSTALLED FOR FUTURE VERSION

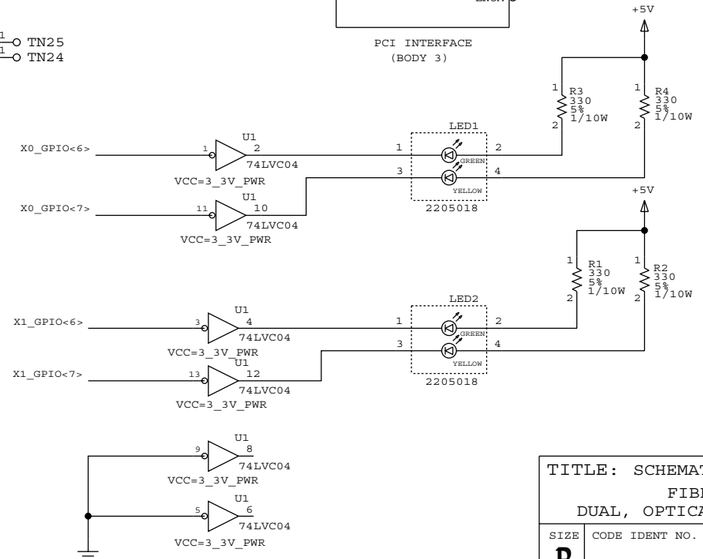
INSTALLED ALL VERSIONS

R241 330 5% 1/10W

NOTE: WHEN POR CIRCUITRY IS REQUIRED, NOT INSTALLED THIS RESISTOR

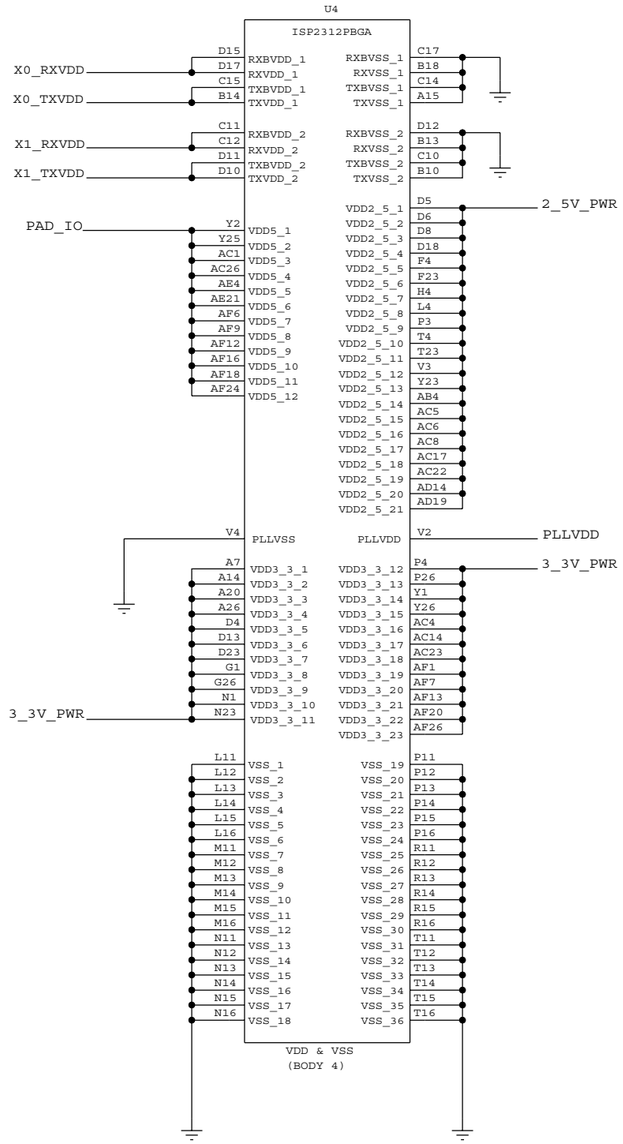
ISP2312 -3

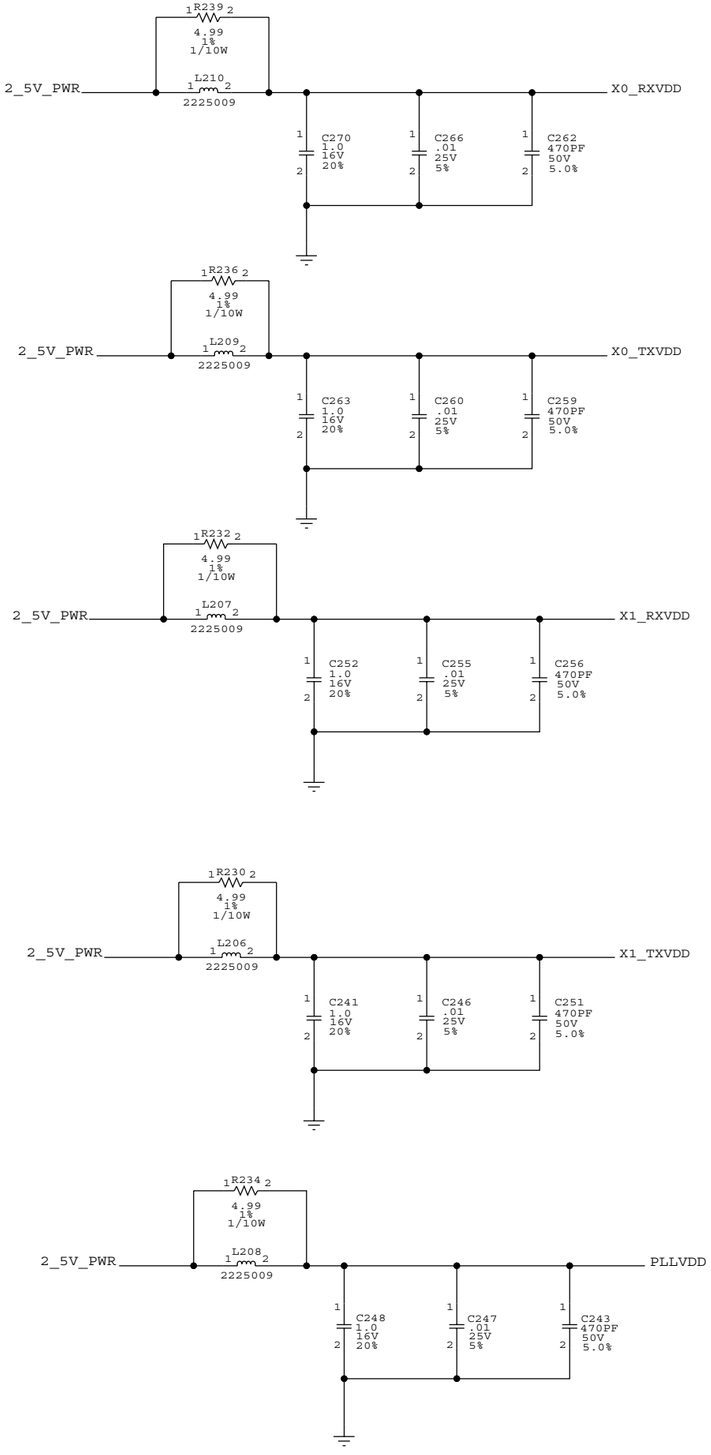




TITLE: SCHEMATIC - ISP2312 FIBRE CHANNEL DUAL, OPTICAL SFF, LOW PROFILE			
SIZE D	CODE IDENT NO.	DRAWING NO. FC5010698-XX	REV 00
Wed Jul 30 16:45:26 2003		SHEET 4 OF 12	

ISP2312 -4





TITLE: SCHEMATIC - ISP2312
FIBRE CHANNEL
DUAL, OPTICAL SFF, LOW PROFILE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

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ISP2312 -1

SSRAM

INSTALL 128K X 18 OR 256K X 18, ALL VERSIONS

U8
IDT71V3579

SSRAM SIZE
1M X 18
512K X 18
256K X 18
128K X 18

X0_RADDR<19>
X0_RADDR<18>
X0_RADDR<17>
X0_RADDR<16>

NF2 42
NF1 43
SA_16 50
SA_15 100
SA_14 99
SA_13 82
SA_12 81
SA_11 80
SA_10 49
SA_9 48
SA_8 47
SA_7 46
SA_6 45
SA_5 44
SA_4 35
SA_3 34
SA_2 33
SA_1 32
SA1 36
SA0 37

X0_RADDR<15>
X0_RADDR<14>
X0_RADDR<13>
X0_RADDR<12>
X0_RADDR<11>
X0_RADDR<10>
X0_RADDR<9>
X0_RADDR<8>
X0_RADDR<7>
X0_RADDR<6>
X0_RADDR<5>
X0_RADDR<4>
X0_RADDR<3>
X0_RADDR<2>
X0_RADDR<1>
X0_RADDR<0>

DQB8 23 X0_RDATA<15>
DQB7 22 X0_RDATA<14>
DQB6 19 X0_RDATA<13>
DQB5 18 X0_RDATA<12>
DQB4 13 X0_RDATA<11>
DQB3 12 X0_RDATA<10>
DQB2 9 X0_RDATA<9>
DQB1 8 X0_RDATA<8>
DQPB 24

DQA8 73 X0_RDATA<7>
DQA7 72 X0_RDATA<6>
DQA6 69 X0_RDATA<5>
DQA5 68 X0_RDATA<4>
DQA4 63 X0_RDATA<3>
DQA3 62 X0_RDATA<2>
DQA2 59 X0_RDATA<1>
DQA1 58 X0_RDATA<0>
DQPA 74 X0_RDPAR

3_3V_PWR
R39 10K 5% 1/10W

3_3V_PWR
R23 10K 5% 1/10W
R35 10K 5% 1/10W

BWb# 94
BWa# 93
BWE# 87
BWc# 95
BWd# 96

X0_WE* GW# 88

CE2# 92
CE2 97
CE# 98

3_3V_PWR
R33 10K 5% 1/10W
R36 330 5% 1/10W
X0_ROE* OE 86

ADV# 83
ADSP# 84
ADSC# 85

3_3V_PWR
R21 10K 5% 1/10W
R34 330 5% 1/10W
R42 330 5% 1/10W
MODE 31

X0_CLKOUT CLK 89

R258 330 5% 1/10W
ZZ 64

VDDQ 77
VDDQ 70
VDDQ 61
VDDQ 54
VDDQ 27
VDDQ 20
VDDQ 11
VDDQ 4

NC/FT# 14

NOT INSTALLED ALL VERSIONS

DNU2 39
DNU1 38

R259 0 1% 1/10W
X0_RADDR<20>
FOR 2M*18 SSRAM

NC 1
NC 2
NC 3
NC 6
NC 7
NC 16
NC 25
NC 28
NC 29
NC 30

NC 51
NC 52
NC 53
NC 56
NC 57
NC 66
NC 75
NC 78
NC 79

3_3V_PWR
R43 3.92K 1% 1/10W
R44 3.92K 1% 1/10W

PDATA<1>
PDATA<0>

3_3V_PWR
NOT INSTALLED
ALL VERSIONS
R242 10K 5% 1/10W

IDENB*
INSTALLED
ALL VERSIONS
R240 330 5% 1/10W

U4
ISP2312PBGA

X0_RDATA<15> M23 RDATA_1(15)
X0_RDATA<14> N24 RDATA_1(14)
X0_RDATA<13> P25 RDATA_1(13)
X0_RDATA<12> P24 RDATA_1(12)
X0_RDATA<11> R26 RDATA_1(11)
X0_RDATA<10> R25 RDATA_1(10)
X0_RDATA<9> R24 RDATA_1(9)
X0_RDATA<8> R23 RDATA_1(8)
X0_RDATA<7> T26 RDATA_1(7)
X0_RDATA<6> T25 RDATA_1(6)
X0_RDATA<5> T24 RDATA_1(5)
X0_RDATA<4> U26 RDATA_1(4)
X0_RDATA<3> U25 RDATA_1(3)
X0_RDATA<2> U24 RDATA_1(2)
X0_RDATA<1> U23 RDATA_1(1)
X0_RDATA<0> V25 RDATA_1(0)
X0_RDPAR M24 RDPAR_1

TN17 PDATA<9> C23 PDATA9
TN16 PDATA<8> A24 PDATA8
PDATA<7> B24 PDATA7
PDATA<6> D21 PDATA6
PDATA<5> C26 PDATA5
PDATA<4> C25 PDATA4
PDATA<3> D26 PDATA3
PDATA<2> D25 PDATA2
D24 PDATA1
B25 PDATA0

NVDATI B22 NVDATI
IDENB W25

C9 TDI
C7 TCK
B9 TMS
A9 TRST

RADDR_1(20N) E23 TN13
RADDR_1(19N) F26 TN1
RADDR_1(18N) F25 TN2

RADDR_1(20) F24 X0_RADDR<20>
RADDR_1(19) G25 X0_RADDR<19>
RADDR_1(18) G24 X0_RADDR<18>
RADDR_1(17) G23 X0_RADDR<17>
RADDR_1(16) H25 X0_RADDR<16>
RADDR_1(15) H24 X0_RADDR<15>
RADDR_1(14) H23 X0_RADDR<14>
RADDR_1(13) J26 X0_RADDR<13>
RADDR_1(12) J25 X0_RADDR<12>
RADDR_1(11) J24 X0_RADDR<11>
RADDR_1(10) J23 X0_RADDR<10>
RADDR_1(9) K26 X0_RADDR<9>
RADDR_1(8) K25 X0_RADDR<8>
RADDR_1(7) K24 X0_RADDR<7>
RADDR_1(6) K23 X0_RADDR<6>
RADDR_1(5) L26 X0_RADDR<5>
RADDR_1(4) L25 X0_RADDR<4>
RADDR_1(3) L24 X0_RADDR<3>
RADDR_1(2) L23 X0_RADDR<2>
RADDR_1(1) M26 X0_RADDR<1>
RADDR_1(0) M25 X0_RADDR<0>

FLASHOE D22 R18 24.9 FLASHOE*
FLASHCS_1 B23 X0_FLASHCS*
FLASHWR A23 R260 24.9 FLASHWR*

WE_1 V24 R22 24.9 X0_WE*
ROE_1 E24 X0_ROE*
IF_1 V23 X0_IF TN22
RISCSTB_1 E25 X0_RISCSTB TN20

NVCS C21 NVCS
NVDATO C22 NVDATO
NVCLK A22 NVCLK

TDO B8 R214 33 1% 1/10W TDO

CLKOUT_1 E26 R19 24.9 1% 1/16W X0_CLKOUT

RISC INTERFACE (1)
(BODY 1)

TDI
TCK
TMS

R211 1K 5% 1/10W
3_3V_PWR
R217 1K 5% 1/10W
R213 1K 5% 1/10W

TRST*
R218 680 5% 1/10W

NOTE:
TO DISABLE FLASH, CUT ETCH BETWEEN PINS 2 AND 3,
THEN INSTALL JUMPER BETWEEN PINS 1 AND 2.

TO RE-ENABLE FLASH, INSTALL JUMPER
BETWEEN PINS 2 AND 3.

3_3V_PWR
NOT INSTALLED
R24 10K 5% 1/10W
J7

FLASH
128KB

X0_FLASHCS*

U9

FLASHOE* 32 OE
FLASHWR* 30 CE
7 WE

X0_RADDR<16> 10 A16
X0_RADDR<15> 11 A15
X0_RADDR<14> 5 A14
X0_RADDR<13> 4 A13
X0_RADDR<12> 12 A12
X0_RADDR<11> 1 A11
X0_RADDR<10> 31 A10
X0_RADDR<9> 2 A9
X0_RADDR<8> 3 A8
X0_RADDR<7> 13 A7
X0_RADDR<6> 14 A6
X0_RADDR<5> 15 A5
X0_RADDR<4> 16 A4
X0_RADDR<3> 17 A3
X0_RADDR<2> 18 A2
X0_RADDR<1> 19 A1
X0_RADDR<0> 20 A0

DQ7 29 PDATA<7>
DQ6 28 PDATA<6>
DQ5 27 PDATA<5>
DQ4 26 PDATA<4>
DQ3 25 PDATA<3>
DQ2 23 PDATA<2>
DQ1 22 PDATA<1>
DQ0 21 PDATA<0>

29LV010B_TSOP
90NS

JTAG CONNECTOR

J5
HDR 2X5

TRST* 1 2
TDI 3 4
TDO 5 6
TMS 7 8
TCK 9 10

5001158

NOT INSTALLED ALL VERSIONS

NVRAM

4K BITS
U5
M93C66

NVCS
NVDATO
NVCLK

CS 1
DI 3
SK 2
DO 4 NVDATI
ORG 6 3_3V_PWR

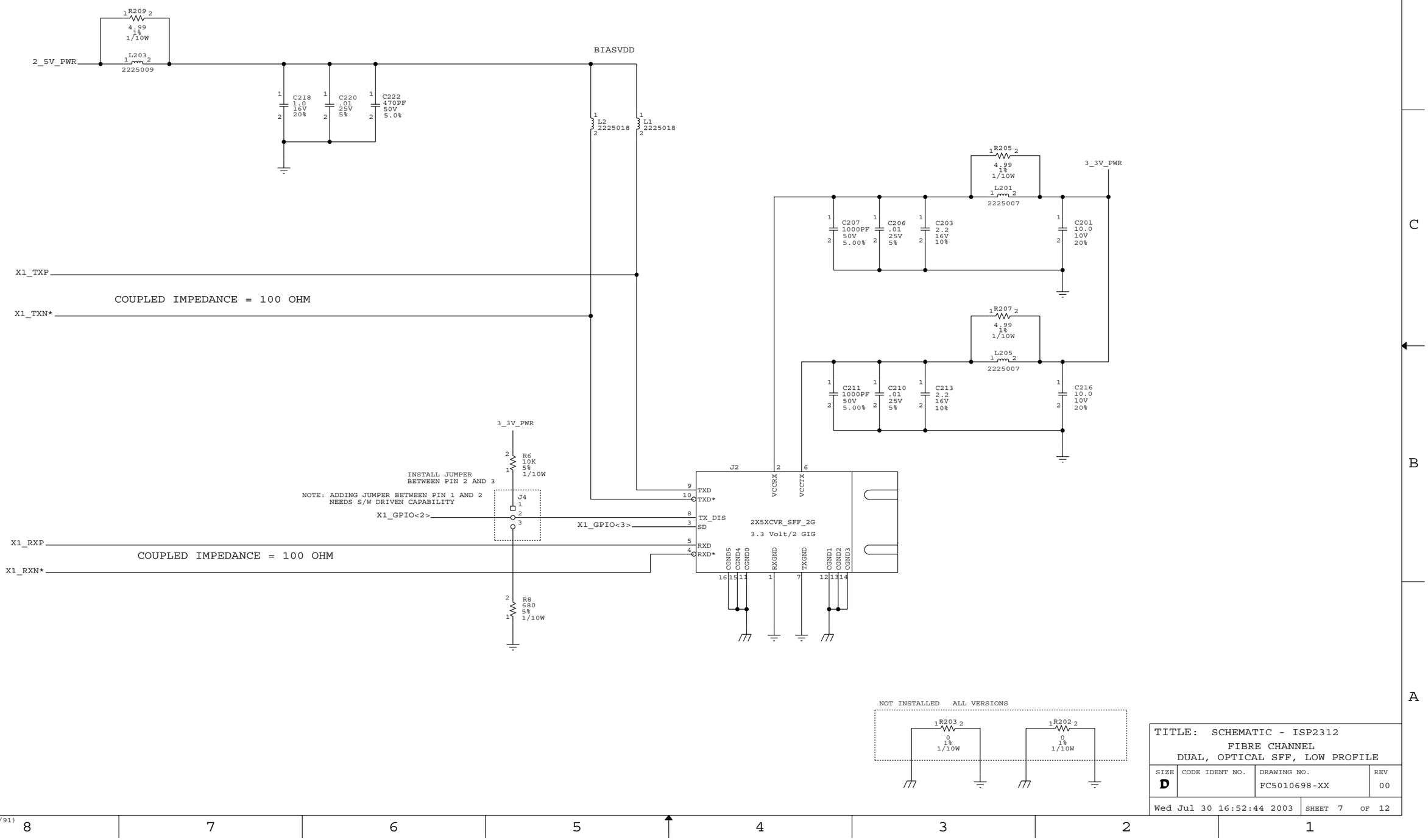
NOT INSTALLED
R15 10K 5% 1/10W

VCC=3_3V_PWR

NOT INSTALLED ALL VERSIONS
TP6

TITLE: SCHEMATIC - ISP2312 FIBRE CHANNEL DUAL, OPTICAL SFF, LOW PROFILE			
SIZE D	CODE IDENT NO.	DRAWING NO. FC5010698-XX	REV 00
Wed Jul 30 17:33:09 2003		SHEET 6 OF 12	

ESF1032GED (6/91)

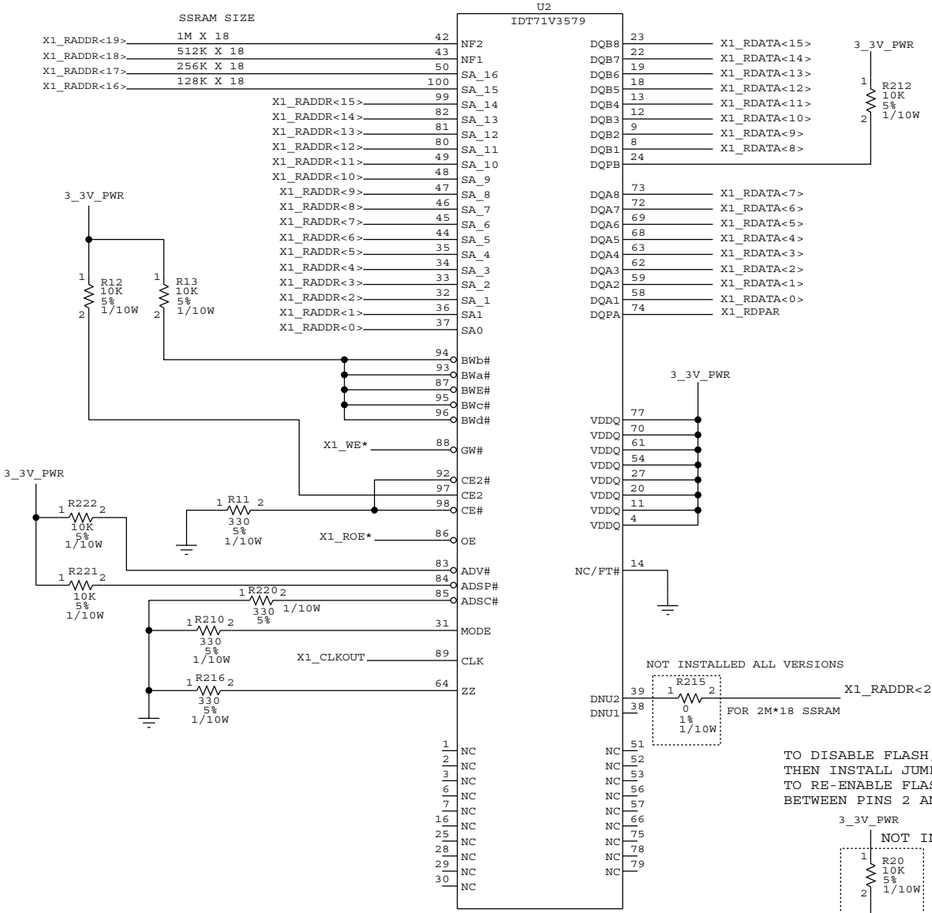


TITLE: SCHEMATIC - ISP2312 FIBRE CHANNEL DUAL, OPTICAL SFF, LOW PROFILE			
SIZE D	CODE IDENT NO.	DRAWING NO. FC5010698-XX	REV 00
Wed Jul 30 16:52:44 2003		SHEET 7 OF 12	

ESF1032GED (6/91)

SSRAM

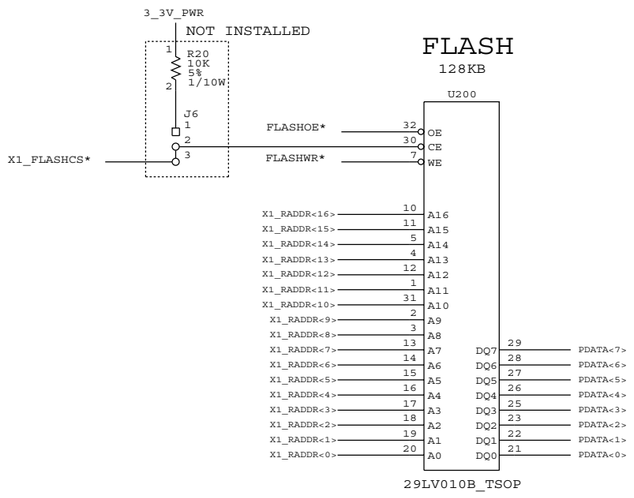
INSTALL 128K X 18 OR 256K X 18, ALL VERSIONS



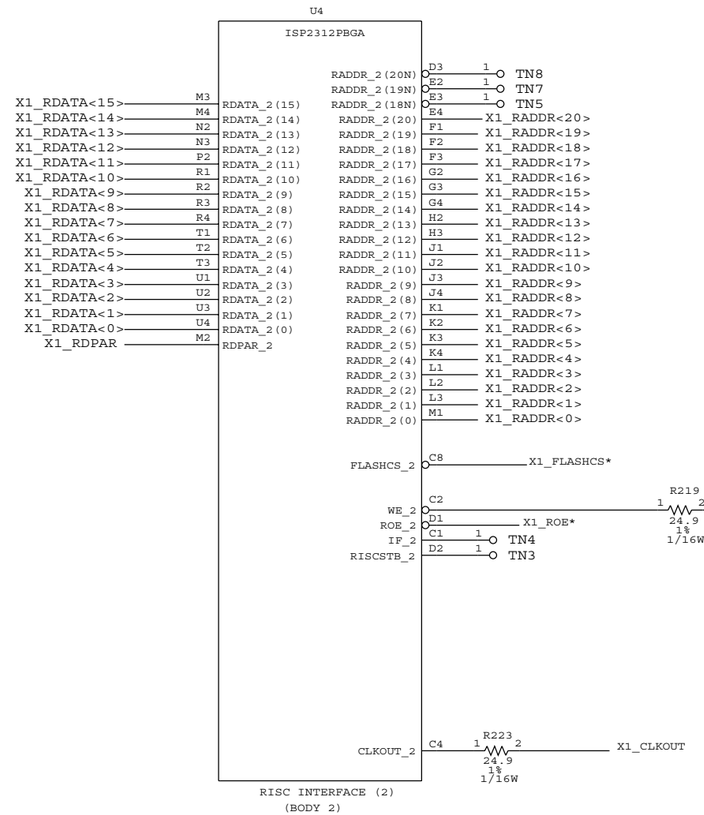
TO DISABLE FLASH, CUT ETCH BETWEEN PINS 2 AND 3,
THEN INSTALL JUMPER BETWEEN PINS 1 AND 2.
TO RE-ENABLE FLASH, INSTALL JUMPER
BETWEEN PINS 2 AND 3.

FLASH

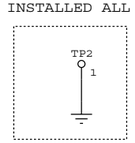
128KB



ISP2312 -2



NOT INSTALLED ALL VERSIONS



TITLE: SCHEMATIC - ISP2312 FIBRE CHANNEL DUAL, OPTICAL SFF, LOW PROFILE			
SIZE D	CODE IDENT NO.	DRAWING NO. FC5010698-XX	REV 00
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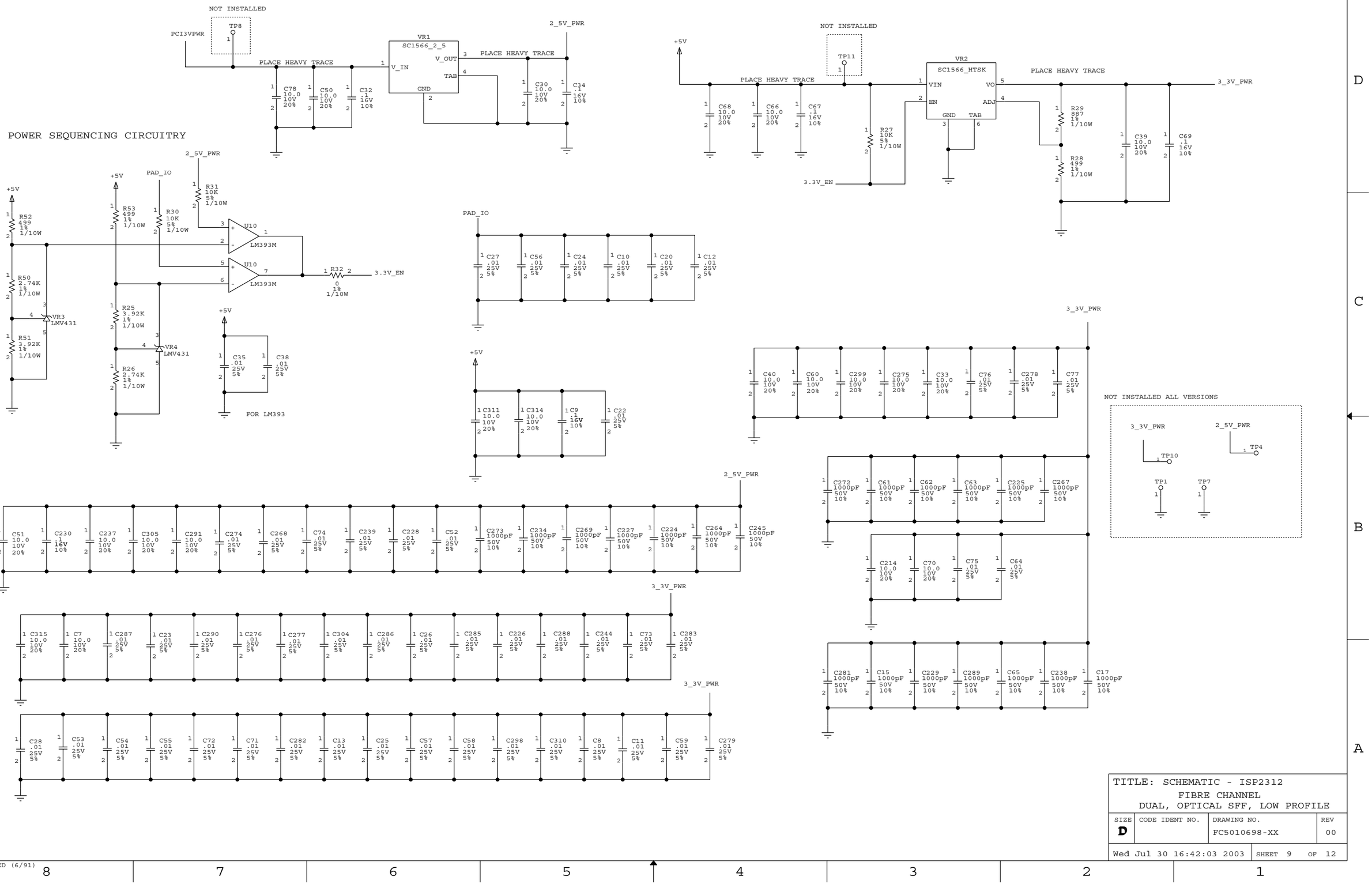

TITLE: SCHEMATIC - ISP2312
FIBRE CHANNEL
DUAL, OPTICAL SFF, LOW PROFILE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

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ESF1032GED (6/91)

*** Signal Cross-Reference for the entire design ***

2_5V_PWR	3D8< 4B7< 4B8< 5A4< 5B4< 5C4< 5C5< 5D4< 5D4< 7D8< 9B1< 9B4< 9D5< 9D7<
3.3V_EN	9C6< 9D3<
3_3V_PWR	3B5< 3C2< 4B1< 4B8< 4C8< 5B5< 5B7< 6A4< 6B5< 6C5< 6C6< 6C8< 6C8< 6D2< 6D5< 6D5< 7B5< 7C2< 8B5< 8C6< 8C8< 8D5< 8D8< 9A4< 9B2< 9B4< 9C2< 9D1<
ACK64*	4C2<> 2B2< 2C5<
AD<0>	4C3<> 2B5<
AD<1>	4C3<> 2C5<
AD<2>	4C3<> 2B5<
AD<3>	4C3<> 2C5<
AD<4>	4C3<> 2B5<
AD<5>	4C3<> 2C5<
AD<6>	4C3<> 2B5<
AD<7>	4C3<> 2C5<
AD<8>	4C3<> 2C5<
AD<9>	4C3<> 2B5<
AD<10>	4C3<> 2C5<
AD<11>	4C3<> 2B6<
AD<12>	4C3<> 2C6<
AD<13>	4C3<> 2B6<
AD<14>	4D3<> 2C6<
AD<15>	4D3<> 2B6<
AD<16>	4D3<> 2B6<
AD<17>	4D3<> 2C6<
AD<18>	4D3<> 2B6<
AD<19>	4D3<> 2C6<
AD<20>	4D3<> 2B6<
AD<21>	4D3<> 2C6<
AD<22>	4D3<> 2B6<
AD<23>	4D3<> 2C7<
AD<24>	4D3<> 2B7<
AD<25>	4D3<> 2C7<
AD<26>	4D3<> 2B7<
AD<27>	4D3<> 2C7<
AD<28>	4D3<> 2B7<
AD<29>	4D3<> 2C7<
AD<30>	4D3<> 2B7<
AD<31>	4D3<> 2C7<
AD<32>	4C2<> 2B3<
AD<33>	4C2<> 2C3<
AD<34>	4C2<> 2B3<
AD<35>	4C2<> 2C3<
AD<36>	4C2<> 2B3<
AD<37>	4C2<> 2C3<
AD<38>	4C2<> 2B3<
AD<39>	4C2<> 2C3<
AD<40>	4C2<> 2B3<
AD<41>	4C2<> 2C3<
AD<42>	4C2<> 2B3<
AD<43>	4C2<> 2C3<
AD<44>	4C2<> 2B3<
AD<45>	4C2<> 2C4<
AD<46>	4D2<> 2B4<
AD<47>	4D2<> 2C4<
AD<48>	4D2<> 2B4<
AD<49>	4D2<> 2C4<
AD<50>	4D2<> 2B4<
AD<51>	4D2<> 2C4<
AD<52>	4D2<> 2B4<
AD<53>	4D2<> 2C4<
AD<54>	4D2<> 2B4<
AD<55>	4D2<> 2C4<
AD<56>	4D2<> 2B4<
AD<57>	4D2<> 2C4<
AD<58>	4D2<> 2B4<
AD<59>	4D2<> 2C4<
AD<60>	4D2<> 2B4<
AD<61>	4D2<> 2C4<
AD<62>	4D2<> 2B4<
AD<63>	4D2<> 2C4<
BGNT*	2B7< 4B3<
BREQ*	4B2> 2C7<
C/BE*<0>	4C3<> 2B5<
C/BE*<1>	4C3<> 2C6<
C/BE*<2>	4C3<> 2C6<
C/BE*<3>	4C3<> 2C7<
C/BE*<4>	4C2<> 2C4<
C/BE*<5>	4C2<> 2B4<
C/BE*<6>	4C2<> 2C4<
C/BE*<7>	4C2<> 2B4<
DEVSEL*	4C3<> 2C6<
FLASHOE*	6C2< 6C2< 8B4<
FLASHWR*	6C2< 6C2< 8B4<
FRAME*	4C3<> 2B6<
IDENB*	6C5<
IDSEL	2B7< 4B3<
INTA*	4B2<> 2B8<
INTB*	4B2<> 2C8<
IRDY*	4B2<> 2C6<
LPENB_1	4B5<>
LPENB_2	4B5<>
M66EN	2D2< 2D5< 4C3<
NVCLK	6C3> 6A4<
NVCS	6C3<> 6A5<
NVDATI	6A3> 6C4<
NVDATO	6C3> 6A4<
PAD_IO	2B1< 2B3< 2B4< 2B4< 2B5< 2B7< 2B7< 2C3< 2C4< 2C4< 2C5< 2C7< 5C7< 9C6< 9D7<
PAR	4C3<> 2B6<
PAR64	4C2<> 2B4<
PCI3VPWR	2B2< 2B7< 2C7< 9D7<
PCIXCAP	2D2< 2D6<
PCI_CLK	2C7< 4B3<
PCI_RST*	4B5<> 2B7<
PDATA<0>	6C1<> 6C5<> 8A4<>
PDATA<1>	6C1<> 6C5<> 8A4<>
PDATA<2>	6C1<> 6C4<> 8A4<>
PDATA<3>	6C1<> 6C4<> 8A4<>
PDATA<4>	6C1<> 6C4<> 8A4<>
PDATA<5>	6C1<> 6C4<> 8A4<>
PDATA<6>	6C1<> 6C4<> 8A4<>
PDATA<7>	6C1<> 6C4<> 8A4<>
PDATA<8>	6C4<>
PDATA<9>	6C4<>
PERR*	4B2<> 2C6<
PLLVDD	5A3< 5C5<
REQ64*	4C2<> 2B2< 2B5<
SERR*	4B2<> 2C6<
STOP*	4C2<> 2B6<
TCK	6B3< 6B5<
TDI	6B3< 6B5<
TDO	6B3< 6C3<
TDX	2B8< 2C8<
TMS	6B3< 6B5<
TRDY*	4C2<> 2B6<
TRST*	6B3< 6B4<
X0_CLKOUT	6B3< 6B8<
X0_FLASHCS*	6C2> 6D2<
X0_GPIO<0>	4B5<>
X0_GPIO<1>	4B5<>
X0_GPIO<2>	4B6<> 3B6<
X0_GPIO<3>	4B6<> 3B5<
X0_GPIO<4>	4B4<>
X0_GPIO<5>	4B4<>
X0_GPIO<6>	4B4<> 4B3<
X0_GPIO<7>	4B4<> 4B3<
X0_IF	6C3<>
X0_RADDR<0>	6C3> 6C2< 6C7<
X0_RADDR<1>	6C3> 6C2< 6C7<
X0_RADDR<2>	6C3> 6C2< 6C7<
X0_RADDR<3>	6C3> 6C2< 6C7<
X0_RADDR<4>	6C3> 6C2< 6C7<
X0_RADDR<5>	6C3> 6C2< 6C7<
X0_RADDR<6>	6C3> 6C2< 6C7<
X0_RADDR<7>	6C3> 6C2< 6C7<
X0_RADDR<8>	6D3> 6C2< 6C7<
X0_RADDR<9>	6D3> 6C2< 6C7<
X0_RADDR<10>	6D3> 6C2< 6D7<
X0_RADDR<11>	6D3> 6C2< 6D7<
X0_RADDR<12>	6D3> 6C2< 6D7<
X0_RADDR<13>	6D3> 6C2< 6D7<
X0_RADDR<14>	6D3> 6C2< 6D7<
X0_RADDR<15>	6D3> 6C2< 6D7<
X0_RADDR<16>	6D3> 6C2< 6D8<
X0_RADDR<17>	6D3> 6D8<
X0_RADDR<18>	6D3> 6D8<
X0_RADDR<19>	6D3> 6D8<
X0_RADDR<20>	6D3> 6B5<
X0_RDATA<0>	6C4<> 6C6<>
X0_RDATA<1>	6C4<> 6C6<>
X0_RDATA<2>	6C6<> 6D4<>
X0_RDATA<3>	6C6<> 6D4<>
X0_RDATA<4>	6C6<> 6D4<>
X0_RDATA<5>	6C6<> 6D4<>
X0_RDATA<6>	6C6<> 6D4<>
X0_RDATA<7>	6C6<> 6D4<>
X0_RDATA<8>	6D4<> 6D6<>
X0_RDATA<9>	6D4<> 6D6<>
X0_RDATA<10>	6D4<> 6D6<>
X0_RDATA<11>	6D4<> 6D6<>
X0_RDATA<12>	6D4<> 6D6<>
X0_RDATA<13>	6D4<> 6D6<>
X0_RDATA<14>	6D4<> 6D6<>
X0_RDATA<15>	6D4<> 6D6<>
X0_RDPAR	6C4<> 6C6<>
X0_REFCLK1	4C7<
X0_RISCSTB	6C3<>
X0_ROE*	6C3> 6C7<
X0_RXN*	3B8< 4D6<
X0_RXP	3B8< 4D6<
X0_RXVDD	4C7< 5D2< 5D7<
X0_TRIMRES	4C6<
X0_TXN*	4D5> 3C8<
X0_TXP	4D5> 3C8<
X0_TXVDD	5D2< 5D7<
X0_WE*	6C2< 6C7<
X1_CLKOUT	8B1< 8B8<
X1_FLASHCS*	8C2> 8B5<
X1_GPIO<0>	4B5<>
X1_GPIO<1>	4B5<>
X1_GPIO<2>	4B6<> 7B6<
X1_GPIO<3>	4B6<> 7B5<
X1_GPIO<4>	4B4<>
X1_GPIO<5>	4B4<>
X1_GPIO<6>	4B4<> 4A3<
X1_GPIO<7>	4B4<> 4A3<
X1_RADDR<0>	8C2> 8A4< 8C7<
X1_RADDR<1>	8C2> 8A4< 8C7<
X1_RADDR<2>	8C2> 8A4< 8C7<
X1_RADDR<3>	8C2> 8A4< 8C7<
X1_RADDR<4>	8C2> 8A4< 8C7<
X1_RADDR<5>	8C2> 8A4< 8C7<
X1_RADDR<6>	8C2> 8A4< 8C7<
X1_RADDR<7>	8C2> 8A4< 8D7<
X1_RADDR<8>	8C2> 8A4< 8D7<
X1_RADDR<9>	8C2> 8A4< 8D7<
X1_RADDR<10>	8C2> 8A4< 8D7<
X1_RADDR<11>	8C2> 8A4< 8D7<
X1_RADDR<12>	8D2> 8A4< 8D7<
X1_RADDR<13>	8D2> 8A4< 8D7<
X1_RADDR<14>	8D2> 8A4< 8D7<
X1_RADDR<15>	8D2> 8A4< 8D7<
X1_RADDR<16>	8D2> 8A4< 8D7<
X1_RADDR<17>	8D2> 8D7<
X1_RADDR<18>	8D2> 8D7<
X1_RADDR<19>	8D2> 8D7<
X1_RADDR<20>	8D2> 8B5<
X1_RDATA<0>	8C3<> 8C6<>
X1_RDATA<1>	8C3<> 8C6<>
X1_RDATA<2>	8C3<> 8C6<>
X1_RDATA<3>	8C3<> 8C6<>
X1_RDATA<4>	8C3<> 8C6<>
X1_RDATA<5>	8C3<> 8D6<>
X1_RDATA<6>	8D3<> 8D6<>
X1_RDATA<7>	8D3<> 8D6<>
X1_RDATA<8>	8D3<> 8D6<>
X1_RDATA<9>	8D3<> 8D6<>
X1_RDATA<10>	8D3<> 8D6<>
X1_RDATA<11>	8D3<> 8D6<>
X1_RDATA<12>	8D3<> 8D6<>
X1_RDATA<13>	8D3<> 8D6<>
X1_RDATA<14>	8D3<> 8D6<>
X1_RDATA<15>	8D3<> 8D6<>
X1_RDPAR	8C3<> 8C6<>
X1_ROE*	8C2> 8C7<
X1_RXN*	4D6< 7B8<
X1_RXP	4D6< 7B8<
X1_RXVDD	4C7< 5C2< 5D7<
X1_TRIMRES	4C6<
X1_TXN*	4D5> 7C8<
X1_TXP	4D5> 7C8<
X1_TXVDD	5B2< 5C7<
X1_WE*	8C1< 8C7<

TITLE: SCHEMATIC - ISP2312
FIBRE CHANNL
DUAL, OPTICAL SFF, LOW PROFILE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

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8 7 6 5 4 3 2 1

*** Part Cross-Reference for the entire design ***

C7	CAP	9B8
C8	CAP	9A5
C9	CAP	9C5
C10	CAP	9C5
C11	CAP	9A5
C12	CAP	9C4
C13	CAP	9A6
C15	CAP	9A3
C17	CAP	9A2
C20	CAP	9C4
C22	CAP	9C5
C23	CAP	9B7
C24	CAP	9C5
C25	CAP	9A6
C26	CAP	9B6
C27	CAP	9C5
C28	CAP	9A8
C30	CAP	9D5
C32	CAP	9D6
C33	CAP	9C3
C34	CAP	9D5
C35	CAP	9C7
C36	CAP	4B8
C37	CAP	4B8
C38	CAP	9C7
C39	CAP	9D2
C40	CAP	9C4
C50	CAP	9D6
C51	CAP	9B8
C52	CAP	9B6
C53	CAP	9A8
C54	CAP	9A8
C55	CAP	9A7
C56	CAP	9C5
C57	CAP	9A6
C58	CAP	9A6
C59	CAP	9A4
C60	CAP	9C4
C61	CAP	9B3
C62	CAP	9B3
C63	CAP	9B3
C64	CAP	9B2
C65	CAP	9A2
C66	CAP	9D4
C67	CAP	9D4
C68	CAP	9D4
C69	CAP	9D1
C70	CAP	9B3
C71	CAP	9A7
C72	CAP	9A7
C73	CAP	9B4
C74	CAP	9B6
C75	CAP	9B3
C76	CAP	9C3
C77	CAP	9C2
C78	CAP	9D7
C200	CAP	3C2
C201	CAP	7C2
C202	CAP	3C3
C203	CAP	7C3
C204	CAP	3C3
C205	CAP	3C4
C206	CAP	7C3
C207	CAP	7C4
C208	CAP	3B3
C209	CAP	3B4
C210	CAP	7B3
C211	CAP	7B4
C212	CAP	3B3
C213	CAP	7B3
C214	CAP	9B3
C215	CAP	3B2
C216	CAP	7B2
C217	CAP	3D7
C218	CAP	7D7
C219	CAP	3D6
C220	CAP	7D6
C221	CAP	3D6
C222	CAP	7D6
C224	CAP	9B4
C225	CAP	9B2
C226	CAP	9B5
C227	CAP	9B5
C228	CAP	9B6
C229	CAP	9A3
C230	CAP	9B8
C233	CAP	2B2
C234	CAP	9B5
C237	CAP	9B8
C238	CAP	9A2
C239	CAP	9B6
C241	CAP	5B3
C243	CAP	5A3
C244	CAP	9B5
C245	CAP	9B4
C246	CAP	5B3
C247	CAP	5A3
C248	CAP	5A4
C250	CAP	2C1
C251	CAP	5B3
C252	CAP	5C3
C255	CAP	5C3
C256	CAP	5C3
C259	CAP	5C3
C260	CAP	5C3
C262	CAP	5D3
C263	CAP	5C3
C264	CAP	9B4
C265	CAP	2D2
C266	CAP	5D3
C267	CAP	9B2
C268	CAP	9B7
C269	CAP	9B5
C270	CAP	5D3
C272	CAP	9B3
C273	CAP	9B5
C274	CAP	9B7
C275	CAP	9C3
C276	CAP	9B7
C277	CAP	9B7
C278	CAP	9C2
C279	CAP	9A4
C280	CAP	2B2
C281	CAP	9A3
C282	CAP	9A7
C283	CAP	9B4
C285	CAP	9B5
C286	CAP	9B6
C287	CAP	9B8
C288	CAP	9B5
C289	CAP	9A3
C290	CAP	9B7
C291	CAP	9B7
C298	CAP	9A5
C299	CAP	9C3
C304	CAP	9B6
C305	CAP	9B7
C310	CAP	9A5
C311	CAP	9C5
C314	CAP	9C5
C315	CAP	9B8
J1	2X5XCVR_SFF_2G	3B4
J2	2X5XCVR_SFF_2G	7B4
J3	HDR1X3	3B5
J4	HDR1X3	7B5
J5	HDR2X5	6B3
J6	HDR1X3	8B5
J7	HDR1X3	6D2
L1	FERRBEAD	7C5
L2	FERRBEAD	7C5
L3	FERRBEAD	3C5
L4	FERRBEAD	3C5
L200	FERRBEAD	3C3
L201	FERRBEAD	7C3
L202	MMZ2012	3D7
L203	MMZ2012	7D7
L204	FERRBEAD	3B3
L205	FERRBEAD	7B3
L206	MMZ2012	5B4
L207	MMZ2012	5C4
L208	MMZ2012	5A4
L209	MMZ2012	5D4
L210	MMZ2012	5D4
LED1	LED_DB_HGT	4B2
LED2	LED_DB_HGT	4A2
MTG1	MTGPAD4_40	3C1
MTG2	MTGPAD4_40	3C1
P1	GFCONN22_72_22_64	2C8
R1	RESISTOR	4A2
R2	RESISTOR	4A1
R3	RESISTOR	4B2
R4	RESISTOR	4B1
R5	RESISTOR	3B5
R6	RESISTOR	7B5
R7	RESISTOR	3A5
R8	RESISTOR	7A5
R11	RESISTOR	8C7
R12	RESISTOR	8C8
R13	RESISTOR	8C7
R14	RESISTOR	4C8
R15	RESISTOR	6A5
R17	RESISTOR	2B1
R18	RESISTOR	6C3
R19	RESISTOR	6B3
R20	RESISTOR	8B5
R21	RESISTOR	6B8
R22	RESISTOR	6C3
R23	RESISTOR	6C8
R24	RESISTOR	6D2
R25	RESISTOR	9C8
R26	RESISTOR	9C8
R27	RESISTOR	9D3
R28	RESISTOR	9D2
R29	RESISTOR	9D2
R30	RESISTOR	9C7
R31	RESISTOR	9D7
R32	RESISTOR	9C6
R33	RESISTOR	6C8
R34	RESISTOR	6B7
R35	RESISTOR	6C7
R36	RESISTOR	6C7
R39	RESISTOR	6D5
R42	RESISTOR	6B7
R43	RESISTOR	6C5
R44	RESISTOR	6C5
R45	RESISTOR	4B8
R46	RESISTOR	4B8
R47	RESISTOR	4B7
R50	RESISTOR	9C8
R51	RESISTOR	9C8
R52	RESISTOR	9C8
R53	RESISTOR	9C8
R200	RESISTOR	3B1
R201	RESISTOR	3B2
R202	RESISTOR	7A2
R203	RESISTOR	7A3
R204	RESISTOR	3C3
R205	RESISTOR	7C3
R206	RESISTOR	3C3
R207	RESISTOR	7C3
R208	RESISTOR	3D7
R209	RESISTOR	7D7
R210	RESISTOR	8B7
R211	RESISTOR	6B4
R212	RESISTOR	8D5
R213	RESISTOR	6B4
R214	RESISTOR	6C3
R215	RESISTOR	8B6
R216	RESISTOR	8B7
R217	RESISTOR	6B4
R218	RESISTOR	6B4
R219	RESISTOR	8C1
R220	RESISTOR	8C7
R221	RESISTOR	8C7
R222	RESISTOR	8C7
R223	RESISTOR	8B2
R224	RESISTOR	4C7
R227	RESISTOR	4B6
R228	RESISTOR	4B6
R229	RESISTOR	4B6
R230	RESISTOR	5B4
R232	RESISTOR	5C4
R233	RESISTOR	4C7
R234	RESISTOR	5B4
R235	RESISTOR	4C7
R236	RESISTOR	5D4
R237	RESISTOR	4B1
R239	RESISTOR	5D4
R240	RESISTOR	6C5
R241	RESISTOR	4A6
R242	RESISTOR	6C5
R243	RESISTOR	4B4
R244	RESISTOR	2B1
R258	RESISTOR	6B7
R259	RESISTOR	6B6
R260	RESISTOR	6C3
TN1	TESTNODE	6D3
TN2	TESTNODE	6D3
TN3	TESTNODE	8C2
TN4	TESTNODE	8C2
TN5	TESTNODE	8D2
TN6	TESTNODE	4B4
TN7	TESTNODE	8D2
TN8	TESTNODE	8D2
TN13	TESTNODE	6D3
TN14	TESTNODE	4B6
TN15	TESTNODE	4B6
TN16	TESTNODE	6C4
TN17	TESTNODE	6C4
TN18	TESTNODE	4B6
TN19	TESTNODE	4B6
TN20	TESTNODE	6C3
TN21	TESTNODE	4B3
TN22	TESTNODE	6C3
TN23	TESTNODE	4B3
TN24	TESTNODE	4B4
TN25	TESTNODE	4B4
TN26	TESTNODE	4B6
TN27	TESTNODE	4B6
TP1	TESTPOINT	9B2
TP2	TESTPOINT	8A2
TP4	TESTPOINT	9B1
TP6	TESTPOINT	6A3
TP7	TESTPOINT	9B1
TP8	TESTPOINT	9D7
TP10	TESTPOINT	9B2
TP11	TESTPOINT	9D3
U1	74LVC04	4A3 4B3
U2	IDT71V3579	8D6
U3	OSCSG	4C7
U4	ISP2312PBGA	4C5 4D2 4D5 5D6 6D4 8D2
U5	M93C66	6A4
U6	MAX6839	4B7
U8	IDT71V3579	6D6
U9	29LV010B_TSOP	6C1
U10	LM393M	9C7
U200	29LV010B_TSOP	8B4
VR1	SC1566_2_5	9D6
VR2	SC1566_HTSK	9D3
VR3	LMV431	9C8
VR4	LMV431	9C7

TITLE: SCHEMATIC - ISP2312
FIBRE CHANNEL
DUAL, OPTICAL SFF, LOW PROFILE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

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ESF1032GED (6/91)

- SPARES LIST -
- PART SUMMARY -

29LV010B_TSOP-SMD	2105030	2
2X5XCVR_SFF_2G-TH	2095101	2
74LVC04-SMD-VCC=3_3V_PWR	2095045	1
CAP-.01,25V,5%,SMD	4105011	68
CAP-.1,16V,10%,SMD	4105023	6
CAP-1.0,16V,20%,SMD	4105024	7
CAP-10.0,10V,20%,SMD	4105018	25
CAP-1000PF,50V,10%,SMD	4105021	20
CAP-1000PF,50V,5.00%,SMD	4105016	4
CAP-2.2,16V,10%,SMD	4105017	4
CAP-470PF,50V,5.0%,SMD	4105012	7
FERRBEAD-2225007	2225007	4
FERRBEAD-2225018	2225018	4
GFCONN22_72_22_64-BASE	N/A	1
HDR1X3-STRT,OPEN	5010642	4
HDR2X5-STRT,OPEN	5001158	1
IDT71V3579-SMD	2105100	2
ISP2312PBGA-SMD,NO	2405322	1
LED_DB_HGT-2205018	2205018	2
LM393M-SMD	2095107	1
LMV431-SMD	2615014	2
M93C66-SMD-VCC=3_3V_PWR	2115063	1
MAX6839-SMD	2605012	1
MMZ2012-2225009	2225009	7
MTGPAD4_40-BASE	N/A	2
OSCSG-106.250MHZ,.01%	2505036	1
RESISTOR-0,1/10W,1%	3015006	7
RESISTOR-10.0K,1/10W,1%	3015125	1
RESISTOR-100K,1/10W,5%	3015026	2
RESISTOR-10K,1/10W,5%	3015009	22
RESISTOR-15K,1/10W,5%	3015157	1
RESISTOR-1K,1/10W,5%	3015010	3
RESISTOR-2.74K,1/10W,1%	3015073	4
RESISTOR-24.9,1/16W,1%	3015037	7
RESISTOR-3.92K,1/10W,1%	3015075	4
RESISTOR-33,1/10W,1%	3015017	1
RESISTOR-330,1/10W,5%	3015059	17
RESISTOR-4.99,1/10W,1%	3015072	11
RESISTOR-499,1/10W,1%	3015076	3
RESISTOR-53.6K,1/10W,1%	3015156	1
RESISTOR-680,1/10W,5%	3015071	3
RESISTOR-887,1/10W,1%	3015099	1
SC1566_2_5-SMD	2615019	1
SC1566_HTSK-SMD	2615023/6905086	1
TESTNODE-BASE	N/A	23
TESTPOINT-LOOP	6905037	4
TESTPOINT-STRT	6900006	4
Total		301

POWER AND GROUND LIST - 1

DESIGNATOR	PART TYPE
U1	74LVC04-SMD-VCC=3_3V_PWR
	3_3V_PWR GND
	14 7
U2	IDT71V3579-SMD
	3_3V_PWR GND
	15 5
	41 10
	65 17
	91 21
	26
	40
	55
	60
	67
	71
	76
	90
U3	OSCSG-106.250MHZ,.01%,CMOS,45/B
	3_3V_PWR GND
	4 2
U4	ISP2312PBGA-SMD,NO
	GND
	A1
	A2
	A8
	A13
	A19
	A25
	AC13
	AD3
	AD24
	AE1
	AE26
	AF2
	AF8
	AF14
	AF19
	AF25
	B1
	B26
	C3
	C24
	D14
	H1
	H26
	N4
	N26
	P1
	P23
	W1
	W26
U5	M93C66-SMD-VCC=3_3V_PWR
	3_3V_PWR GND
	8 5
U8	IDT71V3579-SMD
	3_3V_PWR GND
	15 5
	41 10
	65 17
	91 21
	26
	40
	55
	60
	67
	71
	76
	90
U9	29LV010B_TSOP-SMD
	3_3V_PWR GND
	8 24
U10	LM393M-SMD
	GND VCC
	4 8
U200	29LV010B_TSOP-SMD
	3_3V_PWR GND
	8 24

END POWER AND GROUND LIST

TITLE: SCHEMATIC - ISP2312
FIBRE CHANNEL
DUAL, OPTICAL SFF, LOW PROFILE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		FC5010698-XX	00

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Section 16
Timing

16.1
RISC Processor Timing

Table 16-1. RISC Synchronous SRAM Read Timing

Symbol	Description	Min. (ns)	Max. (ns)
tCYCLE	Read access cycle (CLKOUT_1/CLKOUT_2)	—	9.41
t_{pd}RADDR	RADDR delay from CLKOUT_1/CLKOUT_2	1.3	5.7
$t_{pd}\overline{ROE}$	$\overline{ROE}$ delay from CLKOUT_1/CLKOUT_2	1.6	4.0
t_{su}RDATA	RDATA setup write from CLKOUT_1/CLKOUT_2	1.9	—
t_hRDATA	RDATA hold write from CLKOUT_1/CLKOUT_2	0.5	—

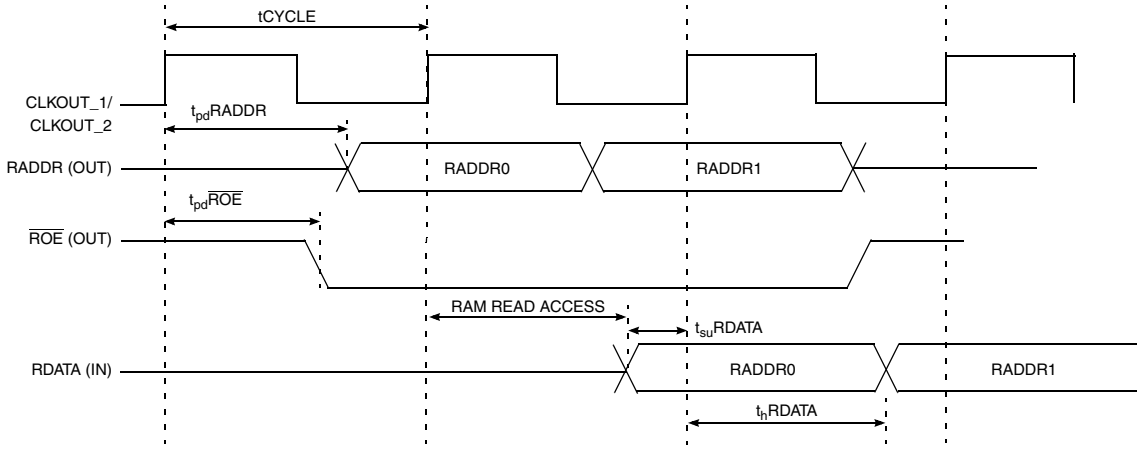

Figure 16-1. RISC Synchronous SRAM Read Timing

Table 16-2. RISC Synchronous SRAM Write Timing

Symbol	Description	Min. (ns)	Max. (ns)
tCYCLE	Write access cycle (CLKOUT_1/CLKOUT_2)	—	9.41
t_{pd}RADDR	RADDR delay from CLKOUT_1/CLKOUT_2)	1.3	5.7
t_{pd}RDPAR	RDPAR delay from CLKOUT_1/CLKOUT_2)	1.9	7.3
t_{pd}RDATA	RDATA delay from CLKOUT_1/CLKOUT_2)	1.6	5.7
$t_{pd}\overline{WE}$	$\overline{WE}$ delay from CLKOUT_1/CLKOUT_2)	1.5	4.0

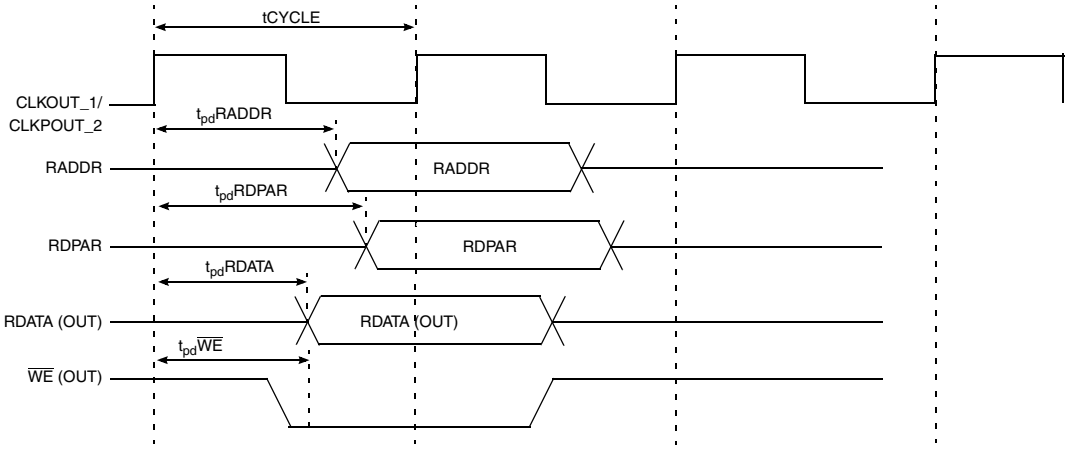

Figure 16-2. RISC Synchronous SRAM Write Timing

16.2 Flash EPROM Read Timing

Table 16-3. Flash EPROM Read Timing

Symbol	Description	Min. (ns)	Max. (ns)
t_rCYCLE	Read cycle	—	120
t_aCSD	Chip select low to data valid	—	120
t_aOED	Output enable low to data valid	—	100
t_hDA	Data hold from address change	0	—
t_hDCS	Data hold from chip select change	0	—
t_hDOE	Data hold from output enable change	0	—
t_wCS	Chip select width	—	190
t_aAD	Address valid to data valid	—	120
t_wOE	Output enable width	—	180

Table Notes
All transitions are based on a 30-pF load capacitance.

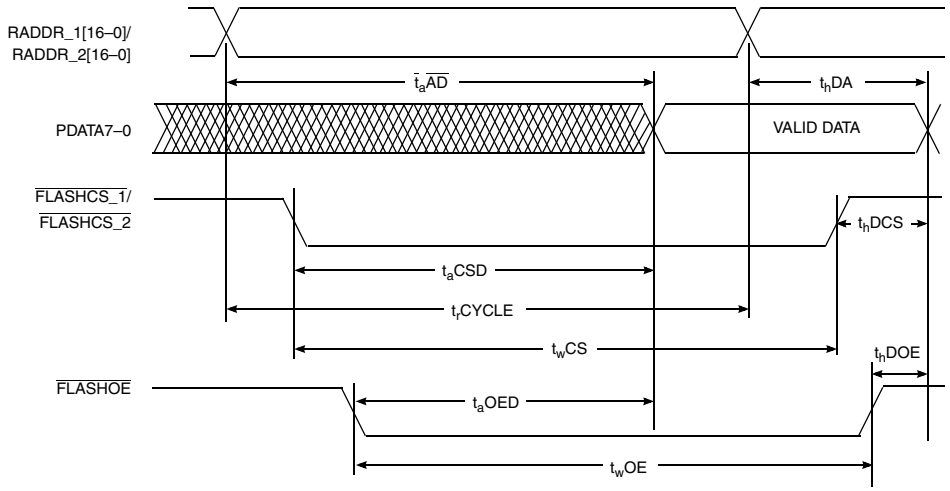

Figure 16-3. Flash EPROM Read Timing

16.3 Flash EPROM Write Timing

Table 16-4. Flash EPROM Write Timing

Symbol	Description	Min. (ns)	Max. (ns)
t_wCYCLE	Write cycle	180	—
t_sAW	Address setup to write start	10	—
t_hAW	Address hold from write end	40	—
t_sDW	Data setup from write end	120	—
t_hDW	Data hold from write end	0	—
t_sCSW	Chip select setup to write end	140	—
t_hCSW	Chip select hold from write end	40	—
t_wW	Write enable pulse width	130	—

Table Notes
All transitions are based on a 30-pF load capacitance.

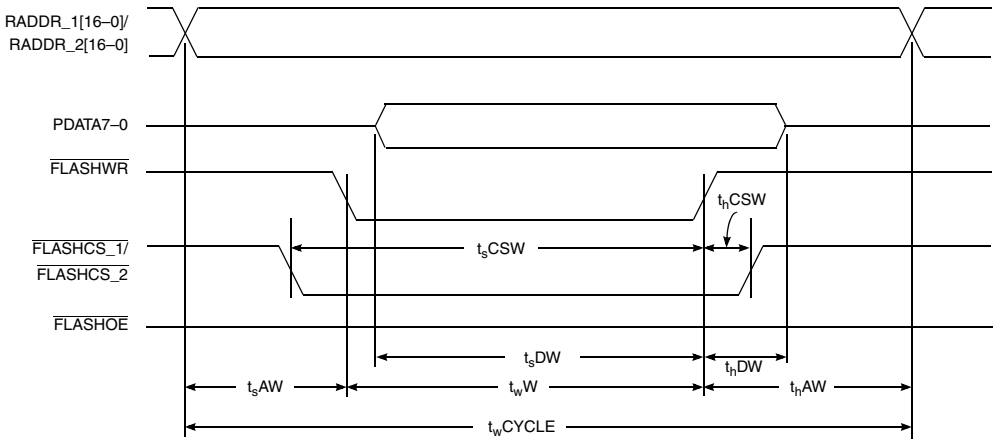

Figure 16-4. Flash EPROM Write Timing

16.4
Serial EEPROM Timing

Table 16-5. Serial EPROM Timing

Symbol	Description	Min. (µs)	Max. (µs)
t_wNVCLKH	NVCLK high time	1.0	—
t_wNVCLKL	NVCLK low time	1.0	—
t_sNVCS	NVCS setup to NVCLK	0.2	—
t_hNVCS	NVCS hold to NVCLK	0	—
t_wNVCSL	Minimum NVCS low time (for back-to-back access)	1.0	—
t_sNVDATO	NVDATO setup to NVCLK	0.4	—
t_hNVDATO	NVDATO hold to NVCLK	0.4	—
t_pNVDATIL	NVDATI 1 → 0 delay	—	2.0
t_pNVDATIH	NVDATI 0 → 1 delay	—	2.0

Table Notes
2.7 V < VCC < 4.5 V

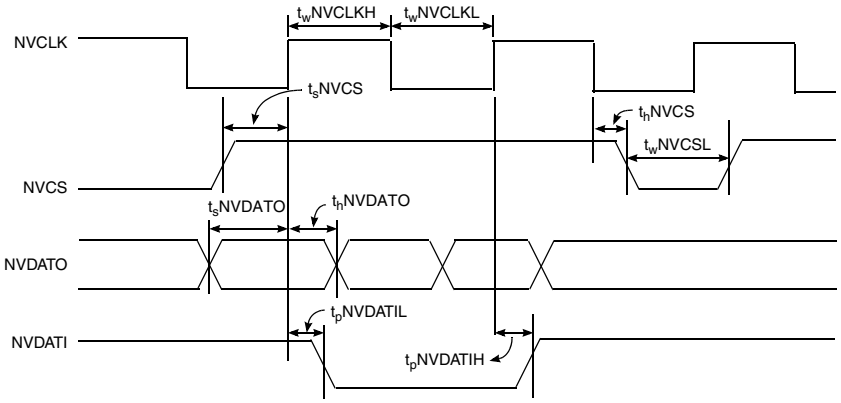

Figure 16-5. Serial EEPROM Timing

Appendix A
Register Summary

A.1 Register Table Listings

Tables A-1 through A-3 summarize the ISP2312 registers described in this document. Individual register tables are listed beginning at section A.2.

Table A-1. PCI Bus Configuration Registers

PCI Configuration Address Space	Access[a]	Register Name	Reset Value (h)
00	R	PCI Vendor ID	1077
02	R	PCI Device ID	2312
04	R/W	PCI Command	0000
06	R/W	PCI Status	Note b
08	R	PCI Revision ID and Class Code	0C040001
0C	R/W	PCI Cache Line Size	00
0D	R/W	PCI Latency Timer	Note c
0E	R	PCI Header Type	80
10	R/W	PCI I/O Base Address	00000001
14	R/W	PCI Lower Memory Base Address	Note d
18	R/W	PCI Upper Memory Base Address	00000000
2C	R	PCI Subsystem Vendor ID	Note e
2E	R	PCI Subsystem Device ID	Note e
30	R/W	PCI Expansion ROM Base Address	00000000
34	R	PCI Capability Pointer Register	00000044
3C	R/W	PCI Interrupt Line	00
3D	R	PCI Interrupt Pin	Note f
3E	R	PCI Minimum Grant	40
3F	R	PCI Maximum Latency	00
44	R	PCI Capability ID	01
45	R	PCI-X Capability Item Pointer	4C
46	R	PCI Power Management Capabilities	02
48	R/W	PCI Power Management Control/Status	00

Table A-1. PCI Bus Configuration Registers (Continued)

PCI Configuration Address Space	Access[a]	Register Name	Reset Value (h)
4A	R	PCI Power Management Bridge Support Extensions	00
4B	R	PCI Power Management Data	00
4C	R	PCI-X Capability ID	07
4D	R	PCI MSI Capability Item Pointer	54
4E	R/W	PCI-X Command	0022
50	R	PCI-X Status	0963FFF8
54	R	PCI MSI Capability ID	05
56	R/W	PCI MSI Message Control	0086
58	R/W	PCI MSI Message Address	00000000
5C	R/W	PCI MSI Message Upper Address	00000000
60	R/W	PCI MSI Message Data	0000
64	R/W	CompactPCI Hot Swap Capability	06
65	R	PCI Next Capability Item Pointer	64
66	R/W	CompactPCI Hot Swap Control and Status	80

Table Notes

[a]R = read, R/W = read/write

[b]The reset value when the ISP2312 is operating in conventional PCI bus mode is 02B0h; the reset value when the ISP2312 is operating in PCI-X bus mode is 0230h.

[c]The reset value when the ISP2312 is operating in conventional PCI bus mode is 00h; the reset value when the ISP2312 is operating in PCI-X bus mode is 40h.

[d]The reset value when the ISP2312 is operating in conventional PCI bus mode is 00000000h; the reset value when the ISP2312 is operating in PCI-X bus mode is 00000004h.

[e]The value in this register is loaded from an external serial EEPROM device at power up when the IDENB pin of the chip is tied to logic 0. Otherwise, this register is initialized to 0.

[f]This register is reset to 01h for function 0 configuration space or to 02h for function 1 configuration space.

Table A-2. PCI Bus Interface Registers

RISC[a]		PCI[b]			
I/O Address	Access[c]	Offset from Base Address (h)	Access[c]	Register Name	Reset Value (h)
—	—	000	R/W	Flash BIOS Address	0000
—	—	002	R/W	Flash BIOS Data	X
003	R	006	R/W	ISP Control/Status	X
—	—	008	R/W	ISP to PCI Interrupt Control	0000
—	—	00A	R	ISP to PCI Interrupt Status	0000
006	R/W	00C	R/W	ISP Semaphore	0000
007	R/W	00E	R/W	ISP Nonvolatile RAM Interface	0000
00E	R/W	—	—	RISC to RISC Semaphore	0000
—	—	010	R/W	Request Queue In Pointer[d]	0000
—	—	012	R	Request Queue Out Pointer[d]	0000
—	—	014	R	Response Queue In Pointer[d]	0000
—	—	016	R/W	Response Queue Out Pointer[d]	0000
—	—	018	R	RISC to Host Status Low	0000
—	—	01A	R	RISC to Host Status High	0000
—	—	01C	R/W	Host to Host Semaphore	0000
—	—	0C0	R/W	RISC Host Command and Control	0000
—	—	0CC	R	GPIOD	000
—	—	0CE	R	GPIOE	000
—	—	040–07E	W	Incoming Mailbox	X
—	—	040–07E	R	Outgoing Mailbox	X

Table Notes

[a]"—" in these columns indicates that the register is not accessible from the RISC.

[b]"—" in these columns indicates that the register is not accessible from the PCI.

[c]R = read, R/W = read/write

[d]These registers are updated/incremented by auto-DMA channel hardware (not the RISC processor) when auto-DMA is enabled. When auto-DMA is disabled (the command DMA channel fetches the IOCB and posts status), the RISC processor updates these pointers.

Table A-3. Mailbox Registers

PCI			
Offset from Base Addr (h)	Access[a]	Mailbox Number	Reset Value (h)[b]
Incoming Mailbox Registers			
040	W	0	X
042	W	1	X
044	W	2	X
046	W	3	X
048	W	4	X

Table A-3. Mailbox Registers (Continued)

PCI			
Offset from Base Addr (h)	Access[a]	Mailbox Number	Reset Value (h)[b]
04A	W	5	X
04C	W	6	X
04E	W	7	X
050	W	8	X
052	W	9	X
054	W	10	X

Table A-3. Mailbox Registers (Continued)

PCI Offset from Base Addr (h)	Access[a]	Mailbox Number	Reset Value (h)[b]
056	W	11	X
058	W	12	X
05A	W	13	X
05C	W	14	X
05E	W	15	X
060	W	16	X
062	W	17	X
064	W	18	X
066	W	19	X
068	W	20	X
06A	W	21	X
06C	W	22	X
06E	W	23	X
070	W	24	X
072	W	25	X
074	W	26	X
076	W	27	X
078	W	28	X
07A	W	29	X
07C	W	30	X
07E	W	31	X
Outgoing Mailbox Registers			
040	R	0	X
042	R	1	X
044	R	2	X
046	R	3	X
048	R	4	X
04A	R	5	X
04C	R	6	X
04E	R	7	X
050	R	8	X
052	R	9	X
054	R	10	X
056	R	11	X
058	R	12	X
05A	R	13	X

Table A-3. Mailbox Registers (Continued)

PCI Offset from Base Addr (h)	Access[a]	Mailbox Number	Reset Value (h)[b]
05C	R	14	X
05E	R	15	X
060	R	16	X
062	R	17	X
064	R	18	X
066	R	19	X
068	R	20	X
06A	R	21	X
06C	R	22	X
06E	R	23	X
070	R	24	X
072	R	25	X
074	R	26	X
076	R	27	X
078	R	28	X
07A	R	29	X
07C	R	30	X
07E	R	31	X

Table Notes
[a]R = read, W = write
[b]A rest value of X indicates an indeterminate value.

A.2
PCI Bus Configuration Registers

PCI Vendor ID Register

Configuration Address Space 00 (R)		
Bit	**Name**	**Reset (h)**
15–0	PCI Vendor ID	1077

PCI Device ID Register

Configuration Address Space 02 (R)		
Bit	**Name**	**Reset (h)**
15–0	PCI Device ID	2312

PCI Command Register

Configuration Address Space 04 (R/W)		
Bit	**Name**	**Reset (h)**
15–10	Reserved	00
9	Fast Back-to-Back Enable (R)	0
8	System Error Enable	0
7	Address/Data Stepping Enable (R)	0
6	Parity Error Response Enable	0
5	VGA Palette Snoop Enable (R)	0
4	Memory Write and Invalidate Enable	0
3	Special Cycles Enable (R)	0
2	Bus Master Enable	0
1	Memory Address Space Enable	0
0	I/O Address Space Enable	0

Table Notes
The (R) indicates a read-only bit.

PCI Status Register

Configuration Address Space 06 (R/W)		
Bit	**Name**	**Reset (h)**
15	Detected Parity Error	0
14	Signaled System Error	0
13	Received Master Abort	0
12	Received Target Abort	0
11	Signaled Target Abort	0
10–9	Device Select Timing (R)	1
8	Data Parity Detected	0
7	Fast Back-to-Back Capable (R)	Note a

PCI Status Register (Continued)

Configuration Address Space 06 (R/W)		
Bit	**Name**	**Reset (h)**
6	UDF	0
5	66 MHz Capable	1
4	Capabilities List	1
3–0	Reserved	0

Table Notes
The (R) indicates a read-only bit.
[a]This bit is set when the ISP2312 operates in conventional PCI bus mode. This bit is reset when the ISP2312 operates in PCI-X bus mode.

PCI Revision ID and Class Code Register

Configuration Address Space 08 (R)		
Bit	**Name**	**Reset (h)**
31–24	PCI Class Code	0C
23–16	PCI Subclass Code	04
15–8	Programming Model	00
7–0	PCI Revision ID	01

PCI Cache Line Size Register

Configuration Address Space 0C (R/W)		
Bit	**Name**	**Reset (h)**
7–0	PCI Cache Line Size	00

PCI Latency Timer Register

Configuration Address Space 0D (R/W)		
Bit	**Name**	**Reset (h)**
7–3	PCI Latency Timer	Note a
2–0	Reserved	0

Table Notes
[a]The conventional PCI reset value is 00h; the PCI-X reset value is 40h.

PCI Header Type Register

Configuration Address Space 0E (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Header Type	80

PCI I/O Base Address Register

Configuration Address Space 10 (R/W)		
Bit	**Name**	**Reset (h)**
31–8	PCI I/O Base Address	000000
7–0	Reserved	01

PCI Lower Memory Base Address Register

Configuration Address Space 14 (R/W)		
Bit	**Name**	**Reset (h)**
31–12	PCI Lower Memory Base Address	00000
11–0	Reserved	Note a

Table Notes

[a]The conventional PCI reset value is 000h; the PCI-X reset value is 004h.

PCI Upper Memory Base Address Register (PCI-X Mode Only)

Configuration Address Space 18 (R/W)		
Bit	**Name**	**Reset (h)**
31–0	PCI Upper Memory Base Address	00000000

PCI Subsystem Vendor ID Register

Configuration Address Space 2C (R)		
Bit	**Name**	**Reset (h)[a]**
15–0	PCI Subsystem Vendor ID	0000

Table Notes

[a]The reset value may also be accessed from the serial EEPROM.

PCI Subsystem Device ID Register

Configuration Address Space 2E (R)		
Bit	**Name**	**Reset (h)[a]**
15–0	PCI Subsystem Device ID	0000

Table Notes

[a]The reset value may also be accessed from the serial EEPROM.

PCI Expansion ROM Base Address Register

Configuration Address Space 30 (R/W)		
Bit	**Name**	**Reset (h)**
31–17	PCI Expansion ROM Base Address	0000
16–1	Reserved	0000
0	BIOS Enable	0

PCI Capability Pointer Register

Configuration Address Space 34 (R)		
Bit	**Name**	**Reset (h)**
31–8	Reserved	000000
7–0	Capability Pointer	44

PCI Interrupt Line Register

Configuration Address Space 3C (R/W)		
Bit	**Name**	**Reset (h)**
7–0	PCI Interrupt Line	00

PCI Interrupt Pin Register

Configuration Address Space 3D (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Interrupt Pin	Note a

Table Notes

[a]This register is reset to 01h for function 0 configuration space or to 02h for function 1 configuration space.

PCI Minimum Grant Register

Configuration Address Space 3E (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Minimum Grant	40

PCI Maximum Latency Register

Configuration Address Space 3F (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Maximum Latency	00

PCI Capability ID Register

Configuration Address Space 44 (R)		
Bit	**Name**	**Reset (h)**
7–0	Capability Identifier	01

PCI-X Capability Item Pointer Register

Configuration Address Space 45 (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI-X Capability Item Pointer	4C

PCI Power Management Capabilities Register

Configuration Address Space 46 (R)		
Bit	**Name**	**Reset (h)**
15–11	Power Management Event Support	00
10	D2 Support	0
9	D1 Support	0
8	Dynamic Data Support	0
7–6	Reserved	0
5	Device Specific Initialization	0
4	Auxiliary Power Source	0
3	Power Management Event Clock	0
2–0	PCI Power Management Specification Version	2

PCI Power Management Control/Status Register

Configuration Address Space 48 (R/W)		
Bit	**Name**	**Reset (h)**
15	Power Management Event Status (R)	0
14–13	Data Scale (R)	0
12–9	Data Select	0
8	Power Management Event Enable (R)	0
7–5	Reserved	0
4	Dynamic Data Power Management Enable (R)	0
3–2	Reserved	0
1–0	Power State	0

Table Notes
The (R) indicates a read-only bit.

PCI Power Management Bridge Support Extensions Register

Configuration Address Space 4A (R)		
Bit	**Name**	**Reset (h)**
7–0	Reserved	00

PCI Power Management Data Register

Configuration Address Space 4B (R)		
Bit	**Name**	**Reset (h)**
7–0	Reserved	00

PCI-X Capability ID Register

Configuration Address Space 4C (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI-X Capability ID	07

PCI MSI Capability Item Pointer Register

Configuration Address Space 4D (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI MSI Capability Item Pointer	54

PCI-X Command Register

Configuration Address Space 4E (R/W)		
Bit	**Name**	**Reset (h)**
15–7	Reserved	000
6–4	Maximum Outstanding Split Transactions	2
3–2	Maximum Memory Read Byte Count	0
1	Enable Relaxed Ordering	1
0	Data Parity Error Recoverable Enable	0

PCI-X Status Register

Configuration Address Space 50 (R/W)		
Bit	**Name**	**Reset (h)**
31–29	Reserved	0
28–26	Designed Maximum Cumulative Read Size (R)	2
25–23	Designed Maximum Outstanding Split Transactions (R)	2
22–21	Designed Maximum Memory Read Byte Count (R)	3
20	Device Complexity (R)	0
19	Unexpected Split Completion	0
18	Split Completion Discarded	0
17	133 MHz Capable (R)	1
16	64-bit Device (R)	1
15–8	Bus Number (R)	FF
7–3	Device Number (R)	1F
2–0	Function Number (R)	0

Table Notes
The (R) indicates a read-only bit.

PCI MSI Capability ID Register

Configuration Address Space 54 (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI MSI Capability ID	05

PCI MSI Message Control Register

Configuration Address Space 56 (R/W)		
Bit	**Name**	**Reset (h)**
15–8	Reserved	00
7	64-bit Address Capable (R)	1
6–4	Multiple Message Enable	0
3–1	Multiple Message Capable (R)	3
0	MSI Enable	0

Table Notes
The (R) indicates a read-only bit.

PCI MSI Message Address Register

Configuration Address Space 58 (R/W)		
Bit	**Name**	**Reset (h)**
31–2	Message Address	00000000
1–0	Reserved	0

PCI MSI Message Upper Address Register

Configuration Address Space 5C (R/W)		
Bit	**Name**	**Reset (h)**
31–0	Message Address	00000000

PCI MSI Message Data Register

Configuration Address Space 60 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Message Data	0000

CompactPCI Hot Swap Capability ID Register

Configuration Address Space 64 (R/W)		
Bit	**Name**	**Reset (h)**
7–0	CompactPCI Hot Swap Capability ID	06

PCI Next Capability Item Pointer Register

Configuration Address Space 65 (R)		
Bit	**Name**	**Reset (h)**
7–0	PCI Next Capability Item Pointer	64

CompactPCI Hot Swap Control and Status Register

Configuration Address Space 66 (R/W)		
Bit	**Name**	**Reset (h)**
7	Hot Swap Insertion Event	1
6	Hot Swap Extraction Event	0
5–4	Reserved	0
3	Hot Swap LED On/Off	0
2	Reserved	0
1	Hot Swap Event Interrupt Mask	0
0	Reserved	0

A.3 PCI Bus Interface Registers

Flash BIOS Address Register

PCI Offset from Base Address 000 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Flash BIOS Byte Address	0000

Flash BIOS Data Register

PCI Offset from Base Address 002 (R/W)		
Bit	**Name**	**Reset (h)**
15–8	Reserved	X
7–0	Flash BIOS Data	X

ISP Control/Status Register

Addresses and Access		
RISC I/O address (R)		003
PCI offset from base address (R/W)		006
Bit	**Name**	**Reset (h)**
15–14	Function Number	Note a
13	System ID Write Enable	0
12–11	Reserved	0
10–9	PCI-X Bus Mode	Note b
8	PCI 66-MHz Enable Status	Note c
7	Reserved	0
6–4	Module Select	0
3	Flash Upper 64K Bank Select	0
2	PCI 64-Bit Bus Slot (R)	Note d

ISP Control/Status Register (Continued)

Addresses and Access		
RISC I/O address (R)		003
PCI offset from base address (R/W)		006
Bit	**Name**	**Reset (h)**
1	Flash BIOS Read/Write Enable	0
0	ISP2312 Soft Reset	0

Table Notes
The (R) indicates a read-only bit.
[a]These bits are reset to 0h for function 0 or to 1h for function 1.
[b]At power-up reset, this field is 0, 1, 2, or 3.
[c]For 66-MHz PCI bus operation, this bit is 1. For 33-MHz PCI bus operation, this bit is 0.
[d]For a 64-bit PCI bus slot, this bit is 1. For a 32-bit PCI bus slot, this bit is 0.

ISP to PCI Interrupt Control Register

PCI Offset from Base Address 008 (R/W)		
Bit	**Name**	**Reset (h)**
15	Enable ISP2312 Interrupts on PCI	0
14–4	Reserved	000
3	Enable RISC Interrupt on PCI	0
2–0	Reserved	0

ISP to PCI Interrupt Status Register

PCI Offset from Base Address 00A (R)		
Bit	**Name**	**Reset (h)**
15	ISP2312 to PCI Interrupt Request	0
14–4	Reserved	000
3	RISC to PCI Interrupt Request	0
2–0	Reserved	0

ISP Semaphore Register

Access (R/W)		
RISC I/O address		006
PCI offset from base address		00C
Bit	**Name**	**Reset (h)**
15–2	Reserved	0000
1	Semaphore Status (R)	0
0	Semaphore Lock	0

Table Notes
The (R) indicates a read-only bit.

ISP Nonvolatile RAM Interface Register

Access (R/W)		
RISC I/O address		007
PCI offset from base address		00E
Bit	**Name**	**Reset (h)**
15	NVRAM Busy	0
14–4	Reserved	000
3	NVRAM Data In	X
2	NVRAM Data Out	0
1	NVRAM Chip Select	0
0	NVRAM Clock	0

RISC to RISC Semaphore Register

RISC I/O Address 00E (R/W)		
Bit	**Name**	**Reset (h)**
15–1	Reserved	0000
0	RISC Semaphore Lock/Status	0

Request Queue In-Pointer Register

PCI Offset from Base Address 010 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Request Queue In-Pointer	0000

Request Queue Out-Pointer Register

PCI Offset from Base Address 012 (R)		
Bit	**Name**	**Reset (h)**
15–0	Request Queue Out-Pointer	0000

Response Queue In-Pointer Register

PCI Offset from Base Address 014 (R)		
Bit	**Name**	**Reset (h)**
15–0	Response Queue In-Pointer	0000

Response Queue Out-Pointer Register

PCI Offset from Base Address 016 (R/W)		
Bit	**Name**	**Reset (h)**
15–0	Response Queue Out-Pointer	0000

RISC to Host Status Low and High Registers

PCI Offset from Base Address			
Access		Low	High
(R)		018	01A
Bit	**Name**		**Reset (h)**
31–16	Interrupt Information (firmware defined)		0000
15	RISC to Host Interrupt Request		0
14–10	Reserved		00
9	Semaphore Status		0
8	RISC Paused		0
7–0	Interrupt Status (firmware defined)		00

Host to Host Semaphore Register

PCI Offset from Base Address 01C (R/W)		
Bit	**Name**	**Reset (h)**
15–1	Reserved	0000
0	Host Semaphore Lock/Status	0

Host Command and Control Register

PCI Offset from Base Address 0C0 (R/W)		
Bit	**Name**	**Reset (h)**
15–12	HCCR Command Field	0
11	External Parity Error (R)	0
10	External RAM Parity Enable (R)	0
9	Frame Buffer Parity Error Mask Status (R)	0
8	Frame Buffer Parity Error (R)	0
7	Host Interrupt (R)	0
6	PCI to RISC Reset (R)	0
5	RISC Pause (R)	0
4–0	Reserved	00

Table Notes
The (R) indicates a read-only bit.

GPIOD Register

PCI Offset from Base Address 0CC (R)		
Bit	**Name**	**Reset (h)**
15–6	Reserved	000
7–0	GIOD Data In (R), GPIO Data Out (W)	X

GPIOE Register

PCI Offset from Base Address 0CE (R)		
Bit	**Name**	**Reset (h)**
15–6	Reserved	000
7–0	GPIO Enables	00

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