COMMUNICATIONS
CONTROLLERS

Marvell Solutions

MV64440, MV64441, MV64442

System Controller for MIPS Processors

Part 1 of 2: Hardware Specifications

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Document Status	
Advanced Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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Final Information	This document contains specifications on a product that is in final release. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Revision Code:	
Preliminary	Technical Publication: 0.x

Document Conventions

Note

Provides related information or information of special importance.

Caution

Indicates potential damage to hardware or software, or loss of data.

Warning

Indicates a risk of personal injury.

FEATURES

The MV64440/1/2 devices are a family of integrated system controllers designed for high-performance embedded control applications. They offer a perfect solution for most internetworking applications.

The MV64440/1/2 family includes the following devices:

MV64440 – Two 64-bit PCI-X buses, three integrated Gigabit Ethernet MAC controllers, 2 Mb integrated SRAM, four IDMA engines, and two XOR DMA engines.

MV64441 – Two 32-bit PCI-X buses and two integrated Gigabit Ethernet MAC controllers, 2 Mb integrated SRAM, four IDMA engines, and two XOR DMA engines.

MV64442 – One 64-bit PCI-X bus and one 32-bit PCI-X bus with one integrated Gigabit Ethernet MAC controllers, and four IDMA engines.

Up to 200 MHz CPU bus frequency

Selectable 2.5V, 3.3V, or HSTL CPU bus interface

Supports MIPS 64-bit bus CPUs.

- 64-bit SYSAD bus CPUs.
- Support CPU specific features:
  - Multiplexed 64-bit address/data bus
  - Supports non pedant reads with out-of-order completion
  - Supports HSTL I/O CPU bus
  - Supports L3 cache
- For details regarding a particular CPU delivered by Marvell's evaluation board, contact a Marvell Marketing or Sale representative.

CPU address remapping to the PCI

Support access, write, and caching protection to a configurable address range

Supports both Big Endian and Little Endian bus modes

Integrated 2 Mb SRAM (MV64440 and MV64441 Only)

- Low latency CPU access
- Accessible from any of the MV64440/1/2 interfaces
- Useful for descriptors and packet headers
- Packets headers retargeted to the SRAM

DDR SDRAM Controller:

- Up to 200 MHz clock frequency (400 MHz data rate) for single load
- Reduced CPU to DRAM latency
- SSTL_2 I/Os
- Supports four DRAM banks
- Supports all DDR devices densities up to 1 Gb
- Up to 8 GB address space (with 1 Gb devices)
- Supports DRAM bank interleaving between all DRAM banks (both the physical banks, and the four internal banks of the DRAM devices)
- Supports up to 16 open pages
- Supports configurable DRAM timing parameters
- Supports up to 128 byte burst per single DRAM access
- Supports DRAM self refresh

Device controller:

- 32-bit multiplexed address/data bus
- Up to 133 MHz clock frequency
- 3.3V I/Os
- Can be used as a high bandwidth interface to user specific logic
- Supports many types of standard memory devices such as FLASH, ROM, and SyncBurst SRAM
- Five chip selects with programmable timing
- Optional external wait-state support
- 8-,16-,32-bit width device support
- Support for boot ROMs

FEATURES

32-bit or 64-bit PCI/PCI-X interfaces:

- 66 MHz PCI 2.2 compliant interface
- 133 MHz PCI-X compliant interface
- 3.3V I/Os, 5V tolerant
- Supports PCI-to-PCI memory, I/O, and configuration transactions between the two PCI interfaces (MV64440 and MV64441 Only)
- Supports PCI-to-PCI-X bridging between the two PCI interfaces (MV64440 and MV64441 Only)
- The two PCI interfaces can run in asynchronous clocks to each other and to the MV64440/1/2 core clock (MV64440 and MV64441 Only)
- 32/64-bit PCI master and target operations
- Supports flexible byte swapping for interfacing Big and Little Endian PCI devices
- Supports 64-bit addressing via DAC transactions
- Configurable PCI arbiter for up to six external masters

PCI master specific features:

- Supports all PCI and PCI-X cycles
- Host to PCI bridge - translates CPU cycles to PCI Memory, I/O, or configuration cycles
- Supports DMA bursts between PCI and memory
- Supports transaction combining to unlimited PCI burst (conventional PCI)
- Supports up to four split transactions (PCI-X)

PCI target specific features:

- Supports all PCI and PCI-X cycles
- Supports programmable read pre-fetch (conventional PCI)
- Supports up to 4 KB read per single transaction (PCI-X)
- Supports unlimited burst write with zero wait states
- Supports up to four delayed reads (conventional PCI)
- Supports up to four split reads (PCI-X)
- Supports PCI access to all of the MV64440/1/2's internal registers
- PCI address remapping to local memory

PICMG CompactPCI Hot-Swap ready

"Plug and Play" support:

- Plug and Play compatible configuration registers
- PCI configuration registers that are accessible from both CPU and PCI
- Vital Product Data (VPD) support
- PCI Power Management (PMG) support
- Message Signal Interrupts (MSI) support

Messaging Unit:

- Doorbell and message interrupts between the CPU and the PCI
- I_2O support

Data integrity support between all interfaces

- Internal data path parity protection
- ECC support on DRAM and integrated SRAM, single bit correction, two bits detection
- Parity support on CPU, PCI, and device buses
- Full error reporting
- Errors propagation between the different interfaces

Gigabit Ethernet MAC Controller:

- Support 10/100/1000 Mbps
- MII, GMII, RGMII or TBI interface
- Priority queueing on receive based on DA, VLAN-Tag, IP-TOS
- Layer2/3/4 frame encapsulation detection
- Supports long frames (up to 9K) on both receive and transmit
- TCP/IP checksum on receive and transmit
- Simplified DA address filtering

Sync FIFO interfaces:

- Each of the Gigabit Ethernet ports, can be configured to work as sync FIFO interface, 8 or 16-bit wide
- Useful as high bandwidth simple interface to user specific logic
- Up to 133MHz Rx and Tx clock frequency

Two XOR DMAs (MV64440 and MV64441 Only):

- Useful for RAID application
- Supports XOR operation on up to eight source blocks
- Supports also DRAM single bit ECC errors cleanup, and CRC-32 calculation

Two Multi-Protocol Serial Controllers (MPSC):

- Each channel supports HDLC, UART, and Transparent protocols
- Bit rate of up to 55 Mb/s per channel
- Dedicated SDMAs per each channel

32 multi-purpose pins dedicated for peripheral functions and general purpose I/O

- Each pin can be configured independently
- GPIO inputs can be used to register interrupts from external devices, and generate maskable interrupts

FEATURES

Four channel Independent DMA controller:

- Chaining via linked-lists of descriptors
- Moves data from any to any interface
- DMA trigger by software or external hardware
- Early DMA termination by software or external hardware
- Supports increment or hold on both source and destination address

Interrupt controller:

- Maskable interrupts to CPU and PCI
- Drives up to four interrupt pins

Four general purpose 32-bit timer/counters

TWSI interface:

- Master/slave operation
- Serial ROM initialization

844PBGA package, 1mm ball pitch

Advanced 0.15u process

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Preface

About This Document

The *MV64440/1/2 Datasheet, Part 1 of 2: Hardware Specifications* provides a features list, overview, pin description, ball map, and electrical specifications for the MV64440, MV64441, and MV64442 devices. This document also includes information on configuration settings and physical specifications.

This document is part of a two-part datasheet set. The other part in this set is the *MV64440/1/2 Datasheet, Part 2 of 2: User Manual* (Document Number MV-S101287-00).

Related Documents

- *MV64440/1/2 Functional Errata*, Document Number MV-S300513-00
- *AN-63: Thermal Management for Selected Marvell Products*, MV-S300281-00
- *AN-155: MV6446x Transaction Ordering*, MV-S300535-00
- *TB-98: Differences Between the Discovery III and Discovery II Devices for MIPS CPUs,* Document Number MV-S101001-00
- *TB-119: MV644xx Design Considerations*, MV-S101897-00
- *ThetaJC, ThetaJA & Temperature Calculations White Paper*, MV-S700019-00

Document Conventions

Document Conventions The following name and usage conventions are used in this document:	
Product Number	This document provides information for the following devices: • MV64440 • MV64441 • MV64442 The usage of “MV64440/1/2“ means that the item or feature applies to all of the devices.
Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_AD[31:0]
Active Low Signal	An “n“ symbol at the end of a signal name indicates that the signal’s active state occurs when voltage is low. Example: CPU_PREQn

State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated in courier blue font. Example: `RegInit` Register field bits are enclosed in brackets. Example: `Field` [1:0] Register addresses are represented in hexadecimal format Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use.

Section 1. Overview

The MV64440/1/2 devices provide a single-chip high performance solution for MIPS CPU based applications, such as routers, web switches, storage applications, wireless infrastructure, and many more.

MV64440

The MV64440 device has a five bus architecture:

- A 64-bit interface to the CPU bus.
- A 64-bit interface to DDR SDRAM (Double Data Rate-Synchronous DRAM).
- A 32-bit interface to devices.
- Two 64-bit PCI/PCI-X interfaces.

Additionally, the MV64440 integrates a 2 Mb SRAM, three Gigabit Ethernet MAC controllers, two MPSCs, two XOR DMA engines, and four IDMA engines.

MV64441

The MV64440 device has a five bus architecture:

- A 64-bit interface to the CPU bus.
- A 64-bit interface to DDR SDRAM (Double Data Rate-Synchronous DRAM).
- A 32-bit interface to devices.
- Two 32-bit PCI/PCI-X interfaces.

Additionally, the MV64441 integrates a 2 Mb SRAM, two Gigabit Ethernet MAC controllers, two MPSCs, two XOR DMA engines, and four IDMA engines.

Note

There are 50 dedicated pins for the Gigabit Ethernet MACs. In GMII mode, only two Gigabit Ethernet ports can utilize these pins. In RGMII mode, the two Gigabit Ethernet ports are multiplexed on the dedicated 50 Gigabit Ethernet pins. For more information on multiplexing for the third port, see the Gigabit Ethernet Multiplexing sections.

MV64442

The MV64440 device has a five bus architecture:

- A 64-bit interface to the CPU bus.
- A 64-bit interface to DDR SDRAM (Double Data Rate-Synchronous DRAM).
- A 32-bit interface to devices.
- One 64-bit and one 32-bit PCI/PCI-X interface.

Additionally, the MV64442 device integrates one Gigabit Ethernet MAC controller, two MPSCs, and four IDMA engines.

In all of the MV64440/1/2 devices, each of the Gigabit Ethernet controllers can be configured as a synchronous (synch) FIFO interface. Each of the interfaces uses a dedicated read and write buffer. The Ethernet MAC(s) and the MPSCs have their own dedicated SDMAs to transfer Rx/Tx data and descriptors to/from memory.

All of these interfaces are connected through a crossbar fabric, enabling concurrent transactions between units. For example, the crossbar can simultaneously control:

- A Gigabit Ethernet MAC fetching a descriptor from the integrated SRAM.
- The CPU reading from the DRAM.
- The DMA moving data from the device bus to the PCI bus.

Section 2. Device Differences

This Hardware Specification provides specification details for the MV64440, MV64441, and MV64442 devices.

Table 1 outlines the various interface and feature differences between these three devices.

Note

For further information, see the specific interface section in this document.

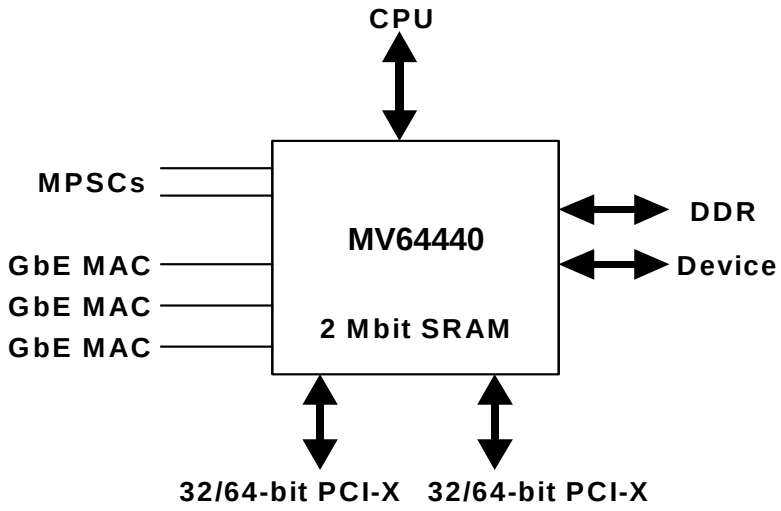
Table 1: Device Architecture

Interface	MV64440	MV64441	MV64442
CPU	• 64-bit bus with a maximum frequency of 200 MHz. • Only works as a slave interface responding to CPU transactions.		
DRAM	• Supports up to four DRAM banks (four DRAM chip selects). • 16-bit address bus (DA[13:0] and BA[1:0]) and a 72-bit data bus (DQ[63:0], CB[7:0]).		
Device	• Supports up to five banks of devices. • Each bank supports up to 512 MB of address space, resulting in total device space of 2.5 GB.		
PCI	Supports two 64-bit PCI/ PCI-X interfaces.	Supports two 32-bit PCI/ PCI-X interfaces.	Supports one 32-bit and one 64-bit PCI/PCI-X interface. Supports PCI to PCI, PCI-X to PCI-X, and PCI to PCI-X bridging between the two PCI interfaces.
Gigabit Ethernet Port	Implements three Gigabit Ethernet Ports.	Implements two Gigabit Ethernet Ports.	Implements one Gigabit Ethernet Ports. Each port can be configured to 10/100 Mbps MII interface, or to GMII/RGMII/TBI 1 Gbps interface. Each port can also be configured to act as a sync FIFO interface.
Integrated SRAM	Includes 2 Mb of integrated SRAM.		No integrated SRAM.
MPSC	Includes two MPSCs that support: • Bit oriented protocols (e.g. HDLC) • Transparent protocols • The UART (Start/Stop) mode The two MPSCs can operate independently and up to a guaranteed bit rate of 55 Mbps.		
IDMA Engine	Four independent IDMA engines.		
XOR Engine	Two XOR DMA engines, useful for Redundant Array of Independent Disks (RAID) applications		No XOR engine.

The following block diagrams also display the basic interfaces for the three different devices.

Figure 1 shows the MV64440 interfaces.

Figure 1: MV64440 Interfaces



Note

The MV64440 has three Gigabit Ethernet ports. Two ports have a dedicated interface. The third port is multiplexed on the upper pins of PCI_1 interface.

Figure 2 shows the MV64441 interfaces.

Figure 2: MV64441 Interfaces

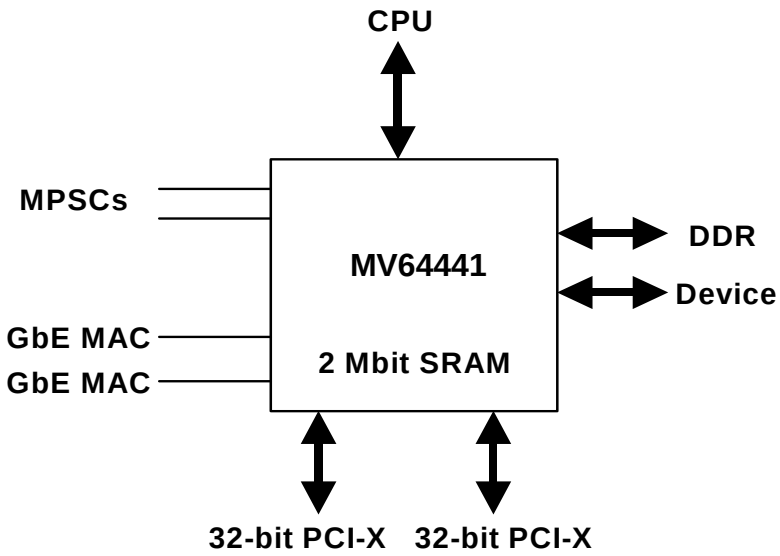
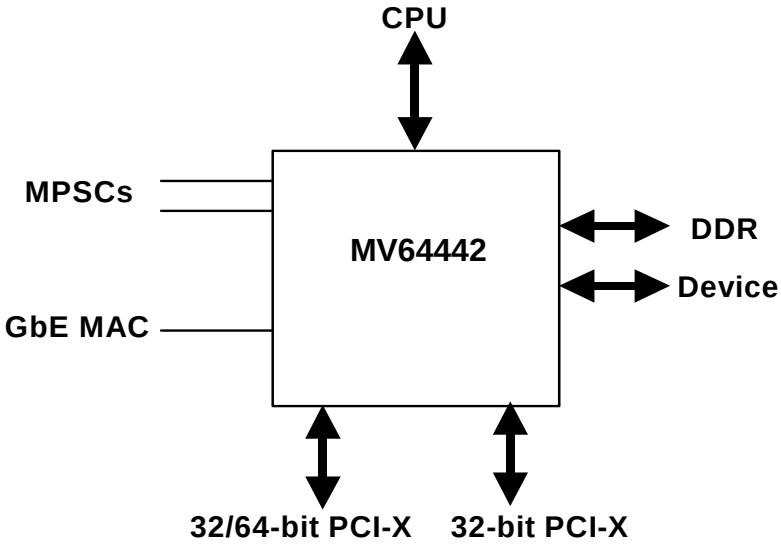


Figure 3 shows the MV64442 interfaces.

Figure 3: MV64442 Interfaces



Section 3. MV64440/1/2 versus MV64340/1/2 Differences

The MV64440/1/2 device is a new member of the Marvell® Discovery system controllers family that introduces an additional upgrade in performance and features.

Note

For full details on changes between the MV64440/1/2 and the MV64340/1/2 devices, see TB-98: *Differences Between the Discovery III and Discovery II Devices for MIPS* CPUs.

3.1 Pinout

- The MV64440/1/2 uses a new 844PBGA package (724 in MV64340/1/2). The package is still 35x35mm in size, 1mm ball pitch.
- Two separate clock inputs - SYS_CLK up to 200MHz, and TCLK up to 133MHz (the MV64340/1/2 has single SYS_CLK clock input, up to 133MHz). The CPU, DRAM, and integrated SRAM are running at SYS_CLK clock domain, while the MV64440/1/2 core is running with TCLK clock domain. The CPU access to DRAM or integrated SRAM is working entirely on the SYS_CLK domain (no clock domains crossing). Meanwhile, the CPU access to IO (e.g., PCI) or IO access to DRAM cross clock domains

Note

The MV64440/1/2 does not support running the CPU bus at lower frequency than the DRAM.

- The MV64440/1/2 supports different configurations of Gigabit Ethernet ports and FIFO interfaces, through different pinout multiplexing.

3.2 Power Supplies

- The MV64440/1/2 device is manufactured at 0.15 process. It requires 1.5V core voltage (1.8V in MV6340/1/2).
- The MV64440/1/2 Gigabit Ethernet ports, are tied to two power segments (one in MV64340/1/2), allowing one port to interface MII PHY (3.3V) while other ports interfacing RGMII PHY (2.5V/HSTL)
- Each PCI interface DLLs have separate quite power supply pins.
- The SYS_CLK clock input is also tied to a separate power segment, enabling easier clocks generation on the board.

3.3 Performance Enhancements

- CPU bus frequency up to 200 MHz (133 MHz in MV64340/1/2). MV64440/1/2 follows the MIPS CPUs road map that targets higher CPU bus speeds
- Reduced CPU-to-DRAM read latency by four cycles. To achieve reduced latency, the MV64440/1/2 implements a fast point-to-point path between the CPU interface and the DRAM controller. The entire path between the CPU and the DRAM runs with the same clock domain, up to 200 MHz.
- iSCSI CRC-32C calculation. Alternatively, it is possible to configure the XOR DMA to calculate CRC-32 on a given block.
- Gigabit Ethernet ports support RGMII (Reduced GMII) interface. In the MV64440, this new interface enables the usage of all three ports, while still having two 64-bit PCI interfaces available.
- Each of the Gigabit Ethernet ports can also work as 8/16-bit sync FIFO interface. This is a high bandwidth streaming interface (up to 133MHz), for easy point-to-point connection to user specific logic.

Note

The MV64442 only supports an 8-bit sync FIFO interface.

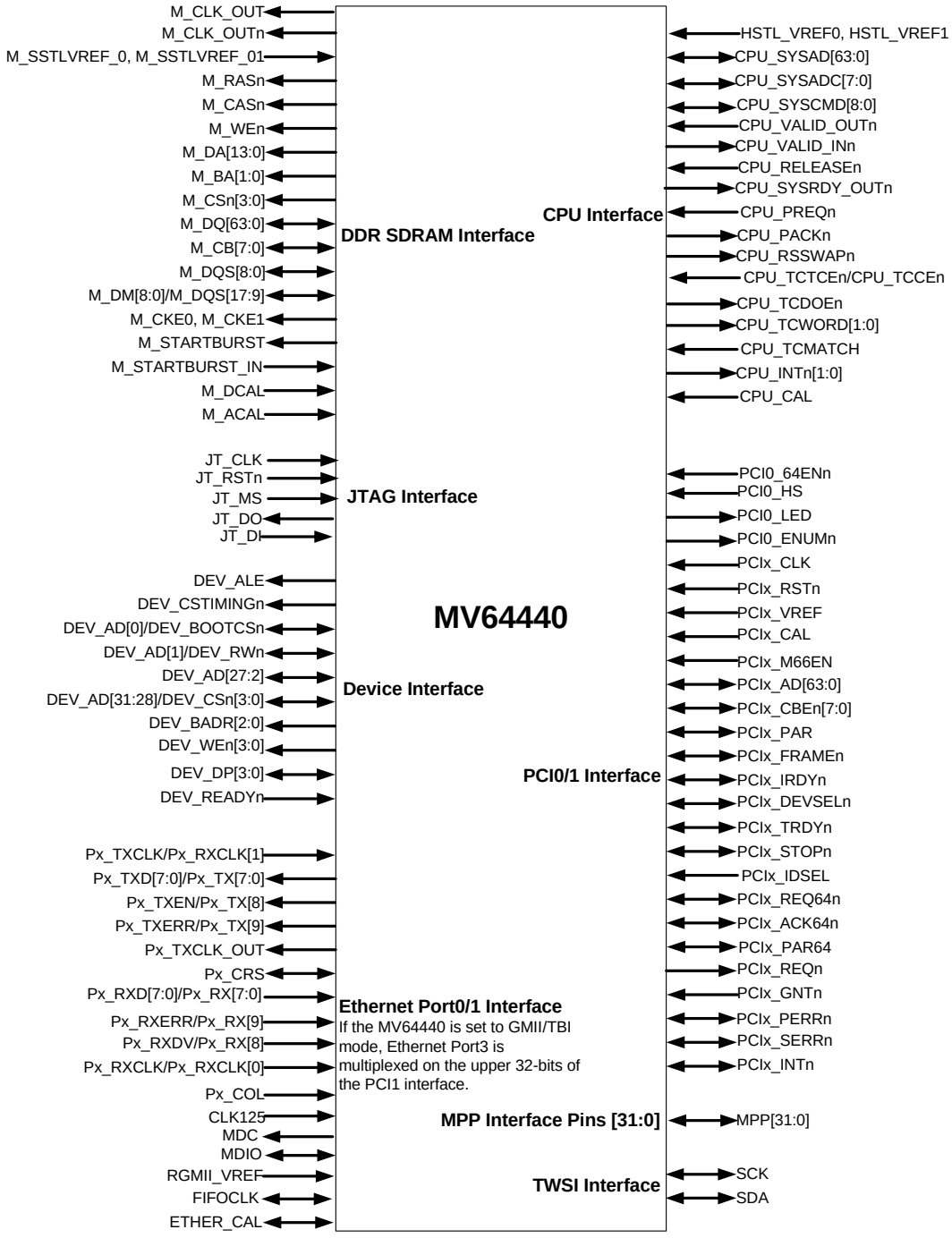
- Multiple Gigabit Ethernet port/FIFO interface configurations. The MV64440/1/2 supports different configurations of Gigabit Ethernet ports and FIFO interfaces.
- PCI ordering rules. The MV64440/1/2 fully supports PCI bridge ordering rules by hardware. See AN-84: *PCI Ordering Implementation* (Doc. No. MV-S300105-00) for full details about PCI ordering issues.

Section 4. Pin Information

4.1 MV64440/1/2 Pin Logic

See the figures in the following pages.

Figure 4: MV64440 Pin Logic



Note

In the MV64440, there are 50 dedicated pins for the Gigabit Ethernet MACs. In GMII mode, only two Gigabit Ethernet ports can utilize these pins. The third port is multiplexed on the upper bits of PCI1, which becomes a 32-bit interface. In RGMII mode, all three Gigabit Ethernet ports are multiplexed on the 50 dedicated Gigabit Ethernet pins, and PCI1 can be configured as a 64-bit interface. For more information on multiplexing for the third port, see Section 8. "MV64440 Gigabit Ethernet Pins Multiplexing" on page 66.

Figure 5: MV64441 Pin Logic

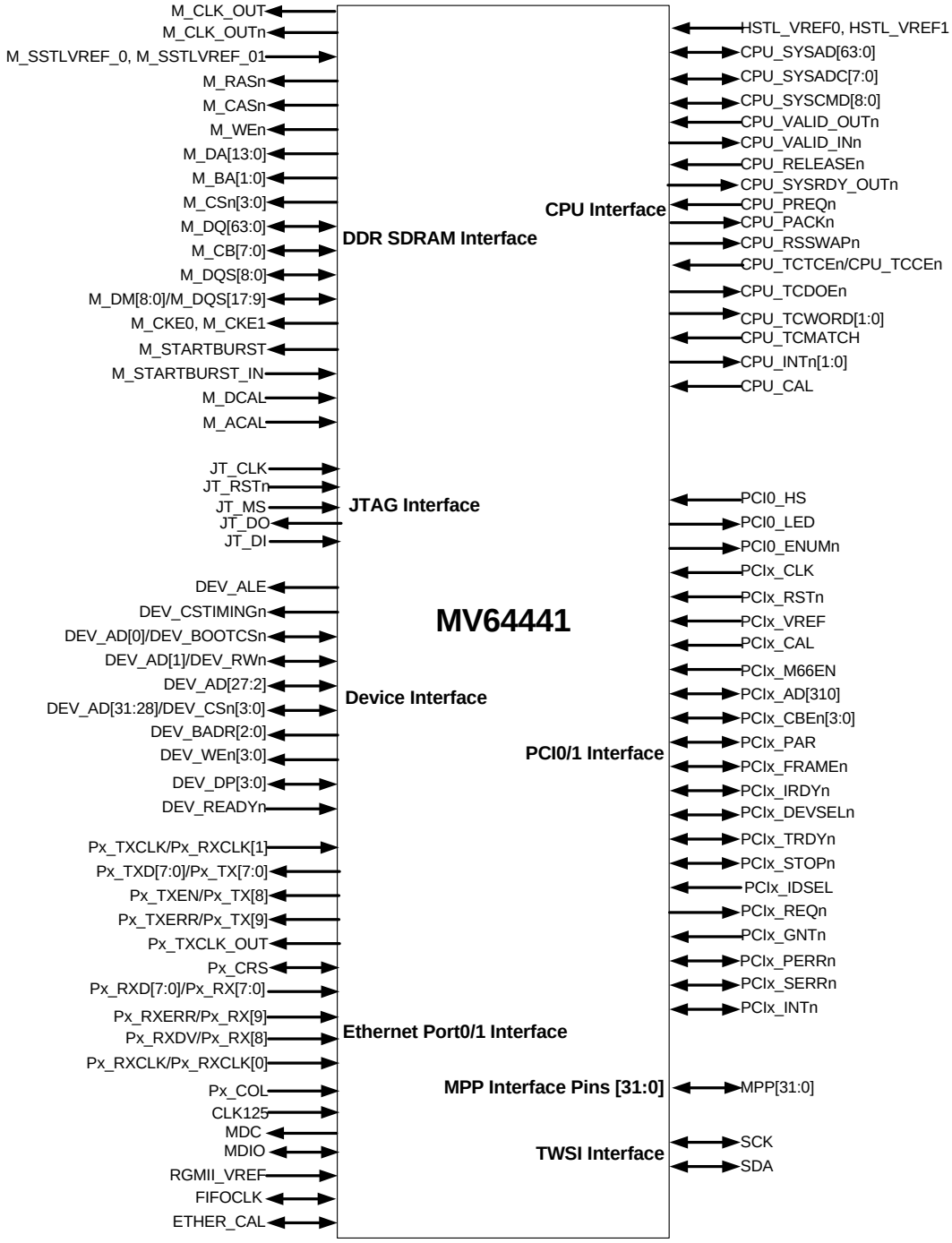
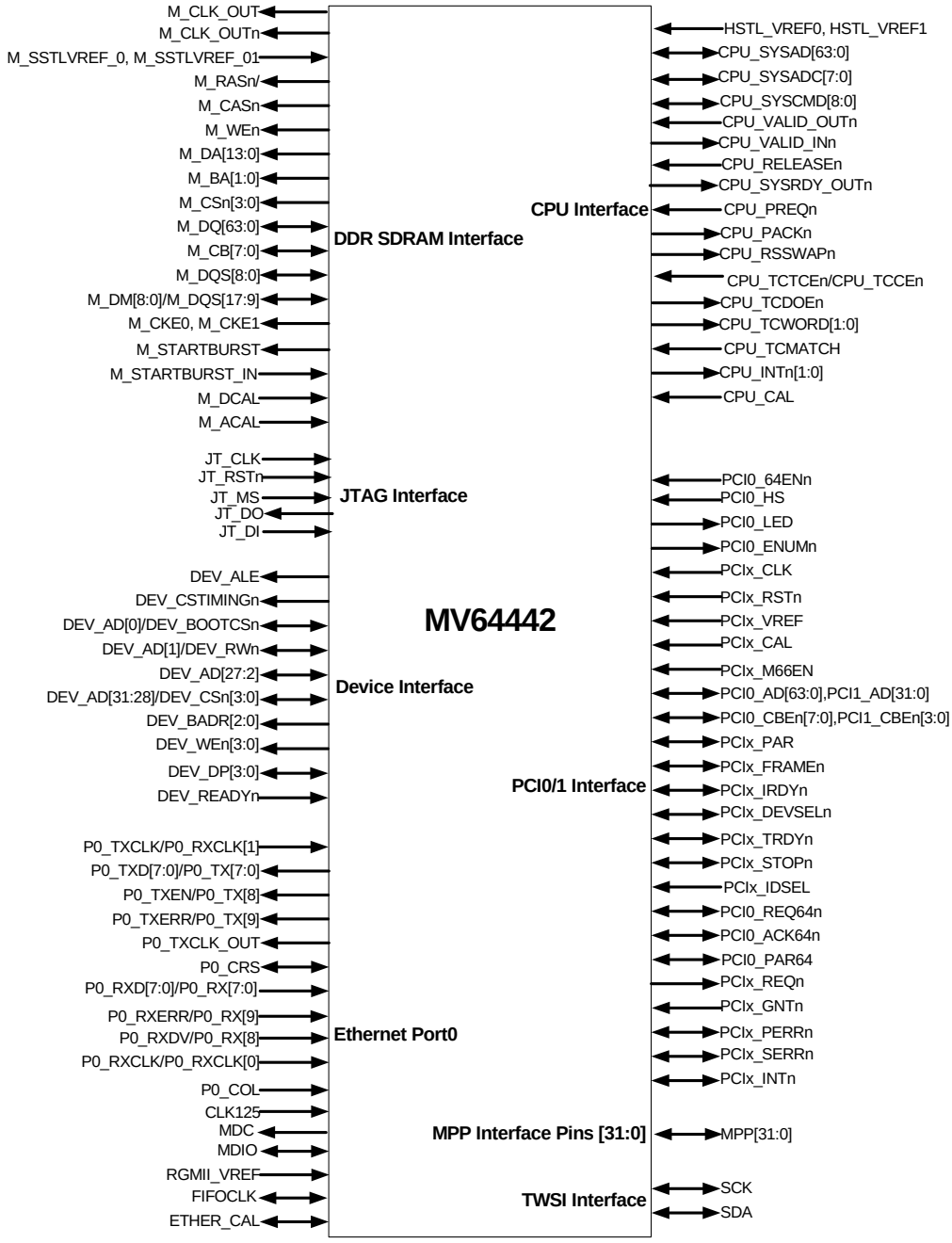


Figure 6: MV64442 Pin Logic



4.2 Pin Name Conventions

Table 2lists the conventions that apply to input/output (I/O) or just output (O) type pins.

Table 2: Pin Types

Abbreviation	Description
t/s	TriState pin.
s/t/s	Sustained TriState pin. Driven to its inactive value for one cycle before float. **NOTE:** A pull up is required to sustain the inactive value.
o/d	Open Drain pin. Allows multiple drivers simultaneously (wire-OR connection). **NOTE:** A pull up is required to sustain the inactive value.

An "n" symbol at the end of a signal name indicates that the signal's active state occurs when voltage is low.

In the signal names, the following prefixes are used to indicate a signal's specific interface.

Note

The "x" indicates the specific unit, i.e, PCI0 or PCI1.

Table 3: Interface Prefixes

Prefix	Interface
CPUx	CPU
DEV	Device
Fx	FIFO Port **NOTE:** See the Sync FIFO Interface section in the *MV64440/1/2 Datasheet User Manual.*
M	SDRAM
PCIx	PCI
Px	Gigabit Ethernet Port
Sx	Serial (MPSC) Port **NOTE:** See the Multi Protocol Serial Controllers section in the *MV64440/1/2 Datasheet User Manual*.
WD	Watchdog Timer

Table 4 shows the supply voltage levels for the various interface pins.

Table 4: Pin Supply Voltage Levels

Interface	Supply Pin Name	Supply Voltage
CPU	VDD_CPU	2.5/3.3V and HSTL
CPU	HSTL_VREF0/1	According to HSTL standard
DRAM	VDD_DRAM	2.5V
DRAM	SSTL_VREF0/1	According to SSTL2 standard
Gigabit Ethernet	V_ETH0, V_ETH1	Two power segments, each one can be powered by 3.3/2.5/HSTL **NOTE:** If working with a RGMII 3-port configuration, Port2 uses V_ETH0 segment.
Other interfaces	VDD_V33	3.3V
PCI	PCI0_VREF, PCI1_VREF	3.3V/5V in Conventional PCI (rev 2.2), 3.3V in PCI-X mode
Core	VDD_CORE	1.5V
Ground	VSS	Ground

4.3 Interface Pin Assignments

Table 5: Clock Pin Assignments

Pin Name	Type	Full Name	Description
SYS_CLK	I	System Clock	System central clock source. Used as the reference clock for the MV64440/1/2 CPU-DRAM interfaces de-skew PLL (up to 200 MHz). Same clock source is used for the CPU.
PLL0_VDDAH	I	PLL0 AVDD	PLL0 quiet 2.5V power supply.
PLL0_VSSA	I	PLL0 AVSS	PLL0 quiet VSS.
PLL1_VDDAH	I	PLL1 AVDD	PLL1 quiet 2.5V power supply.
PLL1_VSSA	I	PLL1 AVSS	PLL1 quiet VSS.
TCLK	I	Core Clock	MV64440/1/2 core clock source. Used as the reference clock for core clock de-skew PLL (up to 133MHz). Device bus and MPP signals toggle on the rising edge of TCLK.
DLL0_VDDAH	I	PCI AVDD	PCI0 DLLs quiet 1.5V power supply.
DLL0_VSSA	I	PCI AVSS	PCI0 DLLs quiet VSS.
DLL1_VDDAH	I	PCI AVDD	PCI1 DLLs quiet 1.5V power supply.

Table 5: Clock Pin Assignments

Pin Name	Type	Full Name	Description
DLL1_VSSA	I	PCI AVSS	PCI1 DLLs quiet VSS.
SYSRSTn	I	System Reset	Main reset signal of the MV64440/1/2. Resets all units to their initial state. **NOTE:** When in the reset state, all output pins are put into tristate.
VDD_CLK	I	V_{dd} Clock	Provides a reference for the clock input voltage level. Voltage level must be the same as SYS_CLK input.
Core Clock Pin Count: 13			

Table 6: CPU Interface Pin Assignments

Pin Name	Type	Full Name	Description
HSTL_VREF0	I	HSTL VREF0	Reference voltage for HSTL interface. Must be half of the voltage for the V_{dd} CPU @ HSTL mode, see EIA/JEDEC standard EIA/JESD8-6 (High speed transceiver logic (HSTL) A 1.5V output buffer supply voltage based interface standard for digital integrated circuits.)
HSTL_VREF1	I	HSTL VREF1	Reference voltage for HSTL interface. Must be half of the voltage for the V_{dd} CPU @ HSTL mode, see EIA/JEDEC standard EIA/JESD8-6 (High speed transceiver logic (HSTL) A 1.5V output buffer supply voltage based interface standard for digital integrated circuits.)
NOTE: HSTL_VREF0 [Y25] and HSTL_VREF1 [N25] are connected to the same VREF rail. Hence, the balls are connected to the same voltage, 0.75V. If not operating in HSTL mode, these pins must be connected to VDD_CPU.			
CPU_SYSAD [63:0]	t/s I/O	System Address/Data Bus	64-bit multiplexed CPU address/data bus. Driven by the CPU during address phase and write data phase. Driven by MV64440/1/2 during read response data phase. **NOTE:** These pins utilize integrated pullups
CPU_ SYSADC[7:0]	t/s I/O	System Address/Data Parity Bus	8-bit parity for the SYSAD bus. Driven by CPU during write data phase. Driven by MV64440/1/2 during read response data phase. **NOTE:** These pins utilize integrated pullups.
CPU_ SYSCMD[8:0]	t/s I/O	System Command/Data Identifier Bus	9-bit multiplexed CPU command/data identifier bus. System Command driven by the CPU during address phase. Data identifier driven by the CPU during write data phase and by the MV64440/1/2 during read response data phase.
CPU_VALID_ OUTn	I	Valid Output	The CPU signals that it is driving valid address/data on the CPU_SYSAD bus and valid command/data identifier on the CPU_SYSCMD bus.

Table 6: CPU Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
CPU_ RELEASEn	I	Release	The CPU signals that it has released the CPU_SYSAD and the CPU_SYSCMD buses after completion of a read request.
CPU_VALID_ INn	t/s O	Valid Input	The MV64440/1/2 signals that it is driving valid read data on the CPU_SYSAD bus and a valid data identifier on the CPU_SYSCMD bus.
CPU_ SYSRDY_ OUTn	t/s O	Read/Write Ready Output	The MV64440/1/2 signals that it can accept a CPU read or write request. **NOTE:** Must be connected to both RdRdyn and WrRdyn CPU input pins.
CPU_PREQn	I	Processor Request	CPU requests from the MV64440/1/2 for SYSAD bus master-ship.
CPU_PACKn	t/s O	Processor Acknowledge	The MV64440/1/2 signals that it releases the SYSAD bus in response to CPU_PREQn.
CPU_RS SWAPn	t/s O	Read Response Swap	The MV64440/1/2 signals that it is returning read data to the CPU out of order.
CPU_TCTCEn /CPU_TCCEn	I	L3 Cache Tag RAM Chip Enable	In normal R7000 L3 cache mode, CPU L3 cache controller signals that it is accessing L3 cache tag SRAM. **NOTE:** If there is no L3 cache, pull up to VDD_CPU.
		L3 RAM Chip Enable	In R7000C EZ cache mode, CPU L3 cache controller signals that it is accessing L3 SRAM (SRAM contains both data and tags).
CPU_TCDOEn	t/s O	L3 Cache Data RAM Output Enable	In normal R7000 L3 cache mode, in case of a cache hit, the MV64440/1/2 enables L3 data SRAM drive read data on SYSAD.
		L3 Cache RAM Output Enable	In R7000C EZ cache mode, the MV64440/1/2 enables L3 SRAM drive the tag on the CPU_SYSAD bus two cycles after CPU issue cycle, and in case of cache hit, it also enables L3 SRAM to drive read data on CPU_SYSAD.
CPU_ TCWORD[1:0]	t/s O	Ternary Cache Word Index	Determines correct L3 double-word index. Driven by the MV64440/1/2 in case of a CPU block read miss (driven by CPU L3 cache controller in case of L3 hit).

Table 6: CPU Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
CPU_ TCMATCH	I	Ternary Cache Tag Match	Asserted by tag RAM on L3 cache tag match. **NOTE:** If there is no L3 cache, or when working in EZCache mode, tie to VSS. If using the SR71000 CPU, CPU_TCMATCH is not asserted by tag RAM. Instead, the SR71000 asserts CPU_TCMATCH.
CPU_INTn [1:0]	t/s O	CPU Interrupts	Level sensitive interrupts driven by the MV64440/1/2 to the CPU.
CPU_CAL	I	CPU Calibration	Allows control of the CPU output buffers' strength. Connect to VDD_CPU through a resistor. The resistor size determines the drive strength of the output buffer. **NOTE:** See *TB-119 MV644xx Design Considerations* for the recommended values of the calibration resistors.
CPU Interface Pin Count: 101			

Table 7: PCI Bus 0 Interface Pin Assignments

Pin Name	Type	Full Name	Description
PCI0_CLK	I	PCI_0 Clock	PCI bus clock. Up to 133 MHz in PCI-X mode and up to 66MHz in conventional PCI mode. It is completely independent of PCI1_CLK, and SYS_CLK.
PCI0_VREF	I	PCI_0 VREF	PCI reference input voltage (3.3V or 5V).
PCI0_CAL	I	PCI_0 Calibration	Allows control of the PCI output buffers' strength. Connect to VDD through a resistor. The resistor size determines the drive strength of the output buffer. **NOTE:** See *TB-119 MV644xx Design Considerations* for the recommended values of the calibration resistors.
PCI0_RSTn	I	PCI_0 Reset	Dedicated reset signal for PCI_0 interface. **NOTE:** Does not affect PCI_1 interface or any other MV64440/1/2 unit. When in the reset state, all PCI_0 output pins are put into tristate and all open drain signals are floated.
PCI0_M66EN	I	PCI_0 66MHz Enable	The MV64440/1/2 samples PCI0_M66EN on reset de-assertion, in order to determine if it is connected to a 66MHz bus. If PCI0_M66EN is sampled 1, the internal PCI interface DLL is enabled. **NOTE:** Only relevant to conventional PCI (if configured to PCI-X, the internal PCI interface DLL is enabled regardless of PCI0_M66EN)

Table 7: PCI Bus 0 Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
MV64440 and MV64442: PCI0_AD[63:0] **MV64441:** PCI0_AD[31:0]	t/s I/O	PCI_0 Address/Data	MV64440 and MV64442: 64-bit PCI_0 multiplexed address/data bus. MV64441: 32-bit PCI_0 multiplexed address/data bus. Driven by the transaction master during address phase and write data phase. Driven by the target device during read data phase. **NOTE:** For the MV64440 and MV64442, PCI0_AD[63:32] requires a pull up. When PCI_0 interface is configured to 32-bit, the MV64440/1/2 drives these pins; a pull up is not required
MV64440 and MV64442: PCI0_CBEn [7:0] **MV64441:** PCI0_CBEn [3:0]	t/s I/O	PCI_0 Command/Byte Enable	MV64440 and MV64442: 8-bit multiplexed command/byte-enable bus, driven by transaction master. MV64441: 4-bit multiplexed command/byte-enable bus, driven by transaction master. Contains command during the address phase and byte-enable during data phase. **NOTE:** For the MV64440 and MV64442, PCI0_CBEn[7:4] requires a pull up. When PCI_0 interface is configured to 32-bit, the MV64440/1/2 drives these pins; a pull up is not required
PCI0_PAR	t/s I/O	PCI_0 Parity (low)	Even parity calculated for PCI0_AD[31:0] and PCI0_CBEn[3:0]. Driven by transaction master for address phase and write data phase. Driven by target for read data phase.
PCI0_ FRAMEn	s/t/s I/O	PCI_0 Frame	Asserted by the transaction master to indicate the beginning of a transaction. The master de-asserts PCI0_FRAMEn to indicate that the next data phase is the final data phase transaction.
PCI0_IRDYn	s/t/s I/O	PCI_0 Initiator Ready	Asserted by the transaction master to indicate it is ready to complete the current data phase of the transaction. A data phase is completed PCI0_TRDYn and PCI0_IRDYn are asserted.
PCI0_DEV SELn	s/t/s I/O	PCI_0 Device Select	Asserted by the target of the current access. As a master, the MV64440/1/2 expects the target to assert PCI0_DEVSELn within five bus cycles. If the target does not assert PCI0_DEVSELn within the required bus cycles, the MV64440/1/2 aborts the cycle. As a target, the MV64440/1/2 asserts PCI0_DEVSELn in a medium speed; two cycles after the assertion of PCI0_FRAMEn.
PCI0_TRDYn	s/t/s I/O	PCI_0 Target Ready	Asserted by the target to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when PCI0_TRDYn and PCI0_IRDYn are asserted.
PCI0_STOPn	s/t/s I/O	PCI_0 Stop	Asserted by target to indicate transaction termination. Used by a target device to generate a Retry, Disconnect, or Target Abort termination signal.

Table 7: PCI Bus 0 Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
PCI0_IDSEL	I	PCI_0 Initialization Device Select	Asserted to act as a target device chip select during PCI configuration transactions.
PCI0_REQ64n	s/t/s I/O	PCI_0 Request 64-bit Transfer	**NOTE:** Only valid for the MV64440 and MV64442 devices. Asserted by the transaction master to indicate a request of a 64-bit bus width transaction. PCI0_REQ64n timing is the same as PCI0_FRAMEn timing. **NOTE:** A 64-bit transaction occurs when PCI0_REQ64n and PCI0_ACK64n are asserted.
PCI0_ACK64n	s/t/s I/O	PCI_0 Acknowledge 64-bit Transfer	**NOTE:** Only valid for the MV64440 and MV64442 devices. Asserted by the target in response to PCI0_REQ64n to indicate it accepts a 64-bit bus width transaction. PCI0_ACK64n timing is the same as PCI0_DEVSELn timing. **NOTE:** A 64-bit transaction occurs when PCI0_REQ64n and PCI0_ACK64n are asserted.
PCI0_PAR64	t/s I/O	PCI_0 Parity (high)	**NOTE:** Only valid for the MV64440 and MV64442 devices. In cases of a 64-bit PCI transaction, even parity is calculated for PCI0_AD[63:32] and PCI0_CBE[7:4]. Driven by the transaction master for address phase and write data phase. Driven by the target for read data phase. **NOTE:** PCI0_PAR64 requires a pull up. When PCI_0 interface is configured to 32-bit, the MV64440/1/2 drives this pin; a pull up is not required
PCI0_REQn	t/s O	PCI_0 Bus Request	In a case using an external PCI arbiter, asserted by the MV64440/1/2 PCI master to indicate it requires PCI bus mastership to initiate a new transaction. **NOTE:** When using the internal PCI arbiter, leave unconnected
PCI0_GNTn	I	PCI_0 Bus Grant	In a case using an external PCI arbiter, asserted to indicates to the MV64440/1/2 PCI master that bus mastership is granted. **NOTE:** When using the internal PCI arbiter, a pull down is required
PCI0_PERRn	s/t/s I/O	PCI_0 Parity Error	Asserted when a data parity error is detected. Asserted by a target device in response to bad address or write data parity, or by a master device in response to bad read data parity.
PCI0_SERRn	o/d O	PCI_0 System Error	Asserted when a serious system error (not necessarily a PCI error) is detected.

Table 7: PCI Bus 0 Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
PCI0_INTn	o/d O	PCI_0 Interrupt Request	Asserted by the MV64440/1/2 when one of the unmasked internal interrupt sources is asserted. **NOTE:** If MSI is enabled, the MV64440/1/2 never asserts PCI0_INTn
PCI Bus 0 Interface Pin Count: 92 (MV64440 and MV64442), 53 (MV64441)			

Table 8: PCI Bus 1 Interface Pin Assignments

Pin Name	Type	Full Name	Description
PCI1_CLK	I	PCI_1 Clock	PCI bus clock. Up to 133MHz in PCI-X mode and up to 66MHz in conventional PCI mode. It is completely independent of PCI0_CLK and SYS_CLK.
PCI1_VREF	I	PCI_1 VREF	PCI reference input voltage (3.3V or 5V).
PCI1_CAL	I	PCI_1 Calibration	Allows control of the PCI output buffers' strength. Connect to VDD through a resistor. The resistor size determines the drive strength of the output buffer. **NOTE:** See *TB-119 MV644xx Design Considerations* for the recommended values of the calibration resistors.
PCI1_RSTn	I	PCI_1 Reset	Dedicated reset signal for PCI_1 interface. **NOTE:** It has no affect on PCI_0 interface nor any other MV64440/1/2 unit. When in the reset state, all PCI output pins are put into tristate and all open drain signals are floated.
PCI1_M66EN	I	PCI_1 66MHz Enable	The MV64440/1/2 samples PCI1_M66EN on reset de-assertion, in order to determine if it is connected to a 66MHz bus. If PCI1_M66EN is sampled 1, the internal PCI interface DLL is enabled. **NOTE:** Only relevant to conventional PCI (if configured to PCI-X, the internal PCI interface DLL is enabled regardless of PCI1_M66EN)
MV64440: PCI1_AD[63:0] **MV64441 and MV64442:** PCI1_AD[31:0]	t/s I/O	PCI_1 Address/Data	MV64440: 64-bit PCI_1 multiplexed address/data bus. MV64441 and MV64442: 32-bit PCI_1 multiplexed address/data bus. Driven by the transaction master during address phase and write data phase. Driven by the target device during read data phase. **NOTE:** For the MV64440, PCI1_AD[63:32] requires a pull up. When PCI_1 interface is configured to 32-bit, the MV64440 drives these pins; a pull up is not required.

Table 8: PCI Bus 1 Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
MV64440: PCI1_CBEn [7:0] **MV64441 and MV64442:** PCI1_CBEn [3:0]	t/s I/O	PCI_1 Command/Byte Enable	MV64440: 8-bit multiplexed command/byte-enable bus, driven by the transaction master. MV64441 and MV64442: 4-bit multiplexed command/byte-enable bus, driven by the transaction master. Contains command during the address phase and byte-enable during data phase. **NOTE:** For the MV64440, PCI1_CBEn[7:4] requires a pull up. When PCI_1 interface is configured to 32-bit, the MV64440 drives these pins; a pull up is not required
PCI1_PAR	t/s I/O	PCI_1 Parity (low)	Even parity calculated for PCI1_AD[31:0] and PCI1_CBEn[3:0]. Driven by the transaction master for the address phase and write data phase. Driven by the target for the read data phase.
PCI1_ FRAMEn	s/t/s I/O	PCI_1 Frame	Asserted by the transaction master to indicate the beginning of a transaction. The master de-asserts PCI1_FRAMEn to indicate that the next data phase is the final data phase transaction.
PCI1_IRDYn	s/t/s I/O	PCI_1 Initiator Ready	Asserted by the transaction master to indicate that it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI1_TRDYn and PCI1_IRDYn are asserted.
PCI1_DEV SELn	s/t/s I/O	PCI_1 Device Select	Asserted by the target of the current access. As a master, the MV64440/1/2 expects the target to assert PCI1_DEVSELn within five bus cycles. If the target does not assert PCI1_DEVSELn within the required bus cycles, the MV64440/1/2 aborts the cycle. As a target, the MV64440/1/2 asserts PCI1_DEVSELn in a medium speed, two cycles after the assertion of PCI1_FRAMEn.
PCI1_TRDYn	s/t/s I/O	PCI_1 Target Ready	Asserted by the target to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI1_TRDYn and PCI1_IRDYn are asserted.
PCI1_STOPn	s/t/s I/O	PCI_1 Stop	Asserted by the target to indicate transaction termination. PCI1_STOPn is used by a target device to generate a Retry, Disconnect, or Target Abort termination.
PCI1_IDSEL	I	PCI_1 Initialization Device Select	Asserted to act as a target device chip select during the PCI configuration transactions.

Table 8: PCI Bus 1 Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
PCI1_REQ64n	s/t/s I/O	PCI_1 Request 64-bit Transfer	**NOTE:** Only valid for the MV64440 device. Asserted by the transaction master to indicate a request of a 64-bit bus width transaction. PCI1_REQ64n timing is the same as PCI1_FRAMEn timing. **NOTE:** A 64-bit transaction occurs if the PCI1_REQ64n and PCI1_ACK64n signals are asserted.
PCI1_ACK64n	s/t/s I/O	PCI_1 Acknowledge 64-bit Transfer	**NOTE:** Only valid for the MV64440 device. Asserted by the target in response to PCI1_REQ64n to indicate that it accepts a 64-bit bus width transaction. PCI1_ACK64n timing is the same as PCI1_DEVSELn timing. **NOTE:** A 64-bit transaction occurs when PCI1_REQ64n and PCI1_ACK64n are asserted.
PCI1_PAR64	t/s I/O	PCI_1 Parity (high)	**NOTE:** Only valid for the MV64440 device. In cases of 64-bit PCI transactions, even parity is calculated for PCI1_PAD[63:32] and PCI1_CBE[7:4]. Driven by the transaction master for address phase and write data phase. Driven by the target for read data phase. **NOTE:** PCI1_PAR64 requires a pull up. When PCI_1 interface is configured to 32-bit, the MV64440 drives this pin; a pull up is not required
PCI1_REQn	t/s O	PCI_1 Bus Request	In a case using an external PCI arbiter, asserted by the MV64440/1/2 PCI master to indicate it requires the PCI bus mastership to initiate a new transaction. **NOTE:** When using the internal PCI arbiter, leave unconnected
PCI1_GNTn	I	PCI_1 Bus Grant	In a case using an external PCI arbiter, asserted to indicate to the MV64440/1/2 PCI master that bus mastership is granted. **NOTE:** When using the internal PCI arbiter, a pull down is required.
PCI1_PERRn	s/t/s I/O	PCI_1 Parity Error	Asserted when a data parity error is detected. Asserted by a target device in response to bad address or write data parity, or by a master device in response to bad read data parity.
PCI1_SERRn	o/d O	PCI_1 System Error	Asserted when a serious system error (not necessarily a PCI error) is detected.
PCI1_INTn	o/d O	PCI_1 Interrupt Request	Asserted by the MV64440/1/2 when one of the unmasked internal interrupt sources is asserted. **NOTE:** If MSI is enabled, the MV64440/1/2 never asserts PCI1_INTn
PCI Bus 1 Interface Pin Count: 92 (MV64440), 53 (MV64441 and MV64442)			

Table 9: PCI_0 CompactPCI Hot Swap Pin Assignments

Pin Name	Type	Full Name	Description
PCI0_ENUMn	o/d O	CompactPCI Hot Swap ENUMn interrupt	If ENUM is enabled, asserted by the MV64440/1/2 during hot swap insertion or removal
PCI0_LED	t/s O	CompactPCI Hot Swap LED	Driven by the MV64440/1/2 to turn the LED on/off.
PCI0_HS	I	CompactPCI Hot Swap Handle Switch	Sampled handle switch status to identify board insertion/ removal. **NOTE:** If not using CompactPCI Hot Swap, must be tied to VSS
PCI0_64ENn	I	CompactPCI Hot Swap 64-bit PCI Enable	The MV64440 and MV64442 devices sample the PCI0_64ENn pin on reset de-assertion, rather than PCI0_REQ64n, to determine whether it is connected to a 64-bit PCI bus.
CompactPCI Hot Swap Pin Count: 4 (MV64440 and MV64442), 3 (MV64441)			

Table 10: DDR SDRAM Interface Pin Assignments

Pin Name	Type	Full Name	Description
M_CLK_OUT	O	SDRAM Clock	DRAM clock input.
M_CLK_OUTn	O	SDRAM Clock	DRAM clock input.
M_SSTLVREF_0	I	SSTL2 VREF	Reference voltage for SSTL interface. Must be half of the voltage for the V_{dd} SDRAM @ SSTL mode, see EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5 volts, SSTL_2).
M_SSTLVREF_1	I	SSTL2 VREF	Reference voltage for SSTL interface. Must be half of the voltage for the V_{dd} SDRAM @ SSTL mode, see EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5 volts, SSTL_2).
NOTE: M_SSTLVREF_0 and M_SSTLVREF_1 are connected to the same VREF rail. Hence, the balls are connected to the same voltage.			
M_RASn	O	SDRAM Row Address Select	Asserted by the MV64440/1/2 to indicate an active ROW address driven on the DRAM address lines.
M_CASn	O	SDRAM Column Address Select	Asserted by the MV64440/1/2 to indicate an active column address driven on the DRAM address lines.
M_WEn	O	SDRAM Write Enable	Asserted by the MV64440/1/2 to indicate a write command to the SDRAM.

Table 10: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
M_DA[13:0]	O	SDRAM Address	Driven by the MV64440/1/2 during M_RASn and M_CASn cycles to generate along with bank address bits 28-bit SDRAM address.
M_BA[1:0]	O	SDRAM Bank Address	Driven by the MV64440/1/2 during M_RASn and M_CASn cycles to select one of the 4 DRAM virtual banks.
M_CSn[3:0]	O	SDRAM Chip Selects	Asserted by the MV64440/1/2 to select a specific SDRAM bank.
M_DQ[63:0]	t/s I/O	SDRAM Data Bus	Driven by the MV64440/1/2 during write to SDRAM. Driven by SDRAM during reads.
M_CB[7:0]	t/s I/O	SDRAM ECC byte	Driven by the MV64440/1/2 during write to SDRAM. Driven by SDRAM during reads.
M_DQS[8:0]	t/s I/O	SDRAM Data Strobe	Driven by the MV64440/1/2 during write to SDRAM. Driven by SDRAM during reads.
M_DM[8:0]/ M_DQS[17:9]	ts I/O	SDRAM Data Mask	Asserted by the MV64440/1/2 to select the specific bytes out of the 72-bit data/ECC to be written to the SDRAM.
		SDRAM Data Strob	Additional 9-bit M_DQS pins when interfacing x4 DDR devices **NOTE:** When interfacing x4 devices, data mask (DM) is not supported
M_CKE0	O	SDRAM Clock Enable	Driven by the MV64440 or MV64441 high to enable DRAM clock. Driven low when putting the DRAM in self refresh mode.
M_CKE1	O	SDRAM Clock Enable	Driven by the MV64440 or MV64441 high to enable DRAM clock. Driven low when putting the DRAM in self refresh mode.
M_START BURST	O	Start Burst	MV64440/1/2 indication of starting a burst. Asserted with the first M_CASn cycle of DRAM access. **NOTE:** Must be routed on board all the way to the DRAM, and back to the MV64440/1/2 as M_STARTBURST_IN.
M_START BURST_IN	I	Start Burst Input	M_STARTBURST signal routed back to MV64440/1/2. Used as a reference signal for the incoming read data driven by the SDRAM.
M_DCAL	I	DRAM Data Calibration	Allows control of the DRAM DQ/DQS output buffers' strength. Connect to VDD_DRAM through a resistor. The resistor size determines the drive strength of the output buffer. **NOTE:** See *TB-119 MV644xx Design Considerations* for the recommended values of the calibration resistors.

Table 10: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
M_ACAL	I	DRAM Address/Control Calibration	Allows control of the DRAM address/control signals output buffers' strength. Connect to VDD_DRAM through a resistor. The resistor size determines the drive strength of the output buffer. **NOTE:** See *TB-119 MV644xx Design Considerations* for the recommended values of the calibration resistors.
SDRAM Interface Pin Count: 124 (MV64440 and MV64441), 122 (MV64442)			

Table 11: Device Interface Pin Assignments

Pin Name	Type	Full Name	Description
DEV_ALE	t/s O	Device Address Latch Enable	Used to latch the DEV_AD[27:2], DEV_BOOTCSn, DEV_CSn[3:0], and DEV_RWn signals from the AD bus.
DEV_CS TIMINGn	t/s O	Device Chip Select Timing	Active for the entire device transaction. Used to qualify DEV_RWn, DEV_CSn[3:0], and DEV_BOOTCSn signals.
DEV_AD[0]/ DEV_BOOT CSn	t/s I/O	Device Data[0]	Used as device data bit [0] during the data phase. Driven by MV64440/1/2 on write access, and by the device on read access.
		Boot Chip Select	Used as boot device chip select during address phase.
DEV_AD[1]/ DEV_RWn	t/s I/O	Device Data[1]	Used as device data bus bit [1] during the data phase. Driven by MV64440/1/2 on write access, and by the device on read access.
		Device Write	Used as device read (1) or write (0) indication during address phase.
DEV_AD[27:2]	t/s I/O	Device Address	DEV_AD[27:2] are used as device address during the address phase. Need to be latched by an external device, using DEV_ALE signal. The latched DEV_AD[27:2] along with DEV_BADR[2:0] are used as the device address.
		Device Data	Used as device data bus during the data phase. Driven by MV64440/1/2 on write access, and by the device on read access.
DEV_AD [31:28]/ DEV_CSn[3:0]	t/s I/O	Device Data[31:28]	Used as device data bus bits [31:28] during the data phase. Driven by MV64440/1/2 on write access, and by the device on read access.
		Device Chip Select [3:0]	Used as device chip select [3:0] during address phase.

Table 11: Device Interface Pin Assignments (Continued)

Pin Name	Type	Full Name	Description
DEV_BADR [2:0]	t/s O	Device Burst Address	Driven by the MV64440/1/2 during burst read/write transactions to a device. **NOTE:** The MV64440/1/2 increments the burst address with each data transfer.
DEV_WEn[3:0]	t/s O	Device Write Byte Enables	Asserted by the MV64440/1/2 to select the specific bytes out of the 32-bit AD bus to be written.
DEV_DP[3:0]	t/s I/O	Device Parity	Device parity (configurable even or odd parity). DEV_DP[0] corresponds to DEV_AD[7:0] DEV_DP[1] to DEV_AD[15:8] DEV_DP[2] to DEV_AD[23:16] DEV_DP[3] to DEV_AD[31:24]. Driven by MV64440/1/2 during address phase and write data phase, and by the device on read data phase.
DEV_READYn	I	Device Ready:	Used as cycle extender when interfacing a slow device. When inactive during a device access, access is extended until DEV_READYn assertion. **NOTE:** If not using DEV_READYn, tie to VSS.
Device Interface Pin Count: 46			

Table 12: Ethernet Port0 Interface Pin Assignments
NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Pin Name	Type	Full Name	Description
P0_TXCLK/ P0_RXCLK[1]	I	Transmit Clock	**For GMII operating in 1000:** This pin is not used and should be pulled down. **For GMII PHYs operating in 10/100:** This pin provides the timing reference for the transmission of the P0_TXEN,P0_TXD[3:0] signals. It operates at 2.5 MHz when in 10 Mbps, and at 25 MHz in 100 Mbps speed.
		Receive Clock	**For the 10-bit interface:** This pin provides the receive code group complimentary 62.5 MHz clock input. Both phases are used to strobe P0_RX[9:0] inputs.

Table 12: Ethernet Port0 Interface Pin Assignments (Continued)

NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Pin Name	Type	Full Name	Description
P0_TXD[7:0]/ P0_TX[7:0]	O	Transmit Data	**For GMII PHYs operating in 1000:** P0_TXD[7:0] contain the transmit data outputs and are synchronous to the P0_TXCLK_OUT output. **For GMII PHYs operating in 10/100:** P0_TXD[3:0] contain the transmit data outputs and are synchronous to the P0_TXCLK input. Pins P0_TXD[7:4] are undefined and should Not be Connected (NC).
		Transmit Data	**For the 10-bit interface:** P0_TX[7:0] are bits [7:0] of the Tx_code_group[9:0] output to the transceiver. They are synchronous to P0_TXCLK_OUT.
P0_TXEN/ P0_TX[8]	O	Transmit Enable	**For GMII PHYs operating in 10/100/1000:** P0_TXEN indicates that the packet is being transmitted to the PHY. It Is synchronous to P0_TXCLK_OUT in GMII mode and to P0_TXCLK in MII mode.
		Transmit Data	**For the 10-bit interface:** P0_TX[8] is bit 8 of the Tx_code_group[9:0] output to the transceiver. It is synchronous to P0_TXCLK_OUT.
P0_TXERR/ P0_TX[9]	O	Transmit Error	**For GMII PHYs operating in 1000:** P0_TXERR is used for implementing carrier extension in half-duplex. Is synchronous to P0_TXCLK_OUT. **For GMII PHYs operating in 10/100:** This output is irrelevant.
		Transmit Data	**For the 10-bit interface:** Tx0[9] is bit 9 of the Tx_code_group[9:0] output to the transceiver. It is synchronous to P0_TXCLK_OUT. This pin is only relevant for the 10-bit interface.
P0_TXCLK_ OUT	O	Transmit Clock Output	**For GMII PHYs operating in 1000:** Provides the timing reference for the transfer of the P0_TXEN, P0_TXERR, and P0_TXD[7:0] signals. It operates at 125 MHz. **For GMII PHYs operating in 10/100:** This pin is irrelevant and must Not be Connected (NC). **For the 10-bit interface**: This pin is the PMA Transmit Clock. It provides the timing reference for the transfer of the P0_TX[9:0] signals. It operates at 125 MHz.
P0_CRS	I/O	Carrier Sense	**For GMII PHYs:** Indicates that either the transmit or receive medium is non-idle. P0_CRS is not synchronous to any clock. **For the 10-bit interface:** This pin is not used and should be pulled down. **NOTE:** P0_CRS is an output when configured to SyncFIFO interface, otherwise is as input.

Table 12: Ethernet Port0 Interface Pin Assignments (Continued)

NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Pin Name	Type	Full Name	Description
P0_RXD[3:0]/ P0_RX[3:0]	I	Receive Data	**For GMII PHYs operating in 10/100:** P0_RXD[3:0] contains the receive data inputs and is synchronous to P0_RXCLK input.
		Receive Data	**For the 10-bit interface**: P0_RX[3:0] are bits [3:0] of the Rx_code_group[9:0] input from the transceiver. They are synchronous to P0_RXCLK[1:0].
P0_RXD[7:4]/ P0_RX[7:4]	I	Receive Data	**For GMII PHYs operating in 1000:** P0_RXD[7:4] contains the receive data inputs and are synchronous to Px_RXCLK input. **For GMII PHYs operating in 10/100:** P0_RXD[7:4] must be held low.
		Receive Data	**For the 10-bit interface**: P0_RX[7:4] are bits [7:4] of the Rx_code_group[9:0] input from the transceiver. They are synchronous to P0_RXCLK[1:0].
P0_RXERR/ P0_RX[9]	I	Receive Error	**For GMII PHYs operating in 1000:** Also used for implementing carrier extension in half-duplex. Synchronous to P0_RXCLK[1:0]. **For GMII PHYs operating in 10/100:** Synchronous to P0_RXCLK input.
		Receive Data	**For the 10-bit interface:** P0_RX[9] is bit 9 of the Rx_code_group[9:0] input from the transceiver. It is synchronous to P0_RXCLK[1:0]. This pin is only relevant for the 10-bit interface.
P0_RXDV/ P0_RX[8]	I	Receive Data Valid	**For GMII PHYs:** Indicates that valid data is present on the P0_RXD lines. It is synchronous to P0_RXCLK.
		Receive Data	**For the 10-bit interface:** P0_RX[8] is bit [8] of the Rx_code_group [9:0] input from the transceiver. It is synchronous to P0_RXCLK[1:0].
P0_RXCLK/ P0_RXCLK[0]	I	Receive Clock	**For GMII mode operating in 1000 (P0_RXCLK):** Provides the timing reference for the reception of the P0_RXDV, P0_RXERR, and P0_RXD[7:0] signals. It operates at 125 MHz. **For GMII mode operating in 10/100 (P0_RXCLK):** Provides the timing reference for the reception of the P0_RXDV, P0_RXERR, and P0_RXD[3:0] signals. It operates at 2.5 MHz when in 10 Mbps, and at 25 MHz in 100 Mbps speed. **For the 10-bit interface (P0_RXCLK[0]):** This pin is the receive code group complimentary 62.5 MHz clock input. Both phases are used to strobe Rx0[9:0] inputs.
			For the 10-bit interface (P0_RXCLK[0]): This pin is the receive code group complimentary 62.5 MHz clock input. Both phases are used to strobe Rx0[9:0] inputs.

Table 12: Ethernet Port0 Interface Pin Assignments (Continued)

NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Pin Name	Type	Full Name	Description
P0_COL	I	Collision Detect	**For GMII mode operating in 10/100 (P0_RXCLK[1]):** Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. P0_COL is not synchronous to any clock.
Device Interface Pin Count: 25			

Table 13: Ethernet Port1 Interface Pin Assignments

NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Ethernet Port1 is only valid for the MV64440 and MV64441 devices.

Pin Name	Type	Full Name	Description
P1_TXCLK/ P1_RXCLK[1]	I	Transmit Clock	**For GMII operating in 1000:** This pin is not used and should be pulled down. **For GMII PHYs operating in 10/100:** Provides the timing reference for the transmission of the P1_TXEN, P1_TXD[3:0] signals. It operates at 2.5 MHz when in 10 Mbps, and at 25 MHz in 100 Mbps speed.
		Receive Clock	**For the 10-bit interface:** Provides the receive code group complimentary 62.5 MHz clock input. Both phases are used to strobe Rx0[9:0] inputs.
P1_TXD[7:0]/ P1_TX[7:0]	O	Transmit Data	**For GMII PHYs operating in 1000:** P1_TXD[7:0] contains the transmit data outputs and is synchronous to the P1_TXCLK_OUT output. **For GMII PHYs operating in 10/100:** P1_TXD[3:0] contains the transmit data outputs and is synchronous to the P1_TXCLK_OUT input. Pins P1_TXD[7:4] are undefined and must Not be Connected (NC).
		Transmit Data	**For the10-bit interface:** Tx1[7:0] are bits [7:0] of the Tx_code_group[9:0] output to the transceiver. They are synchronous to P1_TXCLK_OUT.
P1_TXEN/ P1_TX[8]	O	Transmit Enable	**For GMII PHYs operating in 10/100/1000:** Indicates that the packet is being transmitted to the PHY. It Is synchronous to P1_TXCLK_OUT in GMII mode and to P1_TXCLK in MII mode.
		Transmit Data	**For the 10-bit interface:** P1_TX[8] is bit 8 of the Tx_code_group[9:0] output to the transceiver. It is synchronous to P1_TXCLK_OUT.

Table 13: Ethernet Port1 Interface Pin Assignments (Continued)

NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Ethernet Port1 is only valid for the MV64440 and MV64441 devices.

Pin Name	Type	Full Name	Description
P1_TXERR/ P1_TX[9]	O	Transmit Error	**For GMII PHYs operating in 1000:** P1_TXERR is used for implementing carrier extension in half-duplex. Is synchronous to P1_TXCLK_OUT. **For GMII PHYs operating in 10/100:** This output is irrelevant.
		Transmit Data	**For the 10-bit interface:** P1_TX[9] is bit 9 of the Tx_code_group[9:0] output to the transceiver. It is synchronous to P1_TXCLK_OUT. This pin is only relevant for the 10-bit interface.
P1_TXCLK_ OUT	O	Transmit Clock Output	**For GMII PHYs operating in 1000:** Provides the timing reference for the transfer of the P1_TXEN, P1_TXERR, and P1_TXD[7:0] signals. It operates at 125 MHz. **For GMII PHYs operating in 10/100:** This pin is irrelevant and must Not be Connected (NC). **For the 10-bit interface**: This pin is the PMA Transmit Clock. It provides the timing reference for the transfer of the P1_TX[9:0] signals. It operates at 125 MHz.
P1_CRS	I/O	Carrier Sense	**For GMII PHYs:** Indicates that either the transmit or receive medium is non-idle. P1_CRS is not synchronous to any clock. **For the 10-bit interface:** This pin is not used and should be pulled down. **NOTE:** P1_CRSis an output when configured to SyncFIFO interface, otherwise is as input.
P1_RXD[3:0]/ P1_RX[3:0]	I	Receive Data	**For GMII PHYs operating in 10/100:** P1_RXD[3:0] contains the receive data inputs and is synchronous to Px_RXCLK input.
		Receive Data	**For the 10-bit interface**: Rx1[3:0] are bits [3:0] of the Rx_code_group[9:0] input from the transceiver. They are synchronous to P1_RXCLK[1:0].
P1_RXD[7:4]/ P1_RX[7:4]	I	Receive Data	**For GMII PHYs operating in 1000:** P1_RXD[7:4] contains the receive data inputs and are synchronous to Px_RXCLK input. **For GMII PHYs operating in 10/100:** P1_RXD[7:4] must be held low.
		Receive Data	**For the 10-bit interface**: P1_RX[7:4] are bits [7:4] of the Rx_code_group[9:0] input from the transceiver. They are synchronous to P1_RXCLK[1:0].

Table 13: Ethernet Port1 Interface Pin Assignments (Continued)

NOTE: See the applicable gigabit Ethernet pins multiplexing section for information about using the RGMII and FIFO interfaces on the Gigabit Ethernet ports.

Ethernet Port1 is only valid for the MV64440 and MV64441 devices.

Pin Name	Type	Full Name	Description
P1_RXERR/ P1_RX[9]	I	Receive Error	**For GMII PHYs operating in 1000:** Also used for implementing carrier extension in half-duplex. Synchronous to P1_RXCLK[1:0]. **For GMII PHYs operating in 10/100:** Synchronous to P1_RXCLK input.
		Receive Data	**For the 10-bit interface:** P1_RX[9] is bit 9 of the Rx_code_group[9:0] input from the transceiver. It is synchronous to P1_RXCLK[1:0]. This pin is only relevant for the 10-bit interface.
P1_RXDV/ P1_RX[8]	I	Receive Data Valid	**For GMII PHYs:** Indicates that valid data is present on the P1_RXD lines. It is synchronous to P1_RXCLK.
		Receive Data	**For the 10-bit interface:** P1_RX[8] is bit [8] of the Rx_code_group [9:0] input from the transceiver. It is synchronous to P1_RXCLK [1:0].
P1_RXCLK/ P1_RXCLK[0]	I	Receive Clock	**For GMII mode operating in 1000 (P1_RXCLK):** Provides the timing reference for the reception of the P1_RXDV, P1_RXERR, and P1_RXD[7:0] signals. It operates at 125 MHz. **For GMII mode operating in 10/100 (P1_RXCLK):** Provides the timing reference for the reception of the P1_RXDV, P1_RXERR, and P1_RXD[3:0] signals. It operates at 2.5 MHz when in 10 Mbps, and at 25 MHz in 100 Mbps speed. **For the 10-bit interface (P1_RXCLK[0]):** This pin is the receive code group complimentary 62.5 MHz clock input. Both phases are used to strobe Rx1[9:0] inputs.
		Collision Detect	**For GMII mode operating in 10/100 (P1_RXCLK):** Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. P1_COL is not synchronous to any clock.
P1_COL	I	Collision Detect	**For GMII mode operating in 10/100 (P1_RXCLK):** Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. P1_COL is not synchronous to any clock.
Device Interface Pin Count: 25			

Table 14: Ethernet Control Interface Pin Assignments

Pin Name	Type	Full Name	Description
CLK125	I	Reference Clock	Provides the timing reference for the 1000 Mb mode and must operate at 125 MHz. **NOTE:** When all of the used Ethernet ports are configured to MII only mode, tie it to pull down. Any other configuration requires an input of 125 MHz clock from the PHY.
MDC	O	Management Data Clock	MDC is the CLK input divided by 128. Provides the timing reference for the transfer of the MDIO signal.
MDIO	I/O	Management Data In/Out	Used to transfer control information and status between PHY devices and MV64440/1/2. **NOTE:** When at least one of the GbE ports is used, it is highly recommended to connect the MDIO signal to a pull up resistor.
FIFOCLK	I	FIFO Interface Clock	Provides the timing reference for the FIFO interface. Up to 133 MHz. **NOTE:** Must not exceed TCLK (core clock) frequency. When not using the FIFO interface, tie it to a pull down.
RGMII_VREF	I	RGMII Reference Voltage	Reference voltage for RGMII interface when configured to HSTL mode. **NOTE:** If using the CMOS mode, connect to the Ethernet power supply. Must be half of the voltage for the Vdd Ethernet @ HSTL mode, see EIA/JEDEC standard EIA/JESD8-6 (High speed transceiver logic (HSTL) A 1.5V output buffer supply voltage based interface standard for digital integrated circuits).
ETHER_CAL	I	Ethernet Port Calibration	Allows control of the Ethernet interface signal output buffer strength. Connect to V_ETH0 through a resistor. The resistor size determines the drive strength of the output buffer. **NOTE:** See *TB-119 MV644xx Design Considerations* for the recommended values of the calibration resistors.
Serial Interface Pin Count: 5			

Table 15: MPP Interface Pin Assignment

Pin Name	Type	Full Name	Description
MPP[31:0]	I/O	Multi Purpose Pins	Various functionalities
MPP Interface Pin Count: 32			

Table 16: TWSI Pin Assignment
NOTE: These pins are driven low during reset assertion.

Pin Name	Type	Full Name	Description
SCK	o/d I/O	TWSI Clock	TWSI serial clock. Serves as output when the MV64440/1/2 acts as a TWSI master Serves as input when the MV64440/1/2 acts as a TWSI slave. **NOTE:** Pull up required.
SDA	o/d I/O	TWSI Serial Data	Address or write data driven by the TWSI master or read response data driven by the TWSI slave **NOTE:** Pull up required.
TWSI Interface Pin Count: 2			

Table 17: JTAG Pin Assignment
NOTE: The JTAG pins are not 5V tolerant.

Pin Name	Type	Full Name	Description
JT_CLK	I	JTAG Clock	Clock input for the MV64440/1/2 JTAG controller. **NOTE:** A pull down is required
JT_RSTn	I	JTAG Reset	When asserted, resets the MV64440/1/2 JTAG controller. **NOTE:** A pull down is required. If this pull down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for JTAG interface operation. The TAP can be reset by driving JT_MS signal HIGH for five JT_CLK cycles.
JT_MS	I	JTAG Mode Select	Controls the MV64440/1/2 JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** A pull up is required. Can be pulled either high or low. It has no effect on the TAP controller logic, as long as it is not floating.
JT_DO	O	JTAG Data In	JTAG serial data output. Driven by the MV64440/1/2 on falling edge of JT_CLK.
JT_DI	I	JTAG Data Out	JTAG serial data input. Sampled with JT_CLK rising edge. **NOTE:** A pull up is required. Can be pulled either high or low. It has no effect on the TAP controller logic, as long as it is not floating.
JTAG Interface Pin Count: 5			

Use Table 18 to determine the strapping configuration for systems when one of the following interfaces is not used.

Table 18: Unused Interface Strapping

Unused Interface	Strapping
CPU	Pull up: CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCTCEn Pull down: CPU_TCMATCH Reset configuration: Pull down DEV_AD[5], DEV_AD[8], DEV_AD[9]
Ethernet	Pull down: Px_TXCLK, Px_CRS, Px_COL, Px_RXCLK, Px_RXD[9:0], Px_RXDV, Px_RXERR **NOTE:** When the Ethernet port is not used, tie MDC/MDIO and CLK125 to pull down.
TWSI	Pull up SCK and SDA.
MPP	If all signals are configured as GPIO outputs, no external pullups required.
SDRAM	Route M_STARTBURST to M_STARTBURST_IN.
Device	Pull down the DEV_READYn pin.
PCI	To bypass the need of putting pullups on the data signals, pulldown PCIx_GNTn and configure the chip to work with external PCI arbiter, EN bit [31] (see the PCI Interface Registers in the *MV64440/1/2 Datasheet User Manual*.) PCIx_CLK must be connected to slaw clock (5MHz to 66MHz). PCIx_RSTn can be driven from the same source as reset to SYSRSTn. Must be deasserted with or after SYSRSTn de-assertion. PCIx_VREF must be tied to a 3.3V or 5V input voltage. Pull up: PCIx_FRAMEn, PCIx_IRDYn, PCIx_DEVSELn, PCIx_STOPn, PCIx_TRDYn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PERRn, PCI0_64ENn, PCI0_HS **NOTE:** PCIx_REQ64n, PCIx_ACK64n, and PCI0_64ENn only apply to the MV64440 and MV64442 devices.

Section 5. MV64440 Pinout Map and Table, 844 Pin BGA

Figure 7: MV64440 Pinout Map (Top View, Left Side)

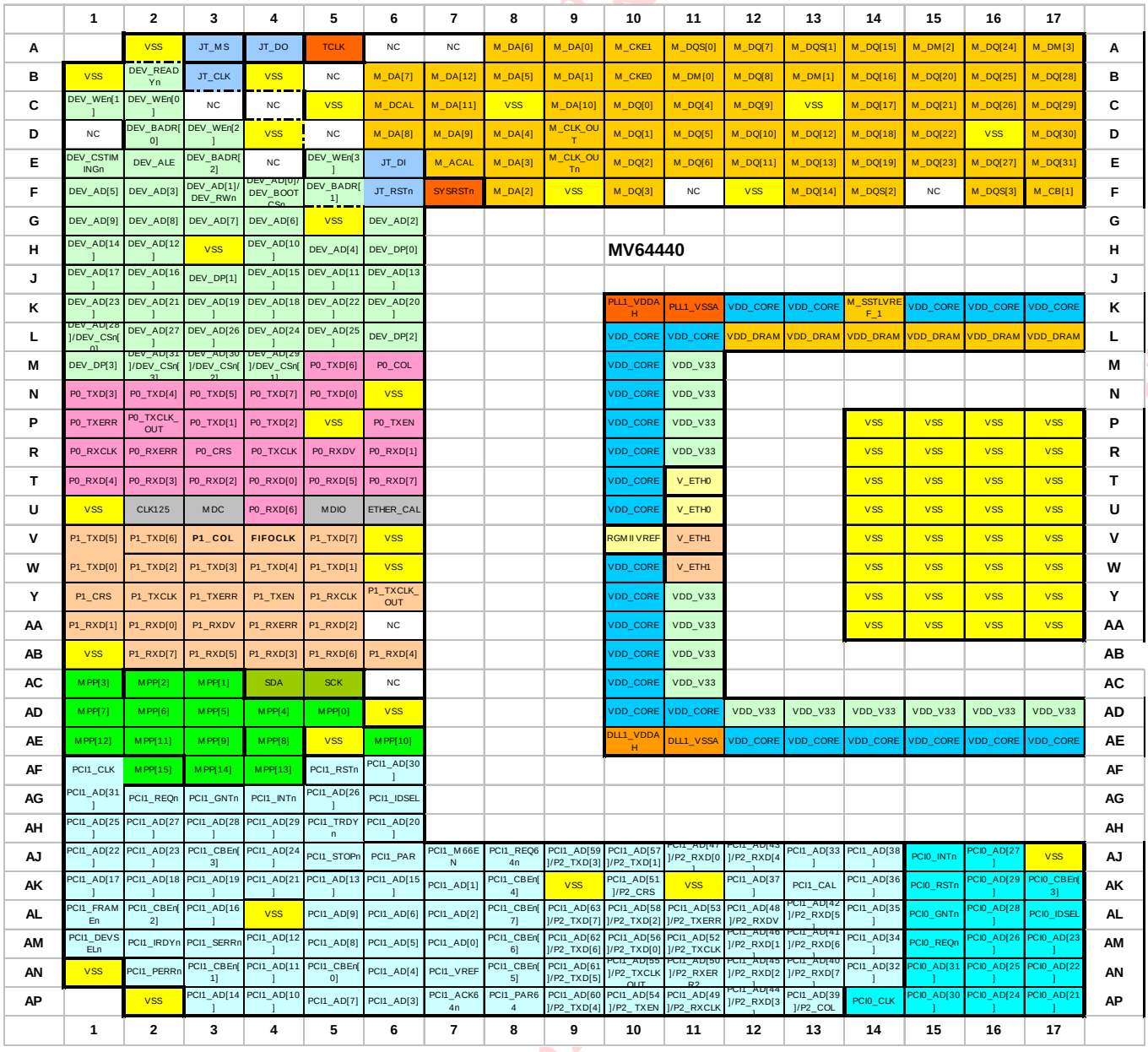
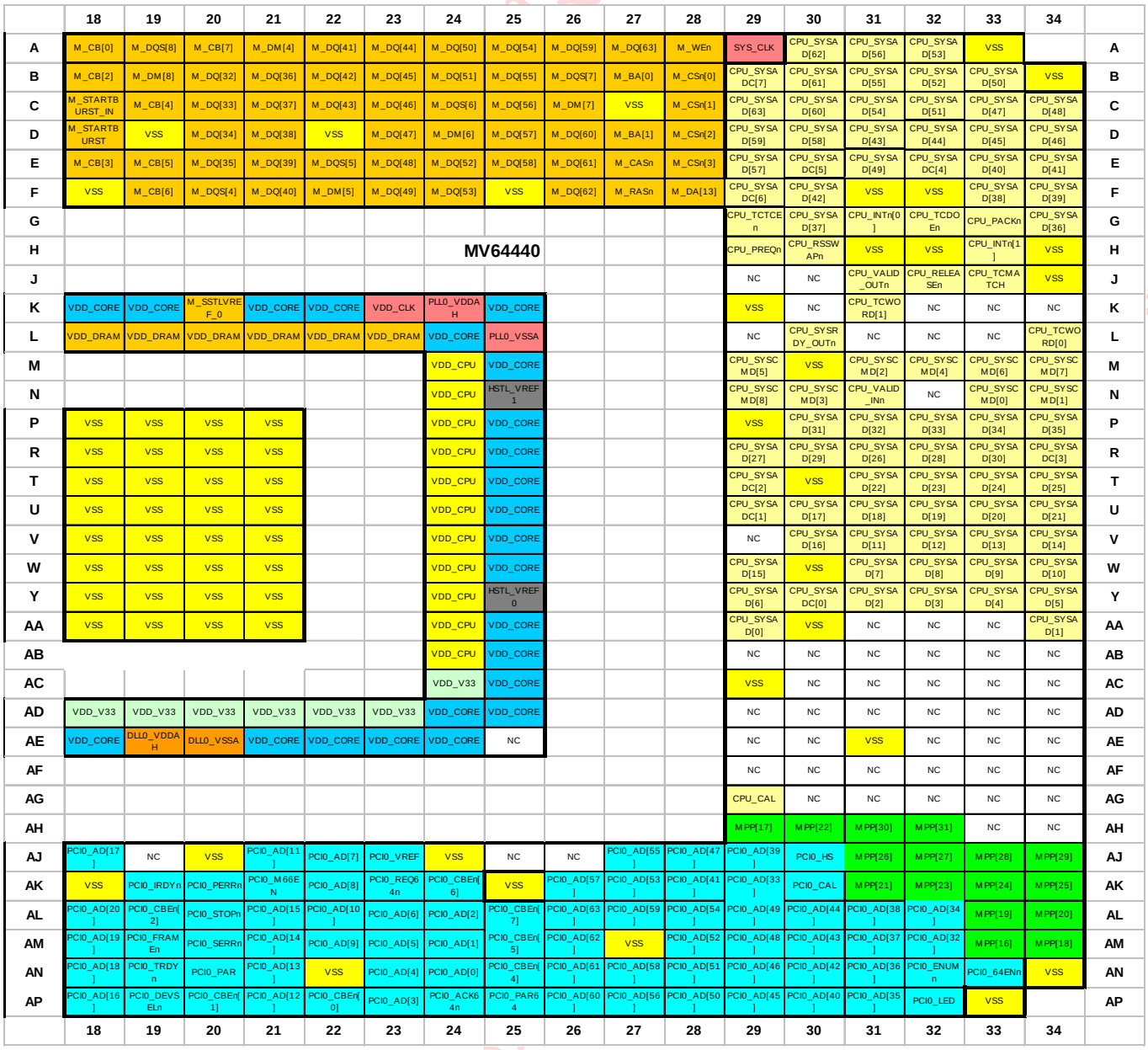


Figure 8: MV64440 Pinout Map (Top View, Right Side)



	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	M_CB[0]	M_DQS[8]	M_CB[7]	M_DM[4]	M_DQ[41]	M_DQ[44]	M_DQ[50]	M_DQ[54]	M_DQ[59]	M_DQ[63]	M_WEn	SYS_CLK	CPU_SYSAD[62]	CPU_SYSAD[56]	CPU_SYSAD[53]	VSS		A
B	M_CB[2]	M_DM[8]	M_DQ[32]	M_DQ[36]	M_DQ[42]	M_DQ[45]	M_DQ[51]	M_DQ[55]	M_DQS[7]	M_BA[0]	M_CSn[0]	CPU_SYSADC[7]	CPU_SYSAD[61]	CPU_SYSAD[55]	CPU_SYSAD[52]	CPU_SYSAD[50]	VSS	B
C	M_STARTBURST_IN	M_CB[4]	M_DQ[33]	M_DQ[37]	M_DQ[43]	M_DQ[46]	M_DQS[6]	M_DQ[56]	M_DM[7]	VSS	M_CSn[1]	CPU_SYSAD[63]	CPU_SYSAD[60]	CPU_SYSAD[54]	CPU_SYSAD[51]	CPU_SYSAD[47]	CPU_SYSAD[48]	C
D	M_STARTBURST	VSS	M_DQ[34]	M_DQ[38]	VSS	M_DQ[47]	M_DM[6]	M_DQ[57]	M_DQ[60]	M_BA[1]	M_CSn[2]	CPU_SYSAD[59]	CPU_SYSAD[58]	CPU_SYSAD[43]	CPU_SYSAD[44]	CPU_SYSAD[45]	CPU_SYSAD[46]	D
E	M_CB[3]	M_CB[5]	M_DQ[35]	M_DQ[39]	M_DQS[5]	M_DQ[48]	M_DQ[52]	M_DQ[58]	M_DQ[61]	M_CASn	M_CSn[3]	CPU_SYSAD[57]	CPU_SYSADC[5]	CPU_SYSAD[49]	CPU_SYSADC[4]	CPU_SYSAD[40]	CPU_SYSAD[41]	E
F	VSS	M_CB[6]	M_DQS[4]	M_DQ[40]	M_DM[5]	M_DQ[49]	M_DQ[53]	VSS	M_DQ[62]	M_RASn	M_DA[13]	CPU_SYSADC[6]	CPU_SYSAD[42]	VSS	VSS	CPU_SYSAD[38]	CPU_SYSAD[39]	F
G												CPU_TCTCEn	CPU_SYSAD[37]	CPU_INTn[0]	CPU_TCDOEn	CPU_PACKn	CPU_SYSAD[36]	G
H							MV64440					CPU_PREQn	CPU_RSSWAPn	VSS	VSS	CPU_INTn[1]	VSS	H
J												NC	NC	CPU_VALID_OUTn	CPU_RELEASEn	CPU_TCMATCH	VSS	J
K	VDD_CORE	VDD_CORE	M_SSTLVREF_0	VDD_CORE	VDD_CORE	VDD_CLK	PLL0_VDDAH	VDD_CORE				VSS	NC	CPU_TCWORD[1]	NC	NC	NC	K
L	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_CORE	PLL0_VSSA				NC	CPU_SYSRDY_OUTn	NC	NC	NC	CPU_TCWORD[0]	L
M							VDD_CPU	VDD_CORE				CPU_SYSCMD[5]	VSS	CPU_SYSCMD[2]	CPU_SYSCMD[4]	CPU_SYSCMD[6]	CPU_SYSCMD[7]	M
N							VDD_CPU	HSTL_VREF1				CPU_SYSCMD[8]	CPU_SYSCMD[3]	CPU_VALID_INn	NC	CPU_SYSCMD[0]	CPU_SYSCMD[1]	N
P	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				VSS	CPU_SYSAD[31]	CPU_SYSAD[32]	CPU_SYSAD[33]	CPU_SYSAD[34]	CPU_SYSAD[35]	P
R	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[27]	CPU_SYSAD[29]	CPU_SYSAD[26]	CPU_SYSAD[28]	CPU_SYSAD[30]	CPU_SYSADC[3]	R
T	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSADC[2]	VSS	CPU_SYSAD[22]	CPU_SYSAD[23]	CPU_SYSAD[24]	CPU_SYSAD[25]	T
U	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSADC[1]	CPU_SYSAD[17]	CPU_SYSAD[18]	CPU_SYSAD[19]	CPU_SYSAD[20]	CPU_SYSAD[21]	U
V	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				NC	CPU_SYSAD[16]	CPU_SYSAD[11]	CPU_SYSAD[12]	CPU_SYSAD[13]	CPU_SYSAD[14]	V
W	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[15]	VSS	CPU_SYSAD[7]	CPU_SYSAD[8]	CPU_SYSAD[9]	CPU_SYSAD[10]	W
Y	VSS	VSS	VSS	VSS			VDD_CPU	HSTL_VREF0				CPU_SYSAD[6]	CPU_SYSADC[0]	CPU_SYSAD[2]	CPU_SYSAD[3]	CPU_SYSAD[4]	CPU_SYSAD[5]	Y
AA	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[0]	VSS	NC	NC	NC	CPU_SYSAD[1]	AA
AB							VDD_CPU	VDD_CORE				NC	NC	NC	NC	NC	NC	AB
AC							VDD_V33	VDD_CORE				VSS	NC	NC	NC	NC	NC	AC
AD	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_CORE	VDD_CORE				NC	NC	NC	NC	NC	NC	AD
AE	VDD_CORE	DLL0_VDDAH	DLL0_VSSA	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	NC				NC	NC	VSS	NC	NC	NC	AE
AF												NC	NC	NC	NC	NC	NC	AF
AG												CPU_CAL	NC	NC	NC	NC	NC	AG
AH												MPP[17]	MPP[22]	MPP[30]	MPP[31]	NC	NC	AH
AJ	PCI0_AD[17]	NC	VSS	PCI0_AD[11]	PCI0_AD[7]	PCI0_VREF	VSS	NC	NC	PCI0_AD[55]	PCI0_AD[47]	PCI0_AD[39]	PCI0_HS	MPP[26]	MPP[27]	MPP[28]	MPP[29]	AJ
AK	VSS	PCI0_IRDYn	PCI0_PERRn	PCI0_M66EN	PCI0_AD[8]	PCI0_REQ64n	PCI0_CBEn[6]	VSS	PCI0_AD[57]	PCI0_AD[53]	PCI0_AD[41]	PCI0_AD[33]	PCI0_CAL	MPP[21]	MPP[23]	MPP[24]	MPP[25]	AK
AL	PCI0_AD[20]	PCI0_CBEn[2]	PCI0_STOPn	PCI0_AD[15]	PCI0_AD[10]	PCI0_AD[6]	PCI0_AD[2]	PCI0_CBEn[7]	PCI0_AD[63]	PCI0_AD[59]	PCI0_AD[54]	PCI0_AD[49]	PCI0_AD[44]	PCI0_AD[38]	PCI0_AD[34]	MPP[19]	MPP[20]	AL
AM	PCI0_AD[19]	PCI0_FRAMEn	PCI0_SERRn	PCI0_AD[14]	PCI0_AD[9]	PCI0_AD[5]	PCI0_AD[1]	PCI0_CBEn[5]	PCI0_AD[62]	VSS	PCI0_AD[52]	PCI0_AD[48]	PCI0_AD[43]	PCI0_AD[37]	PCI0_AD[32]	MPP[16]	MPP[18]	AM
AN	PCI0_AD[18]	PCI0_TRDYn	PCI0_PAR	PCI0_AD[13]	VSS	PCI0_AD[4]	PCI0_AD[0]	PCI0_CBEn[4]	PCI0_AD[61]	PCI0_AD[58]	PCI0_AD[51]	PCI0_AD[46]	PCI0_AD[42]	PCI0_AD[36]	PCI0_ENUMn	PCI0_64ENn	VSS	AN
AP	PCI0_AD[16]	PCI0_DEVSELn	PCI0_CBEn[1]	PCI0_AD[12]	PCI0_CBEn[0]	PCI0_AD[3]	PCI0_ACK64n	PCI0_PAR64	PCI0_AD[60]	PCI0_AD[56]	PCI0_AD[50]	PCI0_AD[45]	PCI0_AD[40]	PCI0_AD[35]	PCI0_LED	VSS		AP
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Table 19: MV64440 Pinout Sorted by Signal Name

Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#
CLK125	U2	CPU_SYSAD[37]	G30	CPU_TCDOEn	G32	DEV_DP[1]	J3	M_DA[5]	B8
CPU_CAL	AG29	CPU_SYSAD[38]	F33	CPU_TCMATCH	J33	DEV_DP[2]	L6	M_DA[6]	A8
CPU_INTn[0]	G31	CPU_SYSAD[39]	F34	CPU_TCTCEn	G29	DEV_DP[3]	M1	M_DA[7]	B6
CPU_INTn[1]	H33	CPU_SYSAD[40]	E33	CPU_TCWORD[(	L34	DEV_READYn	B2	M_DA[8]	D6
CPU_PACKn	G33	CPU_SYSAD[41]	E34	CPU_TCWORD[1	K31	DEV_WEn[0]	C2	M_DA[9]	D7
CPU_PREQn	H29	CPU_SYSAD[42]	F30	CPU_VALID_INn	N31	DEV_WEn[1]	C1	M_DA[10]	C9
CPU_RELEASEn	J32	CPU_SYSAD[43]	D31	CPU_VALID_OU	J31	DEV_WEn[2]	D3	M_DA[11]	C7
CPU_RSSWAPn	H30	CPU_SYSAD[44]	D32	DEV_AD[0]/DEV_	F4	DEV_WEn[3]	E5	M_DA[12]	B7
CPU_SYSAD[0]	AA29	CPU_SYSAD[45]	D33	DEV_AD[1]/DEV_	F3	DLL0_VDDAH	AE19	M_DA[13]	F28
CPU_SYSAD[1]	AA34	CPU_SYSAD[46]	D34	DEV_AD[2]	G6	DLL0_VSSA	AE20	M_DCAL	C6
CPU_SYSAD[2]	Y31	CPU_SYSAD[47]	C33	DEV_AD[3]	F2	DLL1_VDDAH	AE10	M_DM[0]	B11
CPU_SYSAD[3]	Y32	CPU_SYSAD[48]	C34	DEV_AD[4]	H5	DLL1_VSSA	AE11	M_DM[1]	B13
CPU_SYSAD[4]	Y33	CPU_SYSAD[49]	E31	DEV_AD[5]	F1	ETHER_CAL	U6	M_DM[2]	A15
CPU_SYSAD[5]	Y34	CPU_SYSAD[50]	B33	DEV_AD[6]	G4	HSTL_VREF0	Y25	M_DM[3]	A17
CPU_SYSAD[6]	Y29	CPU_SYSAD[51]	C32	DEV_AD[7]	G3	HSTL_VREF1	N25	M_DM[4]	A21
CPU_SYSAD[7]	W31	CPU_SYSAD[52]	B32	DEV_AD[8]	G2	JT_CLK	B3	M_DM[5]	F22
CPU_SYSAD[8]	W32	CPU_SYSAD[53]	A32	DEV_AD[9]	G1	JT_DI	E6	M_DM[6]	D24
CPU_SYSAD[9]	W33	CPU_SYSAD[54]	C31	DEV_AD[10]	H4	JT_DO	A4	M_DM[7]	C26
CPU_SYSAD[10]	W34	CPU_SYSAD[55]	B31	DEV_AD[11]	J5	JT_MS	A3	M_DM[8]	B19
CPU_SYSAD[11]	V31	CPU_SYSAD[56]	A31	DEV_AD[12]	H2	JT_RSTn	F6	M_DQ[0]	C10
CPU_SYSAD[12]	V32	CPU_SYSAD[57]	E29	DEV_AD[13]	J6	M_ACAL	E7	M_DQ[1]	D10
CPU_SYSAD[13]	V33	CPU_SYSAD[58]	D30	DEV_AD[14]	H1	M_BA[0]	B27	M_DQ[2]	E10
CPU_SYSAD[14]	V34	CPU_SYSAD[59]	D29	DEV_AD[15]	J4	M_BA[1]	D27	M_DQ[3]	F10
CPU_SYSAD[15]	W29	CPU_SYSAD[60]	C30	DEV_AD[16]	J2	M_CASn	E27	M_DQ[4]	C11
CPU_SYSAD[16]	V30	CPU_SYSAD[61]	B30	DEV_AD[17]	J1	M_CB[0]	A18	M_DQ[5]	D11
CPU_SYSAD[17]	U30	CPU_SYSAD[62]	A30	DEV_AD[18]	K4	M_CB[1]	F17	M_DQ[6]	E11
CPU_SYSAD[18]	U31	CPU_SYSAD[63]	C29	DEV_AD[19]	K3	M_CB[2]	B18	M_DQ[7]	A12
CPU_SYSAD[19]	U32	CPU_SYSADC[0]	Y30	DEV_AD[20]	K6	M_CB[3]	E18	M_DQ[8]	B12
CPU_SYSAD[20]	U33	CPU_SYSADC[1]	U29	DEV_AD[21]	K2	M_CB[4]	C19	M_DQ[9]	C12
CPU_SYSAD[21]	U34	CPU_SYSADC[2]	T29	DEV_AD[22]	K5	M_CB[5]	E19	M_DQ[10]	D12
CPU_SYSAD[22]	T31	CPU_SYSADC[3]	R34	DEV_AD[23]	K1	M_CB[6]	F19	M_DQ[11]	E12
CPU_SYSAD[23]	T32	CPU_SYSADC[4]	E32	DEV_AD[24]	L4	M_CB[7]	A20	M_DQ[12]	D13
CPU_SYSAD[24]	T33	CPU_SYSADC[5]	E30	DEV_AD[25]	L5	M_CKE0	B10	M_DQ[13]	E13
CPU_SYSAD[25]	T34	CPU_SYSADC[6]	F29	DEV_AD[26]	L3	M_CKE1	A10	M_DQ[14]	F13
CPU_SYSAD[26]	R31	CPU_SYSADC[7]	B29	DEV_AD[27]	L2	M_CLK_OUT	D9	M_DQ[15]	A14
CPU_SYSAD[27]	R29	CPU_SYSCMD[0	N33	DEV_AD[28]/DEV	L1	M_CLK_OUTn	E9	M_DQ[16]	B14
CPU_SYSAD[28]	R32	CPU_SYSCMD[1	N34	DEV_AD[29]/DEV	M4	M_CSn[0]	B28	M_DQ[17]	C14
CPU_SYSAD[29]	R30	CPU_SYSCMD[2	M31	DEV_AD[30]/DEV	M3	M_CSn[1]	C28	M_DQ[18]	D14
CPU_SYSAD[30]	R33	CPU_SYSCMD[3	N30	DEV_AD[31]/DEV	M2	M_CSn[2]	D28	M_DQ[19]	E14
CPU_SYSAD[31]	P30	CPU_SYSCMD[4	M32	DEV_ALE	E2	M_CSn[3]	E28	M_DQ[20]	B15
CPU_SYSAD[32]	P31	CPU_SYSCMD[5	M29	DEV_BADR[0]	D2	M_DA[0]	A9	M_DQ[21]	C15
CPU_SYSAD[33]	P32	CPU_SYSCMD[6	M33	DEV_BADR[1]	F5	M_DA[1]	B9	M_DQ[22]	D15
CPU_SYSAD[34]	P33	CPU_SYSCMD[7	M34	DEV_BADR[2]	E3	M_DA[2]	F8	M_DQ[23]	E15
CPU_SYSAD[35]	P34	CPU_SYSCMD[8	N29	DEV_CSTIMINGn	E1	M_DA[3]	E8	M_DQ[24]	A16
CPU_SYSAD[36]	G34	CPU_SYSRDY_C	L30	DEV_DP[0]	H6	M_DA[4]	D8	M_DQ[25]	B16

Table 19: MV64440 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
M_DQ[26]	C16
M_DQ[27]	E16
M_DQ[28]	B17
M_DQ[29]	C17
M_DQ[30]	D17
M_DQ[31]	E17
M_DQ[32]	B20
M_DQ[33]	C20
M_DQ[34]	D20
M_DQ[35]	E20
M_DQ[36]	B21
M_DQ[37]	C21
M_DQ[38]	D21
M_DQ[39]	E21
M_DQ[40]	F21
M_DQ[41]	A22
M_DQ[42]	B22
M_DQ[43]	C22
M_DQ[44]	A23
M_DQ[45]	B23
M_DQ[46]	C23
M_DQ[47]	D23
M_DQ[48]	E23
M_DQ[49]	F23
M_DQ[50]	A24
M_DQ[51]	B24
M_DQ[52]	E24
M_DQ[53]	F24
M_DQ[54]	A25
M_DQ[55]	B25
M_DQ[56]	C25
M_DQ[57]	D25
M_DQ[58]	E25
M_DQ[59]	A26
M_DQ[60]	D26
M_DQ[61]	E26
M_DQ[62]	F26
M_DQ[63]	A27
M_DQS[0]	A11
M_DQS[1]	A13
M_DQS[2]	F14
M_DQS[3]	F16
M_DQS[4]	F20
M_DQS[5]	E22
M_DQS[6]	C24

Signal Name	Ball#
M_DQS[7]	B26
M_DQS[8]	A19
M_RASn	F27
M_SSTLVREF_0	K20
M_SSTLVREF_1	K14
M_STARTBURST	D18
M_STARTBURST	C18
M_WEn	A28
MDC	U3
MDIO	U5
MPP[0]	AD5
MPP[1]	AC3
MPP[2]	AC2
MPP[3]	AC1
MPP[4]	AD4
MPP[5]	AD3
MPP[6]	AD2
MPP[7]	AD1
MPP[8]	AE4
MPP[9]	AE3
MPP[10]	AE6
MPP[11]	AE2
MPP[12]	AE1
MPP[13]	AF4
MPP[14]	AF3
MPP[15]	AF2
MPP[16]	AM33
MPP[17]	AH29
MPP[18]	AM34
MPP[19]	AL33
MPP[20]	AL34
MPP[21]	AK31
MPP[22]	AH30
MPP[23]	AK32
MPP[24]	AK33
MPP[25]	AK34
MPP[26]	AJ31
MPP[27]	AJ32
MPP[28]	AJ33
MPP[29]	AJ34
MPP[30]	AH31
MPP[31]	AH32
NC	A6
NC	A7
NC	B5

Signal Name	Ball#
NC	C3
NC	C4
NC	D1
NC	D5
NC	E4
NC	F11
NC	F15
NC	J29
NC	J30
NC	K30
NC	K32
NC	K33
NC	K34
NC	L29
NC	L31
NC	L32
NC	L33
NC	N32
NC	V29
NC	AA6
NC	AA31
NC	AA32
NC	AA33
NC	AB29
NC	AB30
NC	AB31
NC	AB32
NC	AB33
NC	AB34
NC	AC6
NC	AC30
NC	AC31
NC	AC32
NC	AC33
NC	AC34
NC	AD29
NC	AD30
NC	AD31
NC	AD32
NC	AD33
NC	AD34
NC	AE25
NC	AE29
NC	AE30
NC	AE32

Signal Name	Ball#
NC	AE33
NC	AE34
NC	AF29
NC	AF30
NC	AF31
NC	AF32
NC	AF33
NC	AF34
NC	AG30
NC	AG31
NC	AG32
NC	AG33
NC	AG34
NC	AH33
NC	AH34
NC	AJ19
NC	AJ25
NC	AJ26
P0_COL	M6
P0_CRS	R3
P0_RXCLK	R1
P0_RXD[0]	T4
P0_RXD[1]	R6
P0_RXD[2]	T3
P0_RXD[3]	T2
P0_RXD[4]	T1
P0_RXD[5]	T5
P0_RXD[6]	U4
P0_RXD[7]	T6
P0_RXDV	R5
P0_RXERR	R2
P0_TXCLK	R4
P0_TXCLK_OUT	P2
P0_TXD[0]	N5
P0_TXD[1]	P3
P0_TXD[2]	P4
P0_TXD[3]	N1
P0_TXD[4]	N2
P0_TXD[5]	N3
P0_TXD[6]	M5
P0_TXD[7]	N4
P0_TXEN	P6
P0_TXERR	P1
P1_COL	V3
P1_CRS	Y1

Signal Name	Ball#
FIFOCLK	V4
P1_RXCLK	Y5
P1_RXD[0]	AA2
P1_RXD[1]	AA1
P1_RXD[2]	AA5
P1_RXD[3]	AB4
P1_RXD[4]	AB6
P1_RXD[5]	AB3
P1_RXD[6]	AB5
P1_RXD[7]	AB2
P1_RXDV	AA3
P1_RXERR	AA4
P1_TXCLK	Y2
P1_TXCLK_OUT	Y6
P1_TXD[0]	W1
P1_TXD[1]	W5
P1_TXD[2]	W2
P1_TXD[3]	W3
P1_TXD[4]	W4
P1_TXD[5]	V1
P1_TXD[6]	V2
P1_TXD[7]	V5
P1_TXEN	Y4
P1_TXERR	Y3
PCI0_64ENn	AN33
PCI0_ACK64n	AP24
PCI0_AD[0]	AN24
PCI0_AD[1]	AM24
PCI0_AD[2]	AL24
PCI0_AD[3]	AP23
PCI0_AD[4]	AN23
PCI0_AD[5]	AM23
PCI0_AD[6]	AL23
PCI0_AD[10]	AL22
PCI0_AD[11]	AJ21
PCI0_AD[12]	AP21
PCI0_AD[13]	AN21
PCI0_AD[14]	AM21
PCI0_AD[15]	AL21
PCI0_AD[16]	AP18
PCI0_AD[17]	AJ18
PCI0_AD[18]	AN18
PCI0_AD[19]	AM18
PCI0_AD[20]	AL18
PCI0_AD[21]	AP17

Table 19: MV64440 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
PCI0_AD[22]	AN17
PCI0_AD[23]	AM17
PCI0_AD[24]	AP16
PCI0_AD[25]	AN16
PCI0_AD[26]	AM16
PCI0_AD[27]	AJ16
PCI0_AD[28]	AL16
PCI0_AD[29]	AK16
PCI0_AD[30]	AP15
PCI0_AD[31]	AN15
PCI0_AD[32]	AM32
PCI0_AD[33]	AK29
PCI0_AD[34]	AL32
PCI0_AD[35]	AP31
PCI0_AD[36]	AN31
PCI0_AD[37]	AM31
PCI0_AD[38]	AL31
PCI0_AD[39]	AJ29
PCI0_AD[40]	AP30
PCI0_AD[41]	AK28
PCI0_AD[42]	AN30
PCI0_AD[43]	AM30
PCI0_AD[44]	AL30
PCI0_AD[45]	AP29
PCI0_AD[46]	AN29
PCI0_AD[47]	AJ28
PCI0_AD[48]	AM29
PCI0_AD[49]	AL29
PCI0_AD[50]	AP28
PCI0_AD[51]	AN28
PCI0_AD[52]	AM28
PCI0_AD[53]	AK27
PCI0_AD[54]	AL28
PCI0_AD[55]	AJ27
PCI0_AD[56]	AP27
PCI0_AD[57]	AK26
PCI0_AD[58]	AN27
PCI0_AD[59]	AL27
PCI0_AD[60]	AP26
PCI0_AD[61]	AN26
PCI0_AD[62]	AM26
PCI0_AD[63]	AL26
PCI0_AD[7]	AJ22
PCI0_AD[8]	AK22
PCI0_AD[9]	AM22

Signal Name	Ball#
PCI0_CAL	AK30
PCI0_CBEn[0]	AP22
PCI0_CBEn[1]	AP20
PCI0_CBEn[2]	AL19
PCI0_CBEn[3]	AK17
PCI0_CBEn[4]	AN25
PCI0_CBEn[5]	AM25
PCI0_CBEn[6]	AK24
PCI0_CBEn[7]	AL25
PCI0_CLK	AP14
PCI0_DEVSELn	AP19
PCI0_ENUMn	AN32
PCI0_FRAMEn	AM19
PCI0_GNTn	AL15
PCI0_HS	AJ30
PCI0_IDSEL	AL17
PCI0_INTn	AJ15
PCI0_IRDYn	AK19
PCI0_LED	AP32
PCI0_M66EN	AK21
PCI0_PAR	AN20
PCI0_PAR64	AP25
PCI0_PERRn	AK20
PCI0_REQ64n	AK23
PCI0_REQn	AM15
PCI0_RSTn	AK15
PCI0_SERRn	AM20
PCI0_STOPn	AL20
PCI0_TRDYn	AN19
PCI0_VREF	AJ23
PCI1_ACK64n	AP7
PCI1_AD[0]	AM7
PCI1_AD[1]	AK7
PCI1_AD[2]	AL7
PCI1_AD[3]	AP6
PCI1_AD[4]	AN6
PCI1_AD[5]	AM6
PCI1_AD[6]	AL6
PCI1_AD[7]	AP5
PCI1_AD[8]	AM5
PCI1_AD[9]	AL5
PCI1_AD[10]	AP4
PCI1_AD[11]	AN4
PCI1_AD[12]	AM4
PCI1_AD[13]	AK5

Signal Name	Ball#
PCI1_AD[14]	AP3
PCI1_AD[15]	AK6
PCI1_AD[16]	AL3
PCI1_AD[17]	AK1
PCI1_AD[18]	AK2
PCI1_AD[19]	AK3
PCI1_AD[20]	AH6
PCI1_AD[21]	AK4
PCI1_AD[22]	AJ1
PCI1_AD[23]	AJ2
PCI1_AD[24]	AJ4
PCI1_AD[25]	AH1
PCI1_AD[26]	AG5
PCI1_AD[27]	AH2
PCI1_AD[28]	AH3
PCI1_AD[29]	AH4
PCI1_AD[30]	AF6
PCI1_AD[31]	AG1
PCI1_AD[32]	AN14
PCI1_AD[33]	AJ13
PCI1_AD[34]	AM14
PCI1_AD[35]	AL14
PCI1_AD[36]	AK14
PCI1_AD[37]	AK12
PCI1_AD[38]	AJ14
PCI1_AD[39]/P2_	AP13
PCI1_AD[40]/P2_	AN13
PCI1_AD[41]/P2_	AM13
PCI1_AD[42]/P2_	AL13
PCI1_AD[43]/P2_	AJ12
PCI1_AD[44]/P2_	AP12
PCI1_AD[45]/P2_	AN12
PCI1_AD[46]/P2_	AM12
PCI1_AD[47]/P2_	AJ11
PCI1_AD[48]/P2_	AL12
PCI1_AD[49]/P2_	AP11
PCI1_AD[50]/P2_	AN11
PCI1_AD[51]/P2_	AK10
PCI1_AD[52]/P2_	AM11
PCI1_AD[53]/P2_	AL11
PCI1_AD[54]/P2_	AP10
PCI1_AD[55]/P2_	AN10
PCI1_AD[56]/P2_	AM10
PCI1_AD[57]/P2_	AJ10
PCI1_AD[58]/P2_	AL10

Signal Name	Ball#
PCI1_AD[59]/P2_	AJ9
PCI1_AD[60]/P2_	AP9
PCI1_AD[61]/P2_	AN9
PCI1_AD[62]/P2_	AM9
PCI1_AD[63]/P2_	AL9
PCI1_CAL	AK13
PCI1_CBEn[0]	AN5
PCI1_CBEn[1]	AN3
PCI1_CBEn[2]	AL2
PCI1_CBEn[3]	AJ3
PCI1_CBEn[4]	AK8
PCI1_CBEn[5]	AN8
PCI1_CBEn[6]	AM8
PCI1_CBEn[7]	AL8
PCI1_CLK	AF1
PCI1_DEVSELn	AM1
PCI1_FRAMEn	AL1
PCI1_GNTn	AG3
PCI1_IDSEL	AG6
PCI1_INTn	AG4
PCI1_IRDYn	AM2
PCI1_M66EN	AJ7
PCI1_PAR	AJ6
PCI1_PAR64	AP8
PCI1_PERRn	AN2
PCI1_REQ64n	AJ8
PCI1_REQn	AG2
PCI1_RSTn	AF5
PCI1_SERRn	AM3
PCI1_STOPn	AJ5
PCI1_TRDYn	AH5
PCI1_VREF	AN7
PLL0_VDDAH	K24
PLL0_VSSA	L25
PLL1_VDDAH	K10
PLL1_VSSA	K11
RGMII VREF	V10
SCK	AC5
SDA	AC4
SYS_CLK	A29
SYSRSTn	F7
TCLK	A5
V_ETH0	T11
V_ETH0	U11
V_ETH1	V11

Signal Name	Ball#
V_ETH1	W11
VDD_CLK	K23
VDD_CORE	K12
VDD_CORE	K13
VDD_CORE	K15
VDD_CORE	K16
VDD_CORE	K17
VDD_CORE	K18
VDD_CORE	K19
VDD_CORE	K21
VDD_CORE	K22
VDD_CORE	K25
VDD_CORE	L10
VDD_CORE	L11
VDD_CORE	L24
VDD_CORE	M10
VDD_CORE	M25
VDD_CORE	N10
VDD_CORE	P10
VDD_CORE	P25
VDD_CORE	R10
VDD_CORE	R25
VDD_CORE	T10
VDD_CORE	T25
VDD_CORE	U10
VDD_CORE	U25
VDD_CORE	V25
VDD_CORE	W10
VDD_CORE	W25
VDD_CORE	Y10
VDD_CORE	AA10
VDD_CORE	AA25
VDD_CORE	AB10
VDD_CORE	AB25
VDD_CORE	AC10
VDD_CORE	AC25
VDD_CORE	AD10
VDD_CORE	AD11
VDD_CORE	AD24
VDD_CORE	AD25
VDD_CORE	AE12
VDD_CORE	AE13
VDD_CORE	AE14
VDD_CORE	AE15
VDD_CORE	AE16

Table 19: MV64440 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
VDD_CORE	AE17
VDD_CORE	AE18
VDD_CORE	AE21
VDD_CORE	AE22
VDD_CORE	AE23
VDD_CORE	AE24
VDD_CPU	M24
VDD_CPU	N24
VDD_CPU	P24
VDD_CPU	R24
VDD_CPU	T24
VDD_CPU	U24
VDD_CPU	V24
VDD_CPU	W24
VDD_CPU	Y24
VDD_CPU	AA24
VDD_CPU	AB24
VDD_DRAM	L12
VDD_DRAM	L13
VDD_DRAM	L14
VDD_DRAM	L15
VDD_DRAM	L16
VDD_DRAM	L17
VDD_DRAM	L18
VDD_DRAM	L19
VDD_DRAM	L20
VDD_DRAM	L21
VDD_DRAM	L22
VDD_DRAM	L23
VDD_V33	M11
VDD_V33	N11
VDD_V33	P11
VDD_V33	R11
VDD_V33	Y11
VDD_V33	AA11
VDD_V33	AB11
VDD_V33	AC11
VDD_V33	AC24
VDD_V33	AD12
VDD_V33	AD13
VDD_V33	AD14
VDD_V33	AD15
VDD_V33	AD16
VDD_V33	AD17
VDD_V33	AD18

Signal Name	Ball#
VDD_V33	AD19
VDD_V33	AD20
VDD_V33	AD21
VDD_V33	AD22
VDD_V33	AD23
VSS	A2
VSS	A33
VSS	B1
VSS	B4
VSS	B34
VSS	C5
VSS	C8
VSS	C13
VSS	C27
VSS	D4
VSS	D16
VSS	D19
VSS	D22
VSS	F9
VSS	F12
VSS	F18
VSS	F25
VSS	F31
VSS	F32
VSS	G5
VSS	H3
VSS	H31
VSS	H32
VSS	H34
VSS	J34
VSS	K29
VSS	M30
VSS	N6
VSS	P5
VSS	P14
VSS	P15
VSS	P16
VSS	P17
VSS	P18
VSS	P19
VSS	P20
VSS	P21
VSS	P29
VSS	R14
VSS	R15

Signal Name	Ball#
VSS	R16
VSS	R17
VSS	R18
VSS	R19
VSS	R20
VSS	R21
VSS	T14
VSS	T15
VSS	T16
VSS	T17
VSS	T18
VSS	T19
VSS	T20
VSS	T21
VSS	T30
VSS	U1
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	U18
VSS	U19
VSS	U20
VSS	U21
VSS	V6
VSS	V14
VSS	V15
VSS	V16
VSS	V17
VSS	V18
VSS	V19
VSS	V20
VSS	V21
VSS	W6
VSS	W14
VSS	W15
VSS	W16
VSS	W17
VSS	W18
VSS	W19
VSS	W20
VSS	W21
VSS	W30
VSS	Y14
VSS	Y15

Signal Name	Ball#
VSS	Y16
VSS	Y17
VSS	Y18
VSS	Y19
VSS	Y20
VSS	Y21
VSS	AA14
VSS	AA15
VSS	AA16
VSS	AA17
VSS	AA18
VSS	AA19
VSS	AA20
VSS	AA21
VSS	AA30
VSS	AB1
VSS	AC29
VSS	AD6
VSS	AE5
VSS	AE31
VSS	AJ17
VSS	AJ20
VSS	AJ24
VSS	AK9
VSS	AK11
VSS	AK18
VSS	AK25
VSS	AL4
VSS	AM27
VSS	AN1
VSS	AN22
VSS	AN34
VSS	AP2
VSS	AP33

Section 6. MV64441 Pinout Map and Table, 844 Pin BGA

Figure 9: MV64441 Pinout Map (Top View, Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A		VSS	JT_MS	JT_DO	TCLK	NC	NC	M_DA[6]	M_DA[0]	M_CKE1	M_DQS[0]	M_DQ[7]	M_DQS[1]	M_DQ[15]	M_DM[2]	M_DQ[24]	M_DM[3]	A
B	VSS	DEV_READYn	JT_CLK	VSS	NC	M_DA[7]	M_DA[12]	M_DA[5]	M_DA[1]	M_CKE0	M_DM[0]	M_DQ[8]	M_DM[1]	M_DQ[16]	M_DQ[20]	M_DQ[25]	M_DQ[28]	B
C	DEV_WEn[1]	DEV_WEn[0]	NC	NC	VSS	M_DCAL	M_DA[11]	VSS	M_DA[10]	M_DQ[0]	M_DQ[4]	M_DQ[9]	VSS	M_DQ[17]	M_DQ[21]	M_DQ[26]	M_DQ[29]	C
D	NC	DEV_BADR[0]	DEV_WEn[2]	VSS	NC	M_DA[8]	M_DA[9]	M_DA[4]	M_CLK_OUT	M_DQ[1]	M_DQ[5]	M_DQ[10]	M_DQ[12]	M_DQ[18]	M_DQ[22]	VSS	M_DQ[30]	D
E	DEV_CSTIMINGn	DEV_ALE	DEV_BADR[2]	NC	DEV_WEn[3]	JT_DI	M_ACAL	M_DA[3]	M_CLK_OUTn	M_DQ[2]	M_DQ[6]	M_DQ[11]	M_DQ[13]	M_DQ[19]	M_DQ[23]	M_DQ[27]	M_DQ[31]	E
F	DEV_AD[5]	DEV_AD[3]	DEV_AD[1]/DEV_RWn	DEV_AD[0]/DEV_BOOTCSn	DEV_BADR[1]	JT_RSTn	SYSRSTn	M_DA[2]	VSS	M_DQ[3]	NC	VSS	M_DQ[14]	M_DQS[2]	NC	M_DQS[3]	M_CB[1]	F
G	DEV_AD[9]	DEV_AD[8]	DEV_AD[7]	DEV_AD[6]	VSS	DEV_AD[2]												G
H	DEV_AD[14]	DEV_AD[12]	VSS	DEV_AD[10]	DEV_AD[4]	DEV_DP[0]				MV64441								H
J	DEV_AD[17]	DEV_AD[16]	DEV_DP[1]	DEV_AD[15]	DEV_AD[11]	DEV_AD[13]												J
K	DEV_AD[23]	DEV_AD[21]	DEV_AD[19]	DEV_AD[18]	DEV_AD[22]	DEV_AD[20]				PLL1_VDDAH	PLL1_VSSA	VDD_CORE	VDD_CORE	M_SSTLVREF_1	VDD_CORE	VDD_CORE	VDD_CORE	K
L	DEV_AD[28]/DEV_CSn[0]	DEV_AD[27]	DEV_AD[26]	DEV_AD[24]	DEV_AD[25]	DEV_DP[2]				VDD_CORE	VDD_CORE	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	L
M	DEV_DP[3]	DEV_AD[31]/DEV_CSn[3]	DEV_AD[30]/DEV_CSn[2]	DEV_AD[29]/DEV_CSn[1]	P0_TXD[6]	P0_COL				VDD_CORE	VDD_V33							M
N	P0_TXD[3]	P0_TXD[4]	P0_TXD[5]	P0_TXD[7]	P0_TXD[0]	VSS				VDD_CORE	VDD_V33							N
P	P0_TXERR	P0_TXCLK_OUT	P0_TXD[1]	P0_TXD[2]	VSS	P0_TXEN				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	P
R	P0_RXCLK	P0_RXERR	P0_CRS	P0_TXCLK	P0_RXDV	P0_RXD[1]				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	R
T	P0_RXD[4]	P0_RXD[3]	P0_RXD[2]	P0_RXD[0]	P0_RXD[5]	P0_RXD[7]				VDD_CORE	V_ETH0			VSS	VSS	VSS	VSS	T
U	VSS	CLK125	MDC	P0_RXD[6]	MDIO	ETHER_CAL				VDD_CORE	V_ETH0			VSS	VSS	VSS	VSS	U
V	P1_TXD[5]	P1_TXD[6]	P1_COL	FIFOCLK	P1_TXD[7]	VSS				RGMII VREF	V_ETH1			VSS	VSS	VSS	VSS	V
W	P1_TXD[0]	P1_TXD[2]	P1_TXD[3]	P1_TXD[4]	P1_TXD[1]	VSS				VDD_CORE	V_ETH1			VSS	VSS	VSS	VSS	W
Y	P1_CRS	P1_TXCLK	P1_TXERR	P1_TXEN	P1_RXCLK	P1_TXCLK_OUT				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	Y
AA	P1_RXD[1]	P1_RXD[0]	P1_RXDV	P1_RXERR	P1_RXD[2]	NC				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	AA
AB	VSS	P1_RXD[7]	P1_RXD[5]	P1_RXD[3]	P1_RXD[6]	P1_RXD[4]				VDD_CORE	VDD_V33							AB
AC	MPP[3]	MPP[2]	MPP[1]	SDA	SCK	NC				VDD_CORE	VDD_V33							AC
AD	MPP[7]	MPP[6]	MPP[5]	MPP[4]	MPP[0]	VSS				VDD_CORE	VDD_CORE	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	AD
AE	MPP[12]	MPP[11]	MPP[9]	MPP[8]	VSS	MPP[10]				DLL1_VDDAH	DLL1_VSSA	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	AE
AF	PCI1_CLK	MPP[15]	MPP[14]	MPP[13]	PCI1_RSTn	PCI1_AD[30]												AF
AG	PCI1_AD[31]	PCI1_REQn	PCI1_GNTn	PCI1_INTn	PCI1_AD[26]	PCI1_IDSEL												AG
AH	PCI1_AD[25]	PCI1_AD[27]	PCI1_AD[28]	PCI1_AD[29]	PCI1_TRDYn	PCI1_AD[20]												AH
AJ	PCI1_AD[22]	PCI1_AD[23]	PCI1_CBEn[3]	PCI1_AD[24]	PCI1_STOPn	PCI1_PAR	PCI1_M66EN	Pull Up	NC	NC	NC	NC	NC	NC	PCI0_INTn	PCI0_AD[27]	VSS	AJ
AK	PCI1_AD[17]	PCI1_AD[18]	PCI1_AD[19]	PCI1_AD[21]	PCI1_AD[13]	PCI1_AD[15]	PCI1_AD[1]	NC	VSS	NC	VSS	NC	PCI1_CAL	NC	PCI0_RSTn	PCI0_AD[29]	PCI0_CBEn[3]	AK
AL	PCI1_FRAMEn	PCI1_CBEn[2]	PCI1_AD[16]	VSS	PCI1_AD[9]	PCI1_AD[6]	PCI1_AD[2]	NC	NC	NC	NC	NC	NC	NC	PCI0_GNTn	PCI0_AD[28]	PCI0_IDSEL	AL
AM	PCI1_DEVSELn	PCI1_IRDYn	PCI1_SERRn	PCI1_AD[12]	PCI1_AD[8]	PCI1_AD[5]	PCI1_AD[0]	NC	NC	NC	NC	NC	NC	NC	PCI0_REQn	PCI0_AD[26]	PCI0_AD[23]	AM
AN	VSS	PCI1_PERRn	PCI1_CBEn[1]	PCI1_AD[11]	PCI1_CBEn[0]	PCI1_AD[4]	PCI1_VREF	NC	NC	NC	NC	NC	NC	NC	PCI0_AD[31]	PCI0_AD[25]	PCI0_AD[22]	AN
AP		VSS	PCI1_AD[14]	PCI1_AD[10]	PCI1_AD[7]	PCI1_AD[3]	Pull Up	NC	NC	NC	NC	NC	NC	PCI0_CLK	PCI0_AD[30]	PCI0_AD[24]	PCI0_AD[21]	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 10: MV64441 Pinout Map (Top View, Right Side)

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	M_CB[0]	M_DQS[8]	M_CB[7]	M_DM[4]	M_DQ[41]	M_DQ[44]	M_DQ[50]	M_DQ[54]	M_DQ[59]	M_DQ[63]	M_WEn	SYS_CLK	CPU_SYSAD[62]	CPU_SYSAD[56]	CPU_SYSAD[53]	VSS		A
B	M_CB[2]	M_DM[8]	M_DQ[32]	M_DQ[36]	M_DQ[42]	M_DQ[45]	M_DQ[51]	M_DQ[55]	M_DQS[7]	M_BA[0]	M_CSn[0]	CPU_SYSADC[7]	CPU_SYSAD[61]	CPU_SYSAD[55]	CPU_SYSAD[52]	CPU_SYSAD[50]	VSS	B
C	M_STARTBURST_IN	M_CB[4]	M_DQ[33]	M_DQ[37]	M_DQ[43]	M_DQ[46]	M_DQS[6]	M_DQ[56]	M_DM[7]	VSS	M_CSn[1]	CPU_SYSAD[63]	CPU_SYSAD[60]	CPU_SYSAD[54]	CPU_SYSAD[51]	CPU_SYSAD[47]	CPU_SYSAD[48]	C
D	M_STARTBURST	VSS	M_DQ[34]	M_DQ[38]	VSS	M_DQ[47]	M_DM[6]	M_DQ[57]	M_DQ[60]	M_BA[1]	M_CSn[2]	CPU_SYSAD[59]	CPU_SYSAD[58]	CPU_SYSAD[43]	CPU_SYSAD[44]	CPU_SYSAD[45]	CPU_SYSAD[46]	D
E	M_CB[3]	M_CB[5]	M_DQ[35]	M_DQ[39]	M_DQS[5]	M_DQ[48]	M_DQ[52]	M_DQ[58]	M_DQ[61]	M_CASn	M_CSn[3]	CPU_SYSAD[57]	CPU_SYSADC[5]	CPU_SYSAD[49]	CPU_SYSADC[4]	CPU_SYSAD[40]	CPU_SYSAD[41]	E
F	VSS	M_CB[6]	M_DQS[4]	M_DQ[40]	M_DM[5]	M_DQ[49]	M_DQ[53]	VSS	M_DQ[62]	M_RASn	M_DA[13]	CPU_SYSADC[6]	CPU_SYSAD[42]	VSS	VSS	CPU_SYSAD[38]	CPU_SYSAD[39]	F
G												CPU_TCTCEn	CPU_SYSAD[37]	CPU_INTn[0]	CPU_TCDOEn	CPU_PACKn	CPU_SYSAD[36]	G
H							MV64441					CPU_PREQn	CPU_RSSWAPn	VSS	VSS	CPU_INTn[1]	VSS	H
J												NC	NC	CPU_VALID_OUTn	CPU_RELEASEn	CPU_TCMATCH	VSS	J
K	VDD_CORE	VDD_CORE	M_SSTLVREF_0	VDD_CORE	VDD_CORE	VDD_CLK	PLL0_VDDAH	VDD_CORE				VSS	NC	CPU_TCWORD[1]	NC	NC	NC	K
L	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_CORE	PLL0_VSSA				NC	CPU_SYSRDY_OUTn	NC	NC	NC	CPU_TCWORD[0]	L
M							VDD_CPU	VDD_CORE				CPU_SYSCMD[5]	VSS	CPU_SYSCMD[2]	CPU_SYSCMD[4]	CPU_SYSCMD[6]	CPU_SYSCMD[7]	M
N							VDD_CPU	HSTL_VREF1				CPU_SYSCMD[8]	CPU_SYSCMD[3]	CPU_VALID_INn	NC	CPU_SYSCMD[0]	CPU_SYSCMD[1]	N
P	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				VSS	CPU_SYSAD[31]	CPU_SYSAD[32]	CPU_SYSAD[33]	CPU_SYSAD[34]	CPU_SYSAD[35]	P
R	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[27]	CPU_SYSAD[29]	CPU_SYSAD[26]	CPU_SYSAD[28]	CPU_SYSAD[30]	CPU_SYSADC[3]	R
T	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSADC[2]	VSS	CPU_SYSAD[22]	CPU_SYSAD[23]	CPU_SYSAD[24]	CPU_SYSAD[25]	T
U	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSADC[1]	CPU_SYSAD[17]	CPU_SYSAD[18]	CPU_SYSAD[19]	CPU_SYSAD[20]	CPU_SYSAD[21]	U
V	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				NC	CPU_SYSAD[16]	CPU_SYSAD[11]	CPU_SYSAD[12]	CPU_SYSAD[13]	CPU_SYSAD[14]	V
W	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[15]	VSS	CPU_SYSAD[7]	CPU_SYSAD[8]	CPU_SYSAD[9]	CPU_SYSAD[10]	W
Y	VSS	VSS	VSS	VSS			VDD_CPU	HSTL_VREF0				CPU_SYSAD[6]	CPU_SYSADC[0]	CPU_SYSAD[2]	CPU_SYSAD[3]	CPU_SYSAD[4]	CPU_SYSAD[5]	Y
AA	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[0]	VSS	NC	NC	NC	CPU_SYSAD[1]	AA
AB							VDD_CPU	VDD_CORE				NC	NC	NC	NC	NC	NC	AB
AC							VDD_V33	VDD_CORE				VSS	NC	NC	NC	NC	NC	AC
AD	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_CORE	VDD_CORE				NC	NC	NC	NC	NC	NC	AD
AE	VDD_CORE	DLL0_VDDAH	DLL0_VSSA	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	NC				NC	NC	VSS	NC	NC	NC	AE
AF												NC	NC	NC	NC	NC	NC	AF
AG												CPU_CAL	NC	NC	NC	NC	NC	AG
AH												MPP[17]	MPP[22]	MPP[30]	MPP[31]	NC	NC	AH
AJ	PCI0_AD[17]	NC	VSS	PCI0_AD[11]	PCI0_AD[7]	PCI0_VREF	VSS	NC	NC	NC	NC	NC	PCI0_HS	MPP[26]	MPP[27]	MPP[28]	MPP[29]	AJ
AK	VSS	PCI0_IRDYn	PCI0_PERRn	PCI0_M66EN	PCI0_AD[8]	Pull Up	NC	VSS	NC	NC	NC	NC	PCI0_CAL	MPP[21]	MPP[23]	MPP[24]	MPP[25]	AK
AL	PCI0_AD[20]	PCI0_CBEn[2]	PCI0_STOPn	PCI0_AD[15]	PCI0_AD[10]	PCI0_AD[6]	PCI0_AD[2]	NC	NC	NC	NC	NC	NC	NC	NC	MPP[19]	MPP[20]	AL
AM	PCI0_AD[19]	PCI0_FRAMEn	PCI0_SERRn	PCI0_AD[14]	PCI0_AD[9]	PCI0_AD[5]	PCI0_AD[1]	NC	NC	VSS	NC	NC	NC	NC	NC	MPP[16]	MPP[18]	AM
AN	PCI0_AD[18]	PCI0_TRDYn	PCI0_PAR	PCI0_AD[13]	VSS	PCI0_AD[4]	PCI0_AD[0]	NC	NC	NC	NC	NC	NC	NC	PCI0_ENUMn	Pull Up	VSS	AN
AP	PCI0_AD[16]	PCI0_DEVSELn	PCI0_CBEn[1]	PCI0_AD[12]	PCI0_CBEn[0]	PCI0_AD[3]	Pull Up	NC	NC	NC	NC	NC	NC	NC	PCI0_LED	VSS		AP
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Table 20: MV64441 Pinout Sorted by Signal Name

Signal Name	Ball#
CLK125	U2
CPU_CAL	AG29
CPU_INTn[0]	G31
CPU_INTn[1]	H33
CPU_PACKn	G33
CPU_PREQn	H29
CPU_RELEASEn	J32
CPU_RSSWAPn	H30
CPU_SYSAD[0]	AA29
CPU_SYSAD[1]	AA34
CPU_SYSAD[2]	Y31
CPU_SYSAD[3]	Y32
CPU_SYSAD[4]	Y33
CPU_SYSAD[5]	Y34
CPU_SYSAD[6]	Y29
CPU_SYSAD[7]	W31
CPU_SYSAD[8]	W32
CPU_SYSAD[9]	W33
CPU_SYSAD[10]	W34
CPU_SYSAD[11]	V31
CPU_SYSAD[12]	V32
CPU_SYSAD[13]	V33
CPU_SYSAD[14]	V34
CPU_SYSAD[15]	W29
CPU_SYSAD[16]	V30
CPU_SYSAD[17]	U30
CPU_SYSAD[18]	U31
CPU_SYSAD[19]	U32
CPU_SYSAD[20]	U33
CPU_SYSAD[21]	U34
CPU_SYSAD[22]	T31
CPU_SYSAD[23]	T32
CPU_SYSAD[24]	T33
CPU_SYSAD[25]	T34
CPU_SYSAD[26]	R31
CPU_SYSAD[27]	R29
CPU_SYSAD[28]	R32
CPU_SYSAD[29]	R30
CPU_SYSAD[30]	R33
CPU_SYSAD[31]	P30
CPU_SYSAD[32]	P31
CPU_SYSAD[33]	P32
CPU_SYSAD[34]	P33
CPU_SYSAD[35]	P34
CPU_SYSAD[36]	G34

Signal Name	Ball#
CPU_SYSAD[37]	G30
CPU_SYSAD[38]	F33
CPU_SYSAD[39]	F34
CPU_SYSAD[40]	E33
CPU_SYSAD[41]	E34
CPU_SYSAD[42]	F30
CPU_SYSAD[43]	D31
CPU_SYSAD[44]	D32
CPU_SYSAD[45]	D33
CPU_SYSAD[46]	D34
CPU_SYSAD[47]	C33
CPU_SYSAD[48]	C34
CPU_SYSAD[49]	E31
CPU_SYSAD[50]	B33
CPU_SYSAD[51]	C32
CPU_SYSAD[52]	B32
CPU_SYSAD[53]	A32
CPU_SYSAD[54]	C31
CPU_SYSAD[55]	B31
CPU_SYSAD[56]	A31
CPU_SYSAD[57]	E29
CPU_SYSAD[58]	D30
CPU_SYSAD[59]	D29
CPU_SYSAD[60]	C30
CPU_SYSAD[61]	B30
CPU_SYSAD[62]	A30
CPU_SYSAD[63]	C29
CPU_SYSADC[0]	Y30
CPU_SYSADC[1]	U29
CPU_SYSADC[2]	T29
CPU_SYSADC[3]	R34
CPU_SYSADC[4]	E32
CPU_SYSADC[5]	E30
CPU_SYSADC[6]	F29
CPU_SYSADC[7]	B29
CPU_SYSCMD[0	N33
CPU_SYSCMD[1	N34
CPU_SYSCMD[2	M31
CPU_SYSCMD[3	N30
CPU_SYSCMD[4	M32
CPU_SYSCMD[5	M29
CPU_SYSCMD[6	M33
CPU_SYSCMD[7	M34
CPU_SYSCMD[8	N29
CPU_SYSRDY_C	L30

Signal Name	Ball#
CPU_TCDOEn	G32
CPU_TCMATCH	J33
CPU_TCTCEn	G29
CPU_TCWORD[(	L34
CPU_TCWORD[1	K31
CPU_VALID_INn	N31
CPU_VALID_OU	J31
DEV_AD[0]/DEV_	F4
DEV_AD[1]/DEV_	F3
DEV_AD[2]	G6
DEV_AD[3]	F2
DEV_AD[4]	H5
DEV_AD[5]	F1
DEV_AD[6]	G4
DEV_AD[7]	G3
DEV_AD[8]	G2
DEV_AD[9]	G1
DEV_AD[10]	H4
DEV_AD[11]	J5
DEV_AD[12]	H2
DEV_AD[13]	J6
DEV_AD[14]	H1
DEV_AD[15]	J4
DEV_AD[16]	J2
DEV_AD[17]	J1
DEV_AD[18]	K4
DEV_AD[19]	K3
DEV_AD[20]	K6
DEV_AD[21]	K2
DEV_AD[22]	K5
DEV_AD[23]	K1
DEV_AD[24]	L4
DEV_AD[25]	L5
DEV_AD[26]	L3
DEV_AD[27]	L2
DEV_AD[28]/DEV	L1
DEV_AD[29]/DEV	M4
DEV_AD[30]/DEV	M3
DEV_AD[31]/DEV	M2
DEV_ALE	E2
DEV_BADR[0]	D2
DEV_BADR[1]	F5
DEV_BADR[2]	E3
DEV_CSTIMINGn	E1
DEV_DP[0]	H6

Signal Name	Ball#
DEV_DP[1]	J3
DEV_DP[2]	L6
DEV_DP[3]	M1
DEV_READYn	B2
DEV_WEn[0]	C2
DEV_WEn[1]	C1
DEV_WEn[2]	D3
DEV_WEn[3]	E5
DLL0_VDDAH	AE19
DLL0_VSSA	AE20
DLL1_VDDAH	AE10
DLL1_VSSA	AE11
ETHER_CAL	U6
FIFOCLK	V4
HSTL_VREF0	Y25
HSTL_VREF1	N25
JT_CLK	B3
JT_DI	E6
JT_DO	A4
JT_MS	A3
JT_RSTn	F6
M_ACAL	E7
M_BA[0]	B27
M_BA[1]	D27
M_CASn	E27
M_CB[0]	A18
M_CB[1]	F17
M_CB[2]	B18
M_CB[3]	E18
M_CB[4]	C19
M_CB[5]	E19
M_CB[6]	F19
M_CB[7]	A20
M_CKE0	B10
M_CKE1	A10
M_CLK_OUT	D9
M_CLK_OUTn	E9
M_CSn[0]	B28
M_CSn[1]	C28
M_CSn[2]	D28
M_CSn[3]	E28
M_DA[0]	A9
M_DA[1]	B9
M_DA[2]	F8
M_DA[3]	E8

Signal Name	Ball#
M_DA[4]	D8
M_DA[5]	B8
M_DA[6]	A8
M_DA[7]	B6
M_DA[8]	D6
M_DA[9]	D7
M_DA[10]	C9
M_DA[11]	C7
M_DA[12]	B7
M_DA[13]	F28
M_DCAL	C6
M_DM[0]	B11
M_DM[1]	B13
M_DM[2]	A15
M_DM[3]	A17
M_DM[4]	A21
M_DM[5]	F22
M_DM[6]	D24
M_DM[7]	C26
M_DM[8]	B19
M_DQ[0]	C10
M_DQ[1]	D10
M_DQ[2]	E10
M_DQ[3]	F10
M_DQ[4]	C11
M_DQ[5]	D11
M_DQ[6]	E11
M_DQ[7]	A12
M_DQ[8]	B12
M_DQ[9]	C12
M_DQ[10]	D12
M_DQ[11]	E12
M_DQ[12]	D13
M_DQ[13]	E13
M_DQ[14]	F13
M_DQ[15]	A14
M_DQ[16]	B14
M_DQ[17]	C14
M_DQ[18]	D14
M_DQ[19]	E14
M_DQ[20]	B15
M_DQ[21]	C15
M_DQ[22]	D15
M_DQ[23]	E15
M_DQ[24]	A16

Table 20: MV64441 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#
M_DQ[25]	B16	M_DQS[6]	C24	NC	B5	NC	AE32	NC	AL28
M_DQ[26]	C16	M_DQS[7]	B26	NC	C3	NC	AE33	NC	AL29
M_DQ[27]	E16	M_DQS[8]	A19	NC	C4	NC	AE34	NC	AL30
M_DQ[28]	B17	M_RASn	F27	NC	D1	NC	AF29	NC	AL31
M_DQ[29]	C17	M_SSTLVREF_0	K20	NC	D5	NC	AF30	NC	AL32
M_DQ[30]	D17	M_SSTLVREF_1	K14	NC	E4	NC	AF31	NC	AL8
M_DQ[31]	E17	M_STARTBURST	D18	NC	F11	NC	AF32	NC	AL9
M_DQ[32]	B20	M_STARTBURST	C18	NC	F15	NC	AF33	NC	AM10
M_DQ[33]	C20	M_WEn	A28	NC	J29	NC	AF34	NC	AM11
M_DQ[34]	D20	MDC	U3	NC	J30	NC	AG30	NC	AM12
M_DQ[35]	E20	MDIO	U5	NC	K30	NC	AG31	NC	AM13
M_DQ[36]	B21	MPP[0]	AD5	NC	K32	NC	AG32	NC	AM14
M_DQ[37]	C21	MPP[1]	AC3	NC	K33	NC	AG33	NC	AM25
M_DQ[38]	D21	MPP[2]	AC2	NC	K34	NC	AG34	NC	AM26
M_DQ[39]	E21	MPP[3]	AC1	NC	L29	NC	AH33	NC	AM28
M_DQ[40]	F21	MPP[4]	AD4	NC	L31	NC	AH34	NC	AM29
M_DQ[41]	A22	MPP[5]	AD3	NC	L32	NC	AJ10	NC	AM30
M_DQ[42]	B22	MPP[6]	AD2	NC	L33	NC	AJ11	NC	AM31
M_DQ[43]	C22	MPP[7]	AD1	NC	N32	NC	AJ12	NC	AM32
M_DQ[44]	A23	MPP[8]	AE4	NC	V29	NC	AJ13	NC	AM8
M_DQ[45]	B23	MPP[9]	AE3	NC	AA31	NC	AJ14	NC	AM9
M_DQ[46]	C23	MPP[10]	AE6	NC	AA32	NC	AJ19	NC	AN10
M_DQ[47]	D23	MPP[11]	AE2	NC	AA33	NC	AJ25	NC	AN11
M_DQ[48]	E23	MPP[12]	AE1	NC	AA6	NC	AJ26	NC	AN12
M_DQ[49]	F23	MPP[13]	AF4	NC	AB29	NC	AJ27	NC	AN13
M_DQ[50]	A24	MPP[14]	AF3	NC	AB30	NC	AJ28	NC	AN14
M_DQ[51]	B24	MPP[15]	AF2	NC	AB31	NC	AJ29	NC	AN25
M_DQ[52]	E24	MPP[16]	AM33	NC	AB32	NC	AJ9	NC	AN26
M_DQ[53]	F24	MPP[17]	AH29	NC	AB33	NC	AK10	NC	AN27
M_DQ[54]	A25	MPP[18]	AM34	NC	AB34	NC	AK12	NC	AN28
M_DQ[55]	B25	MPP[19]	AL33	NC	AC30	NC	AK14	NC	AN29
M_DQ[56]	C25	MPP[20]	AL34	NC	AC31	NC	AK24	NC	AN30
M_DQ[57]	D25	MPP[21]	AK31	NC	AC32	NC	AK26	NC	AN31
M_DQ[58]	E25	MPP[22]	AH30	NC	AC33	NC	AK27	NC	AN8
M_DQ[59]	A26	MPP[23]	AK32	NC	AC34	NC	AK28	NC	AN9
M_DQ[60]	D26	MPP[24]	AK33	NC	AC6	NC	AK29	NC	AP8
M_DQ[61]	E26	MPP[25]	AK34	NC	AD29	NC	AK8	NC	AP10
M_DQ[62]	F26	MPP[26]	AJ31	NC	AD30	NC	AL10	NC	AP11
M_DQ[63]	A27	MPP[27]	AJ32	NC	AD31	NC	AL11	NC	AP12
M_DQS[0]	A11	MPP[28]	AJ33	NC	AD32	NC	AL12	NC	AP13
M_DQS[1]	A13	MPP[29]	AJ34	NC	AD33	NC	AL13	NC	AP25
M_DQS[2]	F14	MPP[30]	AH31	NC	AD34	NC	AL14	NC	AP26
M_DQS[3]	F16	MPP[31]	AH32	NC	AE25	NC	AL25	NC	AP27
M_DQS[4]	F20	NC	A6	NC	AE29	NC	AL26	NC	AP28
M_DQS[5]	E22	NC	A7	NC	AE30	NC	AL27	NC	AP29

Table 20: MV64441 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#	Signal Name	Ball#
NC	AP30	P1_TXD[2]	W2	PCI0_CLK	AP14	PCI1_AD[26]	AG5	V_ETH1	W11
NC	AP31	P1_TXD[3]	W3	PCI0_DEVSELn	AP19	PCI1_AD[27]	AH2	VDD_CLK	K23
NC	AP9	P1_TXD[4]	W4	PCI0_ENUMn	AN32	PCI1_AD[28]	AH3	VDD_CORE	K12
P0_COL	M6	P1_TXD[5]	V1	PCI0_FRAMEn	AM19	PCI1_AD[29]	AH4	VDD_CORE	K13
P0_CRS	R3	P1_TXD[6]	V2	PCI0_GNTn	AL15	PCI1_AD[30]	AF6	VDD_CORE	K15
P0_RXCLK	R1	P1_TXD[7]	V5	PCI0_HS	AJ30	PCI1_AD[31]	AG1	VDD_CORE	K16
P0_RXD[0]	T4	P1_TXEN	Y4	PCI0_IDSEL	AL17	PCI1_CAL	AK13	VDD_CORE	K17
P0_RXD[1]	R6	P1_TXERR	Y3	PCI0_INTn	AJ15	PCI1_CBEn[0]	AN5	VDD_CORE	K18
P0_RXD[2]	T3	PCI0_AD[0]	AN24	PCI0_IRDYn	AK19	PCI1_CBEn[1]	AN3	VDD_CORE	K19
P0_RXD[3]	T2	PCI0_AD[1]	AM24	PCI0_LED	AP32	PCI1_CBEn[2]	AL2	VDD_CORE	K21
P0_RXD[4]	T1	PCI0_AD[2]	AL24	PCI0_M66EN	AK21	PCI1_CBEn[3]	AJ3	VDD_CORE	K22
P0_RXD[5]	T5	PCI0_AD[3]	AP23	PCI0_PAR	AN20	PCI1_CLK	AF1	VDD_CORE	K25
P0_RXD[6]	U4	PCI0_AD[4]	AN23	PCI0_PERRn	AK20	PCI1_DEVSELn	AM1	VDD_CORE	L10
P0_RXD[7]	T6	PCI0_AD[5]	AM23	PCI0_REQn	AM15	PCI1_FRAMEn	AL1	VDD_CORE	L11
P0_RXDV	R5	PCI0_AD[6]	AL23	PCI0_RSTn	AK15	PCI1_GNTn	AG3	VDD_CORE	L24
P0_RXERR	R2	PCI0_AD[10]	AL22	PCI0_SERRn	AM20	PCI1_IDSEL	AG6	VDD_CORE	M10
P0_TXCLK	R4	PCI0_AD[11]	AJ21	PCI0_STOPn	AL20	PCI1_INTn	AG4	VDD_CORE	M25
P0_TXCLK_OUT	P2	PCI0_AD[12]	AP21	PCI0_TRDYn	AN19	PCI1_IRDYn	AM2	VDD_CORE	N10
P0_TXD[0]	N5	PCI0_AD[13]	AN21	PCI0_VREF	AJ23	PCI1_M66EN	AJ7	VDD_CORE	P10
P0_TXD[1]	P3	PCI0_AD[14]	AM21	PCI1_AD[0]	AM7	PCI1_PAR	AJ6	VDD_CORE	P25
P0_TXD[2]	P4	PCI0_AD[15]	AL21	PCI1_AD[1]	AK7	PCI1_PERRn	AN2	VDD_CORE	R10
P0_TXD[3]	N1	PCI0_AD[16]	AP18	PCI1_AD[2]	AL7	PCI1_REQn	AG2	VDD_CORE	R25
P0_TXD[4]	N2	PCI0_AD[17]	AJ18	PCI1_AD[3]	AP6	PCI1_RSTn	AF5	VDD_CORE	T10
P0_TXD[5]	N3	PCI0_AD[18]	AN18	PCI1_AD[4]	AN6	PCI1_SERRn	AM3	VDD_CORE	T25
P0_TXD[6]	M5	PCI0_AD[19]	AM18	PCI1_AD[5]	AM6	PCI1_STOPn	AJ5	VDD_CORE	U10
P0_TXD[7]	N4	PCI0_AD[20]	AL18	PCI1_AD[6]	AL6	PCI1_TRDYn	AH5	VDD_CORE	U25
P0_TXEN	P6	PCI0_AD[21]	AP17	PCI1_AD[7]	AP5	PCI1_VREF	AN7	VDD_CORE	V25
P0_TXERR	P1	PCI0_AD[22]	AN17	PCI1_AD[8]	AM5	PLL0_VDDAH	K24	VDD_CORE	W10
P1_COL	V3	PCI0_AD[23]	AM17	PCI1_AD[9]	AL5	PLL0_VSSA	L25	VDD_CORE	W25
P1_CRS	Y1	PCI0_AD[24]	AP16	PCI1_AD[10]	AP4	PLL1_VDDAH	K10	VDD_CORE	Y10
P1_RXCLK	Y5	PCI0_AD[25]	AN16	PCI1_AD[11]	AN4	PLL1_VSSA	K11	VDD_CORE	AA10
P1_RXD[0]	AA2	PCI0_AD[26]	AM16	PCI1_AD[12]	AM4	Pull Up	AJ8	VDD_CORE	AA25
P1_RXD[1]	AA1	PCI0_AD[27]	AJ16	PCI1_AD[13]	AK5	Pull Up	AK23	VDD_CORE	AB10
P1_RXD[2]	AA5	PCI0_AD[28]	AL16	PCI1_AD[14]	AP3	Pull Up	AN33	VDD_CORE	AB25
P1_RXD[3]	AB4	PCI0_AD[29]	AK16	PCI1_AD[15]	AK6	Pull Up	AP24	VDD_CORE	AC10
P1_RXD[4]	AB6	PCI0_AD[30]	AP15	PCI1_AD[16]	AL3	Pull Up	AP7	VDD_CORE	AC25
P1_RXD[5]	AB3	PCI0_AD[31]	AN15	PCI1_AD[17]	AK1	RGMII VREF	V10	VDD_CORE	AD10
P1_RXD[6]	AB5	PCI0_AD[7]	AJ22	PCI1_AD[18]	AK2	SCK	AC5	VDD_CORE	AD11
P1_RXD[7]	AB2	PCI0_AD[8]	AK22	PCI1_AD[19]	AK3	SDA	AC4	VDD_CORE	AD24
P1_RXDV	AA3	PCI0_AD[9]	AM22	PCI1_AD[20]	AH6	SYS_CLK	A29	VDD_CORE	AD25
P1_RXERR	AA4	PCI0_CAL	AK30	PCI1_AD[21]	AK4	SYSRSTn	F7	VDD_CORE	AE12
P1_TXCLK	Y2	PCI0_CBEn[0]	AP22	PCI1_AD[22]	AJ1	TCLK	A5	VDD_CORE	AE13
P1_TXCLK_OUT	Y6	PCI0_CBEn[1]	AP20	PCI1_AD[23]	AJ2	V_ETH0	T11	VDD_CORE	AE14
P1_TXD[0]	W1	PCI0_CBEn[2]	AL19	PCI1_AD[24]	AJ4	V_ETH0	U11	VDD_CORE	AE15
P1_TXD[1]	W5	PCI0_CBEn[3]	AK17	PCI1_AD[25]	AH1	V_ETH1	V11	VDD_CORE	AE16

Table 20: MV64441 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
VDD_CORE	AE17
VDD_CORE	AE18
VDD_CORE	AE21
VDD_CORE	AE22
VDD_CORE	AE23
VDD_CORE	AE24
VDD_CPU	M24
VDD_CPU	N24
VDD_CPU	P24
VDD_CPU	R24
VDD_CPU	T24
VDD_CPU	U24
VDD_CPU	V24
VDD_CPU	W24
VDD_CPU	Y24
VDD_CPU	AA24
VDD_CPU	AB24
VDD_DRAM	L12
VDD_DRAM	L13
VDD_DRAM	L14
VDD_DRAM	L15
VDD_DRAM	L16
VDD_DRAM	L17
VDD_DRAM	L18
VDD_DRAM	L19
VDD_DRAM	L20
VDD_DRAM	L21
VDD_DRAM	L22
VDD_DRAM	L23
VDD_V33	M11
VDD_V33	N11
VDD_V33	P11
VDD_V33	R11
VDD_V33	Y11
VDD_V33	AA11
VDD_V33	AB11
VDD_V33	AC11
VDD_V33	AC24
VDD_V33	AD12
VDD_V33	AD13
VDD_V33	AD14
VDD_V33	AD15
VDD_V33	AD16
VDD_V33	AD17
VDD_V33	AD18

Signal Name	Ball#
VDD_V33	AD19
VDD_V33	AD20
VDD_V33	AD21
VDD_V33	AD22
VDD_V33	AD23
VSS	A2
VSS	A33
VSS	B1
VSS	B4
VSS	B34
VSS	C5
VSS	C8
VSS	C13
VSS	C27
VSS	D4
VSS	D16
VSS	D19
VSS	D22
VSS	F9
VSS	F12
VSS	F18
VSS	F25
VSS	F31
VSS	F32
VSS	G5
VSS	H3
VSS	H31
VSS	H32
VSS	H34
VSS	J34
VSS	K29
VSS	M30
VSS	N6
VSS	P5
VSS	P14
VSS	P15
VSS	P16
VSS	P17
VSS	P18
VSS	P19
VSS	P20
VSS	P21
VSS	P29
VSS	R14
VSS	R15

Signal Name	Ball#
VSS	R16
VSS	R17
VSS	R18
VSS	R19
VSS	R20
VSS	R21
VSS	T14
VSS	T15
VSS	T16
VSS	T17
VSS	T18
VSS	T19
VSS	T20
VSS	T21
VSS	T30
VSS	U1
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	U18
VSS	U19
VSS	U20
VSS	U21
VSS	V6
VSS	V14
VSS	V15
VSS	V16
VSS	V17
VSS	V18
VSS	V19
VSS	V20
VSS	V21
VSS	W6
VSS	W14
VSS	W15
VSS	W16
VSS	W17
VSS	W18
VSS	W19
VSS	W20
VSS	W21
VSS	W30
VSS	Y14
VSS	Y15

Signal Name	Ball#
VSS	Y16
VSS	Y17
VSS	Y18
VSS	Y19
VSS	Y20
VSS	Y21
VSS	AA14
VSS	AA15
VSS	AA16
VSS	AA17
VSS	AA18
VSS	AA19
VSS	AA20
VSS	AA21
VSS	AA30
VSS	AB1
VSS	AC29
VSS	AD6
VSS	AE5
VSS	AE31
VSS	AJ17
VSS	AJ20
VSS	AJ24
VSS	AK9
VSS	AK11
VSS	AK18
VSS	AK25
VSS	AL4
VSS	AM27
VSS	AN1
VSS	AN22
VSS	AN34
VSS	AP2
VSS	AP33

Section 7. MV64442 Pinout Map and Table, 844 Pin BGA

Figure 11: MV64442 Pinout Map (Top View, Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A		VSS	JT_MS	JT_DO	TCLK	NC	NC	M_DA[6]	M_DA[0]	M_CKE1	M_DQS[0]	M_DQ[7]	M_DQS[1]	M_DQ[15]	M_DM[2]	M_DQ[24]	M_DM[3]	A
B	VSS	DEV_READYn	JT_CLK	VSS	NC	M_DA[7]	M_DA[12]	M_DA[5]	M_DA[1]	M_CKE0	M_DM[0]	M_DQ[8]	M_DM[1]	M_DQ[16]	M_DQ[20]	M_DQ[25]	M_DQ[28]	B
C	DEV_WEn[1]	DEV_WEn[0]	NC	NC	VSS	M_DCAL	M_DA[11]	VSS	M_DA[10]	M_DQ[0]	M_DQ[4]	M_DQ[9]	VSS	M_DQ[17]	M_DQ[21]	M_DQ[26]	M_DQ[29]	C
D	NC	DEV_BADR[0]	DEV_WEn[2]	VSS	NC	M_DA[8]	M_DA[9]	M_DA[4]	M_CLK_OUT	M_DQ[1]	M_DQ[5]	M_DQ[10]	M_DQ[12]	M_DQ[18]	M_DQ[22]	VSS	M_DQ[30]	D
E	DEV_CSTIMINGn	DEV_ALE	DEV_BADR[2]	NC	DEV_WEn[3]	JT_DI	M_ACAL	M_DA[3]	M_CLK_OUTn	M_DQ[2]	M_DQ[6]	M_DQ[11]	M_DQ[13]	M_DQ[19]	M_DQ[23]	M_DQ[27]	M_DQ[31]	E
F	DEV_AD[5]	DEV_AD[3]	DEV_AD[1]/DEV_RWn	DEV_AD[0]/DEV_BOOT_CSn	DEV_BADR[1]	JT_RSTn	SYSRSTn	M_DA[2]	VSS	M_DQ[3]	NC	VSS	M_DQ[14]	M_DQS[2]	NC	M_DQS[3]	M_CB[1]	F
G	DEV_AD[9]	DEV_AD[8]	DEV_AD[7]	DEV_AD[6]	VSS	DEV_AD[2]												G
H	DEV_AD[14]	DEV_AD[12]	VSS	DEV_AD[10]	DEV_AD[4]	DEV_DP[0]				MV64442								H
J	DEV_AD[17]	DEV_AD[16]	DEV_DP[1]	DEV_AD[15]	DEV_AD[11]	DEV_AD[13]												J
K	DEV_AD[23]	DEV_AD[21]	DEV_AD[19]	DEV_AD[18]	DEV_AD[22]	DEV_AD[20]				PLL1_VDDAH	PLL1_VSSA	VDD_CORE	VDD_CORE	M_SSTLVREF_1	VDD_CORE	VDD_CORE	VDD_CORE	K
L	DEV_AD[28]/DEV_CSn[0]	DEV_AD[27]	DEV_AD[26]	DEV_AD[24]	DEV_AD[25]	DEV_DP[2]				VDD_CORE	VDD_CORE	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	L
M	DEV_DP[3]	DEV_AD[31]/DEV_CSn[3]	DEV_AD[30]/DEV_CSn[2]	DEV_AD[29]/DEV_CSn[1]	P0_TXD[6]	P0_COL				VDD_CORE	VDD_V33							M
N	P0_TXD[3]	P0_TXD[4]	P0_TXD[5]	P0_TXD[7]	P0_TXD[0]	VSS				VDD_CORE	VDD_V33							N
P	P0_TXERR	P0_TXCLK_OUT	P0_TXD[1]	P0_TXD[2]	VSS	P0_TXEN				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	P
R	P0_RXCLK	P0_RXERR	P0_CRS	P0_TXCLK	P0_RXDV	P0_RXD[1]				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	R
T	P0_RXD[4]	P0_RXD[3]	P0_RXD[2]	P0_RXD[0]	P0_RXD[5]	P0_RXD[7]				VDD_CORE	V_ETH0			VSS	VSS	VSS	VSS	T
U	VSS	CLK125	MDC	P0_RXD[6]	MDIO	ETHER_CAL				VDD_CORE	V_ETH0			VSS	VSS	VSS	VSS	U
V	Pull Down	NC	VSS	FIFOCLK	NC	VSS				RGMII VREF	V_ETH0			VSS	VSS	VSS	VSS	V
W	Pull Down	Pull Down	Pull Down	Pull Down	Pull Down	VSS				VDD_CORE	V_ETH0			VSS	VSS	VSS	VSS	W
Y	VSS	VSS	NC	NC	VSS	NC				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	Y
AA	VSS	VSS	VSS	VSS	VSS	NC				VDD_CORE	VDD_V33			VSS	VSS	VSS	VSS	AA
AB	VSS	VSS	VSS	VSS	VSS	VSS				VDD_CORE	VDD_V33							AB
AC	MPP[3]	MPP[2]	MPP[1]	SDA	SCK	NC				VDD_CORE	VDD_V33							AC
AD	MPP[7]	MPP[6]	MPP[5]	MPP[4]	MPP[0]	VSS				VDD_CORE	VDD_CORE	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	AD
AE	MPP[12]	MPP[11]	MPP[9]	MPP[8]	VSS	MPP[10]				DLL1_VDDAH	DLL1_VSSA	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	AE
AF	PCI1_CLK	MPP[15]	MPP[14]	MPP[13]	PCI1_RSTn	PCI1_AD[30]												AF
AG	PCI1_AD[31]	PCI1_REQn	PCI1_GNTn	PCI1_INTn	PCI1_AD[26]	PCI1_IDSEL												AG
AH	PCI1_AD[25]	PCI1_AD[27]	PCI1_AD[28]	PCI1_AD[29]	PCI1_TRDYn	PCI1_AD[20]												AH
AJ	PCI1_AD[22]	PCI1_AD[23]	PCI1_CBEn[3]	PCI1_AD[24]	PCI1_STOPn	PCI1_PAR	PCI1_M66EN	Pull Up	NC	NC	NC	NC	NC	NC	PCI0_INTn	PCI0_AD[27]	VSS	AJ
AK	PCI1_AD[17]	PCI1_AD[18]	PCI1_AD[19]	PCI1_AD[21]	PCI1_AD[13]	PCI1_AD[15]	PCI1_AD[1]	NC	VSS	NC	VSS	NC	PCI1_CAL	NC	PCI0_RSTn	PCI0_AD[29]	PCI0_CBEn[3]	AK
AL	PCI1_FRAMEn	PCI1_CBEn[2]	PCI1_AD[16]	VSS	PCI1_AD[9]	PCI1_AD[6]	PCI1_AD[2]	NC	NC	NC	NC	NC	NC	NC	PCI0_GNTn	PCI0_AD[28]	PCI0_IDSEL	AL
AM	PCI1_DEVSELn	PCI1_IRDYn	PCI1_SERRn	PCI1_AD[12]	PCI1_AD[8]	PCI1_AD[5]	PCI1_AD[0]	NC	NC	NC	NC	NC	NC	NC	PCI0_REQn	PCI0_AD[26]	PCI0_AD[23]	AM
AN	VSS	PCI1_PERRn	PCI1_CBEn[1]	PCI1_AD[11]	PCI1_CBEn[0]	PCI1_AD[4]	PCI1_VREF	NC	NC	NC	NC	NC	NC	NC	PCI0_AD[31]	PCI0_AD[25]	PCI0_AD[22]	AN
AP		VSS	PCI1_AD[14]	PCI1_AD[10]	PCI1_AD[7]	PCI1_AD[3]	Pull Up	NC	NC	NC	NC	NC	NC	PCI0_CLK	PCI0_AD[30]	PCI0_AD[24]	PCI0_AD[21]	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 12: MV64442 Pinout Map (Top View, Right Side)

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	M_CB[0]	M_DQS[8]	M_CB[7]	M_DM[4]	M_DQ[41]	M_DQ[44]	M_DQ[50]	M_DQ[54]	M_DQ[59]	M_DQ[63]	M_WEn	SYS_CLK	CPU_SYSAD[62]	CPU_SYSAD[56]	CPU_SYSAD[53]	VSS		A
B	M_CB[2]	M_DM[8]	M_DQ[32]	M_DQ[36]	M_DQ[42]	M_DQ[45]	M_DQ[51]	M_DQ[55]	M_DQS[7]	M_BA[0]	M_CSn[0]	CPU_SYSAD[7]	CPU_SYSAD[61]	CPU_SYSAD[55]	CPU_SYSAD[52]	CPU_SYSAD[50]	VSS	B
C	M_STARTBURST_IN	M_CB[4]	M_DQ[33]	M_DQ[37]	M_DQ[43]	M_DQ[46]	M_DQS[6]	M_DQ[56]	M_DM[7]	VSS	M_CSn[1]	CPU_SYSAD[63]	CPU_SYSAD[60]	CPU_SYSAD[54]	CPU_SYSAD[51]	CPU_SYSAD[47]	CPU_SYSAD[48]	C
D	M_STARTBURST	VSS	M_DQ[34]	M_DQ[38]	VSS	M_DQ[47]	M_DM[6]	M_DQ[57]	M_DQ[60]	M_BA[1]	M_CSn[2]	CPU_SYSAD[59]	CPU_SYSAD[58]	CPU_SYSAD[43]	CPU_SYSAD[44]	CPU_SYSAD[45]	CPU_SYSAD[46]	D
E	M_CB[3]	M_CB[5]	M_DQ[35]	M_DQ[39]	M_DQS[5]	M_DQ[48]	M_DQ[52]	M_DQ[58]	M_DQ[61]	M_CASn	M_CSn[3]	CPU_SYSAD[57]	CPU_SYSADC[5]	CPU_SYSAD[49]	CPU_SYSADC[4]	CPU_SYSAD[40]	CPU_SYSAD[41]	E
F	VSS	M_CB[6]	M_DQS[4]	M_DQ[40]	M_DM[5]	M_DQ[49]	M_DQ[53]	VSS	M_DQ[62]	M_RASn	M_DA[13]	CPU_SYSADC[6]	CPU_SYSAD[42]	VSS	VSS	CPU_SYSAD[38]	CPU_SYSAD[39]	F
G												CPU_TCTCEn	CPU_SYSAD[37]	CPU_INTn[0]	CPU_TCDOEn	CPU_PACKn	CPU_SYSAD[36]	G
H								MV64442				CPU_PREQn	CPU_RSSWAPn	VSS	VSS	CPU_INTn[1]	VSS	H
J												NC	NC	CPU_VALID_OUTn	CPU_RELEASEn	CPU_TCMATCH	VSS	J
K	VDD_CORE	VDD_CORE	M_SSTLVREF_0	VDD_CORE	VDD_CORE	VDD_CLK	PLL0_VDDAH	VDD_CORE				VSS	NC	CPU_TCWORD[1]	NC	NC	NC	K
L	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_DRAM	VDD_CORE	PLL0_VSSA				NC	CPU_SYSRDY_OUTn	NC	NC	NC	CPU_TCWORD[0]	L
M							VDD_CPU	VDD_CORE				CPU_SYSCMD[5]	VSS	CPU_SYSCMD[2]	CPU_SYSCMD[4]	CPU_SYSCMD[6]	CPU_SYSCMD[7]	M
N							VDD_CPU	HSTL_VREF1				CPU_SYSCMD[8]	CPU_SYSCMD[3]	CPU_VALID_INn	NC	CPU_SYSCMD[0]	CPU_SYSCMD[1]	N
P	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				VSS	CPU_SYSAD[31]	CPU_SYSAD[32]	CPU_SYSAD[33]	CPU_SYSAD[34]	CPU_SYSAD[35]	P
R	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[27]	CPU_SYSAD[29]	CPU_SYSAD[26]	CPU_SYSAD[28]	CPU_SYSAD[30]	CPU_SYSADC[3]	R
T	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSADC[2]	VSS	CPU_SYSAD[22]	CPU_SYSAD[23]	CPU_SYSAD[24]	CPU_SYSAD[25]	T
U	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSADC[1]	CPU_SYSAD[17]	CPU_SYSAD[18]	CPU_SYSAD[19]	CPU_SYSAD[20]	CPU_SYSAD[21]	U
V	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				NC	CPU_SYSAD[16]	CPU_SYSAD[11]	CPU_SYSAD[12]	CPU_SYSAD[13]	CPU_SYSAD[14]	V
W	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[15]	VSS	CPU_SYSAD[7]	CPU_SYSAD[8]	CPU_SYSAD[9]	CPU_SYSAD[10]	W
Y	VSS	VSS	VSS	VSS			VDD_CPU	HSTL_VREF0				CPU_SYSAD[6]	CPU_SYSADC[0]	CPU_SYSAD[2]	CPU_SYSAD[3]	CPU_SYSAD[4]	CPU_SYSAD[5]	Y
AA	VSS	VSS	VSS	VSS			VDD_CPU	VDD_CORE				CPU_SYSAD[0]	VSS	NC	NC	NC	CPU_SYSAD[1]	AA
AB							VDD_CPU	VDD_CORE				NC	NC	NC	NC	NC	NC	AB
AC							VDD_V33	VDD_CORE				VSS	NC	NC	NC	NC	NC	AC
AD	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_V33	VDD_CORE	VDD_CORE				NC	NC	NC	NC	NC	NC	AD
AE	VDD_CORE	DLL0_VDDAH	DLL0_VSSA	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	NC				NC	NC	VSS	NC	NC	NC	AE
AF												NC	NC	NC	NC	NC	NC	AF
AG												CPU_CAL	NC	NC	NC	NC	NC	AG
AH												MPP[17]	MPP[22]	MPP[30]	MPP[31]	NC	NC	AH
AJ	PCI0_AD[17]	NC	VSS	PCI0_AD[11]	PCI0_AD[7]	PCI0_VREF	VSS	NC	NC	PCI0_AD[55]	PCI0_AD[47]	PCI0_AD[39]	PCI0_HS	MPP[26]	MPP[27]	MPP[28]	MPP[29]	AJ
AK	VSS	PCI0_IRDYn	PCI0_PERRn	PCI0_M66EN	PCI0_AD[8]	PCI0_REQ64n	PCI0_CBEn[6]	VSS	PCI0_AD[57]	PCI0_AD[53]	PCI0_AD[41]	PCI0_AD[33]	PCI0_CAL	MPP[21]	MPP[23]	MPP[24]	MPP[25]	AK
AL	PCI0_AD[20]	PCI0_CBEn[2]	PCI0_STOPn	PCI0_AD[15]	PCI0_AD[10]	PCI0_AD[6]	PCI0_AD[2]	PCI0_CBEn[7]	PCI0_AD[63]	PCI0_AD[59]	PCI0_AD[54]	PCI0_AD[49]	PCI0_AD[44]	PCI0_AD[38]	PCI0_AD[34]	MPP[19]	MPP[20]	AL
AM	PCI0_AD[19]	PCI0_FRAMEn	PCI0_SERRn	PCI0_AD[14]	PCI0_AD[9]	PCI0_AD[5]	PCI0_AD[1]	PCI0_CBEn[5]	PCI0_AD[62]	VSS	PCI0_AD[52]	PCI0_AD[48]	PCI0_AD[43]	PCI0_AD[37]	PCI0_AD[32]	MPP[16]	MPP[18]	AM
AN	PCI0_AD[18]	PCI0_TRDYn	PCI0_PAR	PCI0_AD[13]	VSS	PCI0_AD[4]	PCI0_AD[0]	PCI0_CBEn[4]	PCI0_AD[61]	PCI0_AD[58]	PCI0_AD[51]	PCI0_AD[46]	PCI0_AD[42]	PCI0_AD[36]	PCI0_ENUMn	PCI0_64ENn	VSS	AN
AP	PCI0_AD[16]	PCI0_DEVSELn	PCI0_CBEn[1]	PCI0_AD[12]	PCI0_CBEn[0]	PCI0_AD[3]	PCI0_ACK64n	PCI0_PAR64	PCI0_AD[60]	PCI0_AD[56]	PCI0_AD[50]	PCI0_AD[45]	PCI0_AD[40]	PCI0_AD[35]	PCI0_LED	VSS		AP
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Table 21: MV64442 Pinout Sorted by Signal Name

Signal Name	Ball#
CLK125	U2
CPU_CAL	AG29
CPU_INTn[0]	G31
CPU_INTn[1]	H33
CPU_PACKn	G33
CPU_PREQn	H29
CPU_RELEASEn	J32
CPU_RSSWAPn	H30
CPU_SYSAD[0]	AA29
CPU_SYSAD[1]	AA34
CPU_SYSAD[2]	Y31
CPU_SYSAD[3]	Y32
CPU_SYSAD[4]	Y33
CPU_SYSAD[5]	Y34
CPU_SYSAD[6]	Y29
CPU_SYSAD[7]	W31
CPU_SYSAD[8]	W32
CPU_SYSAD[9]	W33
CPU_SYSAD[10]	W34
CPU_SYSAD[11]	V31
CPU_SYSAD[12]	V32
CPU_SYSAD[13]	V33
CPU_SYSAD[14]	V34
CPU_SYSAD[15]	W29
CPU_SYSAD[16]	V30
CPU_SYSAD[17]	U30
CPU_SYSAD[18]	U31
CPU_SYSAD[19]	U32
CPU_SYSAD[20]	U33
CPU_SYSAD[21]	U34
CPU_SYSAD[22]	T31
CPU_SYSAD[23]	T32
CPU_SYSAD[24]	T33
CPU_SYSAD[25]	T34
CPU_SYSAD[26]	R31
CPU_SYSAD[27]	R29
CPU_SYSAD[28]	R32
CPU_SYSAD[29]	R30
CPU_SYSAD[30]	R33
CPU_SYSAD[31]	P30
CPU_SYSAD[32]	P31
CPU_SYSAD[33]	P32
CPU_SYSAD[34]	P33
CPU_SYSAD[35]	P34
CPU_SYSAD[36]	G34
CPU_SYSAD[37]	G30
CPU_SYSAD[38]	F33
CPU_SYSAD[39]	F34
CPU_SYSAD[40]	E33
CPU_SYSAD[41]	E34
CPU_SYSAD[42]	F30
CPU_SYSAD[43]	D31
CPU_SYSAD[44]	D32
CPU_SYSAD[45]	D33
CPU_SYSAD[46]	D34
CPU_SYSAD[47]	C33
CPU_SYSAD[48]	C34
CPU_SYSAD[49]	E31
CPU_SYSAD[50]	B33
CPU_SYSAD[51]	C32
CPU_SYSAD[52]	B32
CPU_SYSAD[53]	A32
CPU_SYSAD[54]	C31
CPU_SYSAD[55]	B31
CPU_SYSAD[56]	A31
CPU_SYSAD[57]	E29
CPU_SYSAD[58]	D30
CPU_SYSAD[59]	D29
CPU_SYSAD[60]	C30
CPU_SYSAD[61]	B30
CPU_SYSAD[62]	A30
CPU_SYSAD[63]	C29
CPU_SYSADC[0]	Y30
CPU_SYSADC[1]	U29
CPU_SYSADC[2]	T29
CPU_SYSADC[3]	R34
CPU_SYSADC[4]	E32
CPU_SYSADC[5]	E30
CPU_SYSADC[6]	F29
CPU_SYSADC[7]	B29
CPU_SYSCMD[0	N33
CPU_SYSCMD[1	N34
CPU_SYSCMD[2	M31
CPU_SYSCMD[3	N30
CPU_SYSCMD[4	M32
CPU_SYSCMD[5	M29
CPU_SYSCMD[6	M33
CPU_SYSCMD[7	M34
CPU_SYSCMD[8	N29
CPU_SYSRDY_C	L30
CPU_TCDOEn	G32
CPU_TCMATCH	J33
CPU_TCTCEn	G29
CPU_TCWORD[(	L34
CPU_TCWORD[1	K31
CPU_VALID_INn	N31
CPU_VALID_OU	J31
DEV_AD[0]/DEV_	F4
DEV_AD[1]/DEV_	F3
DEV_AD[2]	G6
DEV_AD[3]	F2
DEV_AD[4]	H5
DEV_AD[5]	F1
DEV_AD[6]	G4
DEV_AD[7]	G3
DEV_AD[8]	G2
DEV_AD[9]	G1
DEV_AD[10]	H4
DEV_AD[11]	J5
DEV_AD[12]	H2
DEV_AD[13]	J6
DEV_AD[14]	H1
DEV_AD[15]	J4
DEV_AD[16]	J2
DEV_AD[17]	J1
DEV_AD[18]	K4
DEV_AD[19]	K3
DEV_AD[20]	K6
DEV_AD[21]	K2
DEV_AD[22]	K5
DEV_AD[23]	K1
DEV_AD[24]	L4
DEV_AD[25]	L5
DEV_AD[26]	L3
DEV_AD[27]	L2
DEV_AD[28]/DEV	L1
DEV_AD[29]/DEV	M4
DEV_AD[30]/DEV	M3
DEV_AD[31]/DEV	M2
DEV_ALE	E2
DEV_BADR[0]	D2
DEV_BADR[1]	F5
DEV_BADR[2]	E3
DEV_CSTIMINGn	E1
DEV_DP[0]	H6
DEV_DP[1]	J3
DEV_DP[2]	L6
DEV_DP[3]	M1
DEV_READYn	B2
DEV_WEn[0]	C2
DEV_WEn[1]	C1
DEV_WEn[2]	D3
DEV_WEn[3]	E5
DLL0_VDDAH	AE19
DLL0_VSSA	AE20
DLL1_VDDAH	AE10
DLL1_VSSA	AE11
ETHER_CAL	U6
FIFOCLK	V4
HSTL_VREF0	Y25
HSTL_VREF1	N25
JT_CLK	B3
JT_DI	E6
JT_DO	A4
JT_MS	A3
JT_RSTn	F6
M_ACAL	E7
M_BA[0]	B27
M_BA[1]	D27
M_CASn	E27
M_CB[0]	A18
M_CB[1]	F17
M_CB[2]	B18
M_CB[3]	E18
M_CB[4]	C19
M_CB[5]	E19
M_CB[6]	F19
M_CB[7]	A20
M_CKE0	B10
M_CKE1	A10
M_CLK_OUT	D9
M_CLK_OUTn	E9
M_CSn[0]	B28
M_CSn[1]	C28
M_CSn[2]	D28
M_CSn[3]	E28
M_DA[0]	A9
M_DA[1]	B9
M_DA[2]	F8
M_DA[3]	E8
M_DA[4]	D8
M_DA[5]	B8
M_DA[6]	A8
M_DA[7]	B6
M_DA[8]	D6
M_DA[9]	D7
M_DA[10]	C9
M_DA[11]	C7
M_DA[12]	B7
M_DA[13]	F28
M_DCAL	C6
M_DM[0]	B11
M_DM[1]	B13
M_DM[2]	A15
M_DM[3]	A17
M_DM[4]	A21
M_DM[5]	F22
M_DM[6]	D24
M_DM[7]	C26
M_DM[8]	B19
M_DQ[0]	C10
M_DQ[1]	D10
M_DQ[2]	E10
M_DQ[3]	F10
M_DQ[4]	C11
M_DQ[5]	D11
M_DQ[6]	E11
M_DQ[7]	A12
M_DQ[8]	B12
M_DQ[9]	C12
M_DQ[10]	D12
M_DQ[11]	E12
M_DQ[12]	D13
M_DQ[13]	E13
M_DQ[14]	F13
M_DQ[15]	A14
M_DQ[16]	B14
M_DQ[17]	C14
M_DQ[18]	D14
M_DQ[19]	E14
M_DQ[20]	B15
M_DQ[21]	C15
M_DQ[22]	D15
M_DQ[23]	E15
M_DQ[24]	A16

Table 21: MV64442 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
M_DQ[25]	B16
M_DQ[26]	C16
M_DQ[27]	E16
M_DQ[28]	B17
M_DQ[29]	C17
M_DQ[30]	D17
M_DQ[31]	E17
M_DQ[32]	B20
M_DQ[33]	C20
M_DQ[34]	D20
M_DQ[35]	E20
M_DQ[36]	B21
M_DQ[37]	C21
M_DQ[38]	D21
M_DQ[39]	E21
M_DQ[40]	F21
M_DQ[41]	A22
M_DQ[42]	B22
M_DQ[43]	C22
M_DQ[44]	A23
M_DQ[45]	B23
M_DQ[46]	C23
M_DQ[47]	D23
M_DQ[48]	E23
M_DQ[49]	F23
M_DQ[50]	A24
M_DQ[51]	B24
M_DQ[52]	E24
M_DQ[53]	F24
M_DQ[54]	A25
M_DQ[55]	B25
M_DQ[56]	C25
M_DQ[57]	D25
M_DQ[58]	E25
M_DQ[59]	A26
M_DQ[60]	D26
M_DQ[61]	E26
M_DQ[62]	F26
M_DQ[63]	A27
M_DQS[0]	A11
M_DQS[1]	A13
M_DQS[2]	F14
M_DQS[3]	F16
M_DQS[4]	F20
M_DQS[5]	E22

Signal Name	Ball#
M_DQS[6]	C24
M_DQS[7]	B26
M_DQS[8]	A19
M_RASn	F27
M_SSTLVREF_0	K20
M_SSTLVREF_1	K14
M_STARTBURST	D18
M_STARTBURST	C18
M_WEn	A28
MDC	U3
MDIO	U5
MPP[0]	AD5
MPP[1]	AC3
MPP[2]	AC2
MPP[3]	AC1
MPP[4]	AD4
MPP[5]	AD3
MPP[6]	AD2
MPP[7]	AD1
MPP[8]	AE4
MPP[9]	AE3
MPP[10]	AE6
MPP[11]	AE2
MPP[12]	AE1
MPP[13]	AF4
MPP[14]	AF3
MPP[15]	AF2
MPP[16]	AM33
MPP[17]	AH29
MPP[18]	AM34
MPP[19]	AL33
MPP[20]	AL34
MPP[21]	AK31
MPP[22]	AH30
MPP[23]	AK32
MPP[24]	AK33
MPP[25]	AK34
MPP[26]	AJ31
MPP[27]	AJ32
MPP[28]	AJ33
MPP[29]	AJ34
MPP[30]	AH31
MPP[31]	AH32
NC	A6
NC	A7

Signal Name	Ball#
NC	B5
NC	C3
NC	C4
NC	D1
NC	D5
NC	E4
NC	F11
NC	F15
NC	J29
NC	J30
NC	K30
NC	K32
NC	K33
NC	K34
NC	L29
NC	L31
NC	L32
NC	L33
NC	N32
NC	V2
NC	V29
NC	V5
NC	Y3
NC	Y4
NC	Y6
NC	AA31
NC	AA32
NC	AA33
NC	AA6
NC	AB29
NC	AB30
NC	AB31
NC	AB32
NC	AB33
NC	AB34
NC	AC30
NC	AC31
NC	AC32
NC	AC33
NC	AC34
NC	AC6
NC	AD29
NC	AD30
NC	AD31
NC	AD32

Signal Name	Ball#
NC	AD33
NC	AD34
NC	AE25
NC	AE29
NC	AE30
NC	AE32
NC	AE33
NC	AE34
NC	AF29
NC	AF30
NC	AF31
NC	AF32
NC	AF33
NC	AF34
NC	AG30
NC	AG31
NC	AG32
NC	AG33
NC	AG34
NC	AH33
NC	AH34
NC	AJ10
NC	AJ11
NC	AJ12
NC	AJ13
NC	AJ14
NC	AJ19
NC	AJ25
NC	AJ26
NC	AJ9
NC	AK10
NC	AK12
NC	AK14
NC	AK8
NC	AL10
NC	AL11
NC	AL12
NC	AL13
NC	AL14
NC	AL8
NC	AL9
NC	AM10
NC	AM11
NC	AM12
NC	AM13

Signal Name	Ball#
NC	AM14
NC	AM8
NC	AM9
NC	AN10
NC	AN11
NC	AN12
NC	AN13
NC	AN14
NC	AN8
NC	AN9
NC	AP8
NC	AP10
NC	AP11
NC	AP12
NC	AP13
NC	AP9
P0_COL	M6
P0_CRS	R3
P0_RXCLK	R1
P0_RXD[0]	T4
P0_RXD[1]	R6
P0_RXD[2]	T3
P0_RXD[3]	T2
P0_RXD[4]	T1
P0_RXD[5]	T5
P0_RXD[6]	U4
P0_RXD[7]	T6
P0_RXDV	R5
P0_RXERR	R2
P0_TXCLK	R4
P0_TXCLK_OUT	P2
P0_TXD[0]	N5
P0_TXD[1]	P3
P0_TXD[2]	P4
P0_TXD[3]	N1
P0_TXD[4]	N2
P0_TXD[5]	N3
P0_TXD[6]	M5
P0_TXD[7]	N4
P0_TXEN	P6
P0_TXERR	P1
PCI0_64ENn	AN33
PCI0_ACK64n	AP24
PCI0_AD[0]	AN24
PCI0_AD[1]	AM24

Table 21: MV64442 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
PCI0_AD[2]	AL24
PCI0_AD[3]	AP23
PCI0_AD[4]	AN23
PCI0_AD[5]	AM23
PCI0_AD[6]	AL23
PCI0_AD[10]	AL22
PCI0_AD[11]	AJ21
PCI0_AD[12]	AP21
PCI0_AD[13]	AN21
PCI0_AD[14]	AM21
PCI0_AD[15]	AL21
PCI0_AD[16]	AP18
PCI0_AD[17]	AJ18
PCI0_AD[18]	AN18
PCI0_AD[19]	AM18
PCI0_AD[20]	AL18
PCI0_AD[21]	AP17
PCI0_AD[22]	AN17
PCI0_AD[23]	AM17
PCI0_AD[24]	AP16
PCI0_AD[25]	AN16
PCI0_AD[26]	AM16
PCI0_AD[27]	AJ16
PCI0_AD[28]	AL16
PCI0_AD[29]	AK16
PCI0_AD[30]	AP15
PCI0_AD[31]	AN15
PCI0_AD[32]	AM32
PCI0_AD[33]	AK29
PCI0_AD[34]	AL32
PCI0_AD[35]	AP31
PCI0_AD[36]	AN31
PCI0_AD[37]	AM31
PCI0_AD[38]	AL31
PCI0_AD[39]	AJ29
PCI0_AD[40]	AP30
PCI0_AD[41]	AK28
PCI0_AD[42]	AN30
PCI0_AD[43]	AM30
PCI0_AD[44]	AL30
PCI0_AD[45]	AP29
PCI0_AD[46]	AN29
PCI0_AD[47]	AJ28
PCI0_AD[48]	AM29
PCI0_AD[49]	AL29

Signal Name	Ball#
PCI0_AD[50]	AP28
PCI0_AD[51]	AN28
PCI0_AD[52]	AM28
PCI0_AD[53]	AK27
PCI0_AD[54]	AL28
PCI0_AD[55]	AJ27
PCI0_AD[56]	AP27
PCI0_AD[57]	AK26
PCI0_AD[58]	AN27
PCI0_AD[59]	AL27
PCI0_AD[60]	AP26
PCI0_AD[61]	AN26
PCI0_AD[62]	AM26
PCI0_AD[63]	AL26
PCI0_AD[7]	AJ22
PCI0_AD[8]	AK22
PCI0_AD[9]	AM22
PCI0_CAL	AK30
PCI0_CBEn[0]	AP22
PCI0_CBEn[1]	AP20
PCI0_CBEn[2]	AL19
PCI0_CBEn[3]	AK17
PCI0_CBEn[4]	AN25
PCI0_CBEn[5]	AM25
PCI0_CBEn[6]	AK24
PCI0_CBEn[7]	AL25
PCI0_CLK	AP14
PCI0_DEVSELn	AP19
PCI0_ENUMn	AN32
PCI0_FRAMEn	AM19
PCI0_GNTn	AL15
PCI0_HS	AJ30
PCI0_IDSEL	AL17
PCI0_INTn	AJ15
PCI0_IRDYn	AK19
PCI0_LED	AP32
PCI0_M66EN	AK21
PCI0_PAR	AN20
PCI0_PAR64	AP25
PCI0_PERRn	AK20
PCI0_REQ64n	AK23
PCI0_REQn	AM15
PCI0_RSTn	AK15
PCI0_SERRn	AM20
PCI0_STOPn	AL20

Signal Name	Ball#
PCI0_TRDYn	AN19
PCI0_VREF	AJ23
PCI1_AD[0]	AM7
PCI1_AD[1]	AK7
PCI1_AD[2]	AL7
PCI1_AD[3]	AP6
PCI1_AD[4]	AN6
PCI1_AD[5]	AM6
PCI1_AD[6]	AL6
PCI1_AD[7]	AP5
PCI1_AD[8]	AM5
PCI1_AD[9]	AL5
PCI1_AD[10]	AP4
PCI1_AD[11]	AN4
PCI1_AD[12]	AM4
PCI1_AD[13]	AK5
PCI1_AD[14]	AP3
PCI1_AD[15]	AK6
PCI1_AD[16]	AL3
PCI1_AD[17]	AK1
PCI1_AD[18]	AK2
PCI1_AD[19]	AK3
PCI1_AD[20]	AH6
PCI1_AD[21]	AK4
PCI1_AD[22]	AJ1
PCI1_AD[23]	AJ2
PCI1_AD[24]	AJ4
PCI1_AD[25]	AH1
PCI1_AD[26]	AG5
PCI1_AD[27]	AH2
PCI1_AD[28]	AH3
PCI1_AD[29]	AH4
PCI1_AD[30]	AF6
PCI1_AD[31]	AG1
PCI1_CAL	AK13
PCI1_CBEn[0]	AN5
PCI1_CBEn[1]	AN3
PCI1_CBEn[2]	AL2
PCI1_CBEn[3]	AJ3
PCI1_CLK	AF1
PCI1_DEVSELn	AM1
PCI1_FRAMEn	AL1
PCI1_GNTn	AG3
PCI1_IDSEL	AG6
PCI1_INTn	AG4

Signal Name	Ball#
PCI1_IRDYn	AM2
PCI1_M66EN	AJ7
PCI1_PAR	AJ6
PCI1_PERRn	AN2
PCI1_REQn	AG2
PCI1_RSTn	AF5
PCI1_SERRn	AM3
PCI1_STOPn	AJ5
PCI1_TRDYn	AH5
PCI1_VREF	AN7
PLL0_VDDAH	K24
PLL0_VSSA	L25
PLL1_VDDAH	K10
PLL1_VSSA	K11
Pull Down	V1
Pull Down	W1
Pull Down	W2
Pull Down	W3
Pull Down	W4
Pull Down	W5
Pull Up	AJ8
Pull Up	AP7
RGMII VREF	V10
SCK	AC5
SDA	AC4
SYS_CLK	A29
SYSRSTn	F7
TCLK	A5
V_ETH0	T11
V_ETH0	U11
V_ETH0	V11
V_ETH0	W11
VDD_CLK	K23
VDD_CORE	K12
VDD_CORE	K13
VDD_CORE	K15
VDD_CORE	K16
VDD_CORE	K17
VDD_CORE	K18
VDD_CORE	K19
VDD_CORE	K21
VDD_CORE	K22
VDD_CORE	K25
VDD_CORE	L10
VDD_CORE	L11

Signal Name	Ball#
VDD_CORE	L24
VDD_CORE	M10
VDD_CORE	M25
VDD_CORE	N10
VDD_CORE	P10
VDD_CORE	P25
VDD_CORE	R10
VDD_CORE	R25
VDD_CORE	T10
VDD_CORE	T25
VDD_CORE	U10
VDD_CORE	U25
VDD_CORE	V25
VDD_CORE	W10
VDD_CORE	W25
VDD_CORE	Y10
VDD_CORE	AA10
VDD_CORE	AA25
VDD_CORE	AB10
VDD_CORE	AB25
VDD_CORE	AC10
VDD_CORE	AC25
VDD_CORE	AD10
VDD_CORE	AD11
VDD_CORE	AD24
VDD_CORE	AD25
VDD_CORE	AE12
VDD_CORE	AE13
VDD_CORE	AE14
VDD_CORE	AE15
VDD_CORE	AE16
VDD_CORE	AE17
VDD_CORE	AE18
VDD_CORE	AE21
VDD_CORE	AE22
VDD_CORE	AE23
VDD_CORE	AE24
VDD_CPU	M24
VDD_CPU	N24
VDD_CPU	P24
VDD_CPU	R24
VDD_CPU	T24
VDD_CPU	U24
VDD_CPU	V24
VDD_CPU	W24

Table 21: MV64442 Pinout Sorted by Signal Name (Continued)

Signal Name	Ball#
VDD_CPU	Y24
VDD_CPU	AA24
VDD_CPU	AB24
VDD_DRAM	L12
VDD_DRAM	L13
VDD_DRAM	L14
VDD_DRAM	L15
VDD_DRAM	L16
VDD_DRAM	L17
VDD_DRAM	L18
VDD_DRAM	L19
VDD_DRAM	L20
VDD_DRAM	L21
VDD_DRAM	L22
VDD_DRAM	L23
VDD_V33	M11
VDD_V33	N11
VDD_V33	P11
VDD_V33	R11
VDD_V33	Y11
VDD_V33	AA11
VDD_V33	AB11
VDD_V33	AC11
VDD_V33	AC24
VDD_V33	AD12
VDD_V33	AD13
VDD_V33	AD14
VDD_V33	AD15
VDD_V33	AD16
VDD_V33	AD17
VDD_V33	AD18
VDD_V33	AD19
VDD_V33	AD20
VDD_V33	AD21
VDD_V33	AD22
VDD_V33	AD23
VSS	A2
VSS	A33
VSS	AA1
VSS	B1
VSS	B34
VSS	B4
VSS	C13
VSS	C27
VSS	C5

Signal Name	Ball#
VSS	C8
VSS	D16
VSS	D19
VSS	D22
VSS	D4
VSS	F12
VSS	F18
VSS	F25
VSS	F31
VSS	F32
VSS	F9
VSS	G5
VSS	H3
VSS	H31
VSS	H32
VSS	J34
VSS	H34
VSS	K29
VSS	M30
VSS	N6
VSS	P14
VSS	P15
VSS	P16
VSS	P17
VSS	P18
VSS	P19
VSS	P20
VSS	P21
VSS	P29
VSS	P5
VSS	R14
VSS	R15
VSS	R16
VSS	R17
VSS	R18
VSS	R19
VSS	R20
VSS	R21
VSS	T14
VSS	T15
VSS	T16
VSS	T17
VSS	T18
VSS	T19
VSS	T20

Signal Name	Ball#
VSS	T21
VSS	T30
VSS	U1
VSS	U14
VSS	U15
VSS	U16
VSS	U17
VSS	U18
VSS	U19
VSS	U20
VSS	U21
VSS	V14
VSS	W14
VSS	V15
VSS	W15
VSS	V16
VSS	W16
VSS	V17
VSS	W17
VSS	V18
VSS	W18
VSS	V19
VSS	W19
VSS	V20
VSS	W20
VSS	V21
VSS	W21
VSS	V3
VSS	W30
VSS	V6
VSS	W6
VSS	Y1
VSS	Y14
VSS	Y15
VSS	Y16
VSS	Y17
VSS	Y18
VSS	Y19
VSS	Y2
VSS	Y20
VSS	Y21
VSS	Y5
VSS	AA14
VSS	AA15
VSS	AA16

Signal Name	Ball#
VSS	AA17
VSS	AA18
VSS	AA19
VSS	AA2
VSS	AA20
VSS	AA21
VSS	AA3
VSS	AA30
VSS	AA4
VSS	AA5
VSS	AB1
VSS	AB2
VSS	AB3
VSS	AB4
VSS	AB5
VSS	AB6
VSS	AC29
VSS	AD6
VSS	AE31
VSS	AE5
VSS	AJ17
VSS	AJ20
VSS	AJ24
VSS	AK11
VSS	AK18
VSS	AK25
VSS	AK9
VSS	AL4
VSS	AM27
VSS	AN1
VSS	AN22
VSS	AN34
VSS	AP2
VSS	AP33

Section 8. MV64440 Gigabit Ethernet Pins Multiplexing

The MV64440 contains three Gigabit Ethernet MACs/FIFO interfaces. These interfaces have 50 dedicated pins, plus an additional 25 optional pins. These optional pins use the PCI1 interface's upper bus signals. If DEV_AD[25] is sampled HIGH during reset (see Table 29 on page 84), PCI1_PAD[63:39] are no longer used as PCI signals. These pins become Gigabit Ethernet MAC/FIFO interface signals.

8.1 Gigabit Ethernet Pins Multiplexing

Each port is separately configured at reset to one of the following modes, as described in Table 22

Table 22: Gigabit Ethernet Port/FIFO Interface Reset Configurations

Reset Sample	Mode
0x0	Unused
0x1	TBI
0x2	GMII/MII
0x3	MII only
0x4	8-bit FIFO
0x5	16-bit FIFO
0x6	Reserved
0x7	RGMII

Note

See Table 29 on page 84 for exact reset strapping configuration.

These reset configurations not only define each port operation mode, but also the entire 50 (75) pins multiplexing. The entire set of ports configurations is narrowed down to the three muxing options, named `MuxSel`. See Table 22 for each pin functionality, per different MuxSel setting.

If only using, the 50 Gigabit Ethernet dedicated pins, the possible configurations are:

- Two MII/GMII/TBI Gigabit Ethernet ports 0/1 (MuxSel = 0x0)
- One MII/GMII/TBI Gigabit Ethernet port 0/1 + one 8-bit FIFO port 0/1 (MuxSel = 0x0)
- Two 8-bit FIFO ports 0/1 (MuxSel = 0x0)
- Three RGMII Gigabit Ethernet ports (MuxSel = 0x1)
- Two RGMII Gigabit Ethernet ports 0/2 + one 8-bit FIFO port 1 (MuxSel = 0x1)
- Two RGMII Gigabit Ethernet ports 0/2 + one MII/GMII/TBI port1 (MuxSel = 0x1)
- One 16-bit FIFO port 0 (MuxSel = 0x2)

If using the 50 Gigabit Ethernet pins and the 25 PCI1 pins, the possible configurations are:

- Three MII/GMII/TBI Gigabit Ethernet ports 0/1/2 (MuxSel = 0x0)
- Two MII/GMII/TBI Gigabit Ethernet ports 0/1/2 + one 8-bit FIFO port 0/1/2 (MuxSel = 0x0)
- One MII/GMII/TBI Gigabit Ethernet port 0/1/2 + two 8-bit FIFO ports 0/1/2 (MuxSel = 0x0)
- Three 8-bit FIFO ports 0/1/2 (MuxSel = 0x0)
- One 16-bit FIFO port 0 + one MII/GMII/TBI Gigabit Ethernet port 2 (MuxSel = 0x2)
- One 16-bit FIFO port 0 + one 8-bit FIFO port 2 (MuxSel = 2)

Note

It is the user's responsibility to correctly set the reset configuration of each port to a valid configuration. Setting the ports to an unsupported configuration (e.g. two ports configured to 16-bit FIFO interface) will have unpredictable results.

Table 23 shows the different Gigabit Ethernet (GbE) MAC/FIFO interface pins multiplexing.

Table 23: Gigabit Ethernet Unit Pins Multiplexing

I/O	Mux Sel = 0x0		Mux Sel = 0x1			Mux Sel = 0x2		
	GbE P0/1/2 (GMII/ TBI/MII)	8-bit FIFO F0/1/2	GbE P0/1/2 (RGMII)	GbE P1 (GMII/TBI/ MII)	8-bit FIFO F1	16-bit FIFO F0	GbE P2 (GMII/TBI/ MII)	8-bit FIFO F2
O	P0_TXD[0]	F0_TXD[0]	P0_TXD[0]			F0_TXD[0]		
O	P0_TXD[1]	F0_TXD[1]	P0_TXD[1]			F0_TXD[1]		
O	P0_TXD[2]	F0_TXD[2]	P0_TXD[2]			F0_TXD[2]		
O	P0_TXD[3]	F0_TXD[3]	P0_TXD[3]			F0_TXD[3]		
O	P0_TXD[4]	F0_TXD[4]	P2_TXD[0]			F0_TXD[4]		
O	P0_TXD[5]	F0_TXD[5]	P2_TXD[1]			F0_TXD[5]		
O	P0_TXD[6]	F0_TXD[6]	P2_TXD[2]			F0_TXD[6]		
O	P0_TXD[7]	F0_TXD[7]	P2_TXD[3]			F0_TXD[7]		
O	P0_TXEN	F0_TXEN	P0_TXEN			F0_TXEN		
I	P0_TXCLK	F0_TXFC	P2_RXDV			F0_TXFC		
O	P0_TX ERR	F0_TXV ALID	P2_TXEN			F0_TXVALID		
O	P0_TXCLK _OUT	F0_TXCLK _OUT	P0_TXCLK_O UT			F0_TXCLK_O UT		
I	P0_COL							
I	P0_RXD[0]	F0_RXD[0]	P0_RXD[0]			F0_RXD[0]		
I	P0_RXD[1]	F0_RXD[1]	P0_RXD[1]			F0_RXD[1]		
I	P0_RXD[2]	F0_RXD[2]	P0_RXD[2]			F0_RXD[2]		
I	P0_RXD[3]	F0_RXD[3]	P0_RXD[3]			F0_RXD[3]		
I	P0_RXD[4]	F0_RXD[4]	P2_RXD[0]			F0_RXD[4]		
I	P0_RXD[5]	F0_RXD[5]	P2_RXD[1]			F0_RXD[5]		
I	P0_RXD[6]	F0_RXD[6]	P2_RXD[2]			F0_RXD[6]		
I	P0_RXD[7]	F0_RXD[7]	P2_RXD[3]			F0_RXD[7]		

Table 23: Gigabit Ethernet Unit Pins Multiplexing (Continued)

I/O	Mux Sel = 0x0		Mux Sel = 0x1			Mux Sel = 0x2		
	GbE P0/1/2 (GMII/ TBI/MII)	8-bit FIFO F0/1/2	GbE P0/1/2 (RGMII)	GbE P1 (GMII/TBI/ MII)	8-bit FIFO F1	16-bit FIFO F0	GbE P2 (GMII/TBI/ MII)	8-bit FIFO F2
I/O	P0_CRS (I)	F0_RXFC0 (O)	P2_TXCLK_OUT (O)			F0_RXFC0 (O)		
I	P0_RXDV	F0_RXEN	P0_RXDV			F0_RXEN		
I	P0_RX ERR	F0_RX VALID	P2_RXCLK			F0_RXVALID		
I	P0_RXCLK	F0_RXCLK	P0_RXCLK			F0_RXCLK		
O	P1_TXD[0]	F1_TXD[0]	P1_TXD[0]	P1_TXD[0]	F1_TXD[0]	F0_TXD[8]		
O	P1_TXD[1]	F1_TXD[1]	P1_TXD[1]	P1_TXD[1]	F1_TXD[1]	F0_TXD[9]		
O	P1_TXD[2]	F1_TXD[2]	P1_TXD[2]	P1_TXD[2]	F1_TXD[2]	F0_TXD[10]		
O	P1_TXD[3]	F1_TXD[3]	P1_TXD[3]	P1_TXD[3]	F1_TXD[3]	F0_TXD[11]		
O	P1_TXD[4]	F1_TXD[4]		P1_TXD[4]	F1_TXD[4]	F0_TXD[12]		
O	P1_TXD[5]	F1_TXD[5]		P1_TXD[5]	F1_TXD[5]	F0_TXD[13]		
O	P1_TXD[6]	F1_TXD[6]		P1_TXD[6]	F1_TXD[6]	F0_TXD[14]		
O	P1_TXD[7]	F1_TXD[7]		P1_TXD[7]	F1_TXD[7]	F0_TXD[15]		
O	P1_TXEN	F1_TXEN	P1_TXEN	P1_TXEN	F1_TXEN	F0_TXLBE		
I	P1_TXCLK	F1_TXFC		P1_TXCLK	F1_TXFC			
O	P1_TX ERR	F1_TX VALID		P1_TXERR	F1_TXVALID			
O	P1_TXCLK_OUT	F1_TXCLK_OUT	P1_TXCLK_OUT	P1_TXCLK_OUT	F1_TXCLK_OUT			
I	P1_COL			P1_COL				
I	P1_RXD[0]	F1_RXD[0]	P1_RXD[0]	P1_RXD[0]	F1_RXD[0]	F0_RXD[8]		
I	P1_RXD[1]	F1_RXD[1]	P1_RXD[1]	P1_RXD[1]	F1_RXD[1]	F0_RXD[9]		
I	P1_RXD[2]	F1_RXD[2]	P1_RXD[2]	P1_RXD[2]	F1_RXD[2]	F0_RXD[10]		
I	P1_RXD[3]	F1_RXD[3]	P1_RXD[3]	P1_RXD[3]	F1_RXD[3]	F0_RXD[11]		
I	P1_RXD[4]	F1_RXD[4]		P1_RXD[4]	F1_RXD[4]	F0_RXD[12]		
I	P1_RXD[5]	F1_RXD[5]		P1_RXD[5]	F1_RXD[5]	F0_RXD[13]		
I	P1_RXD[6]	F1_RXD[6]		P1_RXD[6]	F1_RXD[6]	F0_RXD[14]		
I	P1_RXD[7]	F1_RXD[7]		P1_RXD[7]	F1_RXD[7]	F0_RXD[15]		
I/O	P1_CRS (I)	F1_RXFC (O)		P1_CRS (I)	F1_RXFC (O)			
I	P1_RXDV	F1_RXEN	P1_RXDV	P1_RXDV	F1_RXEN	F0_RXLBE		
I	P1_RXERR	F1_RXVALID		P1_RXERR	F1_RXVALID			
I	P1_RXCLK	F1_RXCLK	P1_RXCLK	P1_RXCLK	F1_RXCLK			
O	PCI1_AD[56]/ P2_TXD[0]	PCI1_AD[56]/ F2_TXD[0]					PCI1_AD[56]/ P2_TXD[0]	PCI1_AD[56]/ F2_TXD[0]

Table 23: Gigabit Ethernet Unit Pins Multiplexing (Continued)

I/O	Mux Sel = 0x0		Mux Sel = 0x1			Mux Sel = 0x2		
	GbE P0/1/2 (GMII/ TBI/MII)	8-bit FIFO F0/1/2	GbE P0/1/2 (RGMII)	GbE P1 (GMII/TBI/ MII)	8-bit FIFO F1	16-bit FIFO F0	GbE P2 (GMII/TBI/ MII)	8-bit FIFO F2
O	PCI1_AD [57]/ P2_TXD[1]	PCI1_AD [57]/ F2_TXD[1]					PCI1_AD[57]/ P2_TXD[1]	PCI1_AD[57]/ F2_TXD[1]
O	PCI1_AD [58]/ P2_TXD[2]	PCI1_AD [58]/ F2_TXD[2]					PCI1_AD[58]/ P2_TXD[2]	PCI1_AD[58]/ F2_TXD[2]
O	PCI1_AD [59]/ P2_TXD[3]	PCI1_AD [59]/ F2_TXD[3]					PCI1_AD[59]/ P2_TXD[3]	PCI1_AD[59]/ F2_TXD[3]
O	PCI1_AD [60]/ P2_TXD[4]	PCI1_AD [60]/ F2_TXD[4]					PCI1_AD[60]/ P2_TXD[4]	PCI1_AD[60]/ F2_TXD[4]
O	PCI1_AD [61]/ P2_TXD[5]	PCI1_AD [61]/ F2_TXD[5]					PCI1_AD[61]/ P2_TXD[5]	PCI1_AD[61]/ F2_TXD[5]
O	PCI1_AD [62]/ P2_TXD[6]	PCI1_AD [62]/ F2_TXD[6]					PCI1_AD[62]/ P2_TXD[6]	PCI1_AD[62]/ F2_TXD[6]
O	PCI1_AD [63]/ P2_TXD[7]	PCI1_AD [63]/ F2_TXD[7]					PCI1_AD[63]/ P2_TXD[7]	PCI1_AD[63]/ F2_TXD[7]
O	PCI1_AD [54]/ P2_TxEn	PCI1_AD [54]/ F2_TxEn					PCI1_AD[54]/ P2_TxEn	PCI1_AD[54]/ F2_TxEn
I	PCI1_AD [52]/ P2_TXCLK	PCI1_AD [52]/ F2_TXFC					PCI1_AD[52]/ P2_TXCLK	PCI1_AD[52]/ F2_TXFC
O	PCI1_AD [53]/ P2_TXERR	PCI1_AD [53]/ F2_TXVALID					PCI1_AD[53]/ P2_TXERR	PCI1_AD[53]/ F2_TXVALID
O	PCI1_AD [55]/ P2_TXCLK_OUT	PCI1_AD [55]/ F2_TXCLK_OUT					PCI1_AD[55]/ P2_TXCLK_OUT	PCI1_AD[55]/ F2_TXCLK_OUT
I	PCI1_AD[39]/P2_COL	PCI1_AD[39]/NA					PCI1_AD[39]/ P2_COL	PCI1_AD[39]/ NA
I	PCI1_AD [47]/ P2_RXD[0]	PCI1_AD [47]/ F2_RXD[0]					PCI1_AD[47]/ P2_RXD[0]	PCI1_AD[47]/ F2_RXD[0]
I	PCI1_AD [46]/ P2_RXD[1]	PCI1_AD [46]/ F2_RXD[1]					PCI1_AD[46]/ P2_RXD[1]	PCI1_AD[46]/ F2_RXD[1]

Table 23: Gigabit Ethernet Unit Pins Multiplexing (Continued)

I/O	Mux Sel = 0x0		Mux Sel = 0x1			Mux Sel = 0x2		
	GbE P0/1/2 (GMII/ TBI/MII)	8-bit FIFO F0/1/2	GbE P0/1/2 (RGMII)	GbE P1 (GMII/TBI/ MII)	8-bit FIFO F1	16-bit FIFO F0	GbE P2 (GMII/TBI/ MII)	8-bit FIFO F2
I	PCI1_AD [45]/ P2_RXD[2]	PCI1_AD [45]/ F2_RXD[2]					PCI1_AD[45]/ P2_RXD[2]	PCI1_AD[45]/ F2_RXD[2]
I	PCI1_AD [44]/ P2_RXD[3]	PCI1_AD [44]/ F2_RXD[3]					PCI1_AD[44]/ P2_RXD[3]	PCI1_AD[44]/ F2_RXD[3]
I	PCI1_AD [43]/ P2_RXD[4]	PCI1_AD [43]/ F2_RXD[4]					PCI1_AD[43]/ P2_RXD[4]	PCI1_AD[43]/ F2_RXD[4]
I	PCI1_AD [42]/ P2_RXD[5]	PCI1_AD [42]/ F2_RXD[5]					PCI1_AD[42]/ P2_RXD[5]	PCI1_AD[42]/ F2_RXD[5]
I	PCI1_AD [41]/ P2_RXD[6]	PCI1_AD [41]/ F2_RXD[6]					PCI1_AD[41]/ P2_RXD[6]	PCI1_AD[41]/ F2_RXD[6]
I	PCI1_AD [40]/ P2_RXD[7]	PCI1_AD [40]/ F2_RXD[7]					PCI1_AD[40]/ P2_RXD[7]	PCI1_AD[40]/ F2_RXD[7]
I/O	PCI1_AD [51]/ P2_CRS (I)	PCI1_AD [51]/ F2_RXFC (O)					PCI1_AD[51]/ P2_CRS (I)	PCI1_AD[51]/ F2_RXFC (O)
I	PCI1_AD [48]/ P2_RXDV	PCI1_AD [48]/ F2_RXEN					PCI1_AD[48]/ P2_RXDV	PCI1_AD[48]/ F2_RXEN
I	PCI1_AD [50]/ P2_RX ERR	PCI1_AD [50]/ F2_RX VALID					PCI1_AD[50]/ P2_RXERR	PCI1_AD[50]/ F2_RXVALID
I	PCI1_AD [49]/ P2_RXCLK	PCI1_AD [49]/ F2_RXCLK					PCI1_AD[49]/ P2_RXCLK	PCI1_AD[49]/ F2_RXCLK

Notes

- When a Gigabit Ethernet or FIFO port is not used, its input signals must be pulled down, see Table 18 on page 47.
- Px_CRS pins change direction in/out according to the port reset configuration. If Port0 is configured to FIFO interface or if Port2 is configured to RGMII, P0_CRS acts as an output. Otherwise, it is an input (requires a pull down if not used). If Port1 is configured to 8-bit FIFO interface, F1_CRS is an output. Otherwise, it is an input (requires pull down if not used). If Port2 is using the upper PCI1 bus, and the port is configured to 8-bit FIFO interface, F2_CRS is an output. Otherwise, it is an input (requires pull down if not used).

8.2 Gigabit Ethernet Ports I/Os

The 50 Gigabit Ethernet ports pins are located on two separate power segments. This allows having the two segments powered differently. For example, Gigabit Ethernet ports 0 and 2 are on one 1.5V segment, running RGMII in HSTL mode. Meanwhile, port 1 is used as 8-bit FIFO interface powered with 2.5V supply.

Note

If port 2 is using the upper PCI1 pins, it is powered with 3.3V (since it is located on the PCI power segment).

Additionally, each 25 port pins can be configured at reset to act as HSTL pins (differential input) or regular CMOS pin.

The voltage levels of MDC/MDIO when interfacing MII or GMII PHYs are 3.3V. However, when interfacing with an RGMII PHY, the level is 2.5V or even 1.5V, in case of HSTL interface.

As long as the MV64440 interfaces a single PHY device (or multiple devices of the same type), it constantly drives MDC (also MDIO during an SMI write). However, when interfacing two different PHYs that work with different voltage levels (e.g., RGMII and MII), this drive is not appropriate.

When the reset strapping of the Gigabit Ethernet ports indicates that there is a combination of RGMII and MII/GMII/TBI PHYs, the MV64440 treats MDC/MDIO as open drain signals. The signals must be externally pulled up.

Note

Interfacing to two different PHYs that work with different pad types (e.g., RGMII-HSTL and MII-CMOS) isn't supported by the MV64440 MDC and MDIO pads.

For improved signal integrity and board timing design, the Gigabit Ethernet interface pads have a calibration mechanism to control pad drive and impedance. Connect the ETHER_CAL pin to V_ETH0 via a resistor. The resistor size must match the Gigabit Ethernet interface equivalent load. For recommended resistor values, see *TB-119 MV644xx Design Considerations*. After reset de-assertion, the auto-calibration logic tunes the Gigabit Ethernet interface output drivers.

The auto-calibration logic, tunes the entire 50 pins. If the upper PCI1 bus is also used as Gigabit Ethernet port, the auto-calibration mechanism also tunes these pins. It is possible after reset, for the software to change the calibration values via the Ethernet Unit Ports Pads Calibration (EUPCR0/1/2) register (see the Gigabit Ethernet Controller Interface Registers in the *MV64440/1/2 Datasheet User Manual*). This is useful for cases where different ports have different board topology.

Section 9. MV64441 Gigabit Ethernet Pins Multiplexing

The MV64441 contains two Gigabit Ethernet MACs / FIFO interfaces. These interfaces have 50 dedicated pins.

9.1 Gigabit Ethernet Pins Multiplexing

Each port is separately configured at reset to one of the following modes, as described in Table 24

Table 24: Gigabit Ethernet Port/FIFO Interface Reset Configurations

Reset Sample	Mode
0x0	Unused
0x1	TBI
0x2	GMII/MII
0x3	MII only
0x4	8-bit FIFO
0x5	16-bit FIFO
0x6	Reserved
0x7	RGMII

Note

See Table 29 on page 84 for exact reset strapping configuration.

These reset configurations not only define each port operation mode, but also the entire 50 pins multiplexing. The entire set of ports configurations is narrowed down to the three muxing options, named MuxSel. See Table 25 for each pin functionality, per different MuxSel setting.

The possible configurations are:

- Two MII/GMII/TBI Gigabit Ethernet ports 0/1 (MuxSel = 0x0)
- One MII/GMII/TBI Gigabit Ethernet port 0/1 + one 8-bit FIFO port 0/1 (MuxSel = 0x0)
- Two 8-bit FIFO ports 0/1 (MuxSel = 0x0)
- Two RGMII Gigabit Ethernet ports 0/1 (MuxSel = 0x1)
- One RGMII Gigabit Ethernet port 0 + one 8-bit FIFO port 1 (MuxSel = 0x1)
- One RGMII Gigabit Ethernet ports 0 + one MII/GMII/TBI port1 (MuxSel = 0x1)
- One 16-bit FIFO port 0 (MuxSel = 0x2)

Note

It is the user's responsibility to correctly set the reset configuration of each port to a valid configuration. Setting the ports to an unsupported configuration (e.g. two ports configured to 16-bit FIFO interface) will have unpredictable results.

Table 25 shows the different Gigabit Ethernet (GbE) MAC/FIFO interface pins multiplexing.

Table 25: Gigabit Unit Pins Multiplexing

I/O	Mux Sel = 0x0		Mux Sel = 0x1			Mux Sel = 0x2
	GbE P0/1 (GMII/TBI/ MII)	8-bit FIFO F0/1	GbE P0/1 (RGMII)	GbE P1 (GMII/TBI/ MII)	8-bit FIFO F1	16-bit FIFO F0
O	P0_TXD[0]	F0_TXD[0]	P0_TXD[0]			F0_TXD[0]
O	P0_TXD[1]	F0_TXD[1]	P0_TXD[1]			F0_TXD[1]
O	P0_TXD[2]	F0_TXD[2]	P0_TXD[2]			F0_TXD[2]
O	P0_TXD[3]	F0_TXD[3]	P0_TXD[3]			F0_TXD[3]
O	P0_TXD[4]	F0_TXD[4]				F0_TXD[4]
O	P0_TXD[5]	F0_TXD[5]				F0_TXD[5]
O	P0_TXD[6]	F0_TXD[6]				F0_TXD[6]
O	P0_TXD[7]	F0_TXD[7]				F0_TXD[7]
O	P0_TXEN	F0_TXEN	P0_TXEN			F0_TXEN
I	P0_TXCLK	F0_TXFC				F0_TXFC
O	P0_TXERR	F0_TXVALID				F0_TXVALID
O	P0_TXCLK_OUT	F0_TXCLK_OUT	P0_TXCLK_OUT			F0_TXCLK_OUT
I	P0_COL					
I	P0_RXD[0]	F0_RXD[0]	P0_RXD[0]			F0_RXD[0]
I	P0_RXD[1]	F0_RXD[1]	P0_RXD[1]			F0_RXD[1]
I	P0_RXD[2]	F0_RXD[2]	P0_RXD[2]			F0_RXD[2]
I	P0_RXD[3]	F0_RXD[3]	P0_RXD[3]			F0_RXD[3]
I	P0_RXD[4]	F0_RXD[4]				F0_RXD[4]
I	P0_RXD[5]	F0_RXD[5]				F0_RXD[5]
I	P0_RXD[6]	F0_RXD[6]				F0_RXD[6]
I	P0_RXD[7]	F0_RXD[7]				F0_RXD[7]
I/O	P0_CRS (I)	F0_RXFC0 (O)				F0_RXFC0 (O)
I	P0_RXDV	F0_RXEN	P0_RXDV			F0_RXEN
I	P0_RXERR	F0_RXVALID				F0_RXVALID
I	P0_RXCLK	F0_RXCLK	P0_RXCLK			F0_RXCLK
O	P1_TXD[0]	F1_TXD[0]	P1_TXD[0]	P1_TXD[0]	F1_TXD[0]	F0_TXD[8]
O	P1_TXD[1]	F1_TXD[1]	P1_TXD[1]	P1_TXD[1]	F1_TXD[1]	F0_TXD[9]
O	P1_TXD[2]	F1_TXD[2]	P1_TXD[2]	P1_TXD[2]	F1_TXD[2]	F0_TXD[10]
O	P1_TXD[3]	F1_TXD[3]	P1_TXD[3]	P1_TXD[3]	F1_TXD[3]	F0_TXD[11]
O	P1_TXD[4]	F1_TXD[4]		P1_TXD[4]	F1_TXD[4]	F0_TXD[12]

Table 25: Gigabit Unit Pins Multiplexing (Continued)

I/O	Mux Sel = 0x0		Mux Sel = 0x1			Mux Sel = 0x2
	GbE P0/1 (GMII/TBI/ MII)	8-bit FIFO F0/1	GbE P0/1 (RGMII)	GbE P1 (GMII/TBI/ MII)	8-bit FIFO F1	16-bit FIFO F0
O	P1_TXD[5]	F1_TXD[5]		P1_TXD[5]	F1_TXD[5]	F0_TXD[13]
O	P1_TXD[6]	F1_TXD[6]		P1_TXD[6]	F1_TXD[6]	F0_TXD[14]
O	P1_TXD[7]	F1_TXD[7]		P1_TXD[7]	F1_TXD[7]	F0_TXD[15]
O	P1_TXEN	F1_TXEN	P1_TXEN	P1_TXEN	F1_TXEN	F0_TXLBE
I	P1_TXCLK	F1_TXFC		P1_TXCLK	F1_TXFC	
O	P1_TXERR	F1_TXVALID		P1_TXERR	F1_TXVALID	
O	P1_TXCLK_ OUT	F1_TXCLK_ OUT	P1_TXCLK_ OUT	P1_TXCLK_ OUT	F1_TXCLK_ OUT	
I	P1_COL			P1_COL		
I	P1_RXD[0]	F1_RXD[0]	P1_RXD[0]	P1_RXD[0]	F1_RXD[0]	F0_RXD[8]
I	P1_RXD[1]	F1_RXD[1]	P1_RXD[1]	P1_RXD[1]	F1_RXD[1]	F0_RXD[9]
I	P1_RXD[2]	F1_RXD[2]	P1_RXD[2]	P1_RXD[2]	F1_RXD[2]	F0_RXD[10]
I	P1_RXD[3]	F1_RXD[3]	P1_RXD[3]	P1_RXD[3]	F1_RXD[3]	F0_RXD[11]
I	P1_RXD[4]	F1_RXD[4]		P1_RXD[4]	F1_RXD[4]	F0_RXD[12]
I	P1_RXD[5]	F1_RXD[5]		P1_RXD[5]	F1_RXD[5]	F0_RXD[13]
I	P1_RXD[6]	F1_RXD[6]		P1_RXD[6]	F1_RXD[6]	F0_RXD[14]
I	P1_RXD[7]	F1_RXD[7]		P1_RXD[7]	F1_RXD[7]	F0_RXD[15]
I/O	P1_CRS (I)	F1_RXFC (O)		P1_CRS (I)	F1_RXFC (O)	
I	P1_RXDV	F1_RXEN	P1_RXDV	P1_RXDV	F1_RXEN	F0_RXLBE
I	P1_RXERR	F1_RXVALID		P1_RXERR	F1_RXVALID	
I	P1_RXCLK	F1_RXCLK	P1_RXCLK	P1_RXCLK	F1_RXCLK	

Notes

- When a Gigabit Ethernet or FIFO port is not used, its input signals must be pulled down.
- Px_CRS pins change direction in/out according to the port reset configuration. If Port0 is configured to an 8-bit FIFO interface, P0_CRS acts as an output. Otherwise, it is an input (requires a pull down if not used). If Port1 is configured to an 8-bit FIFO interface, F1_CRS is an output. Otherwise, it is an input (requires pull down if not used).

9.2 Gigabit Ethernet Ports I/Os

The 50 Gigabit Ethernet ports pins are located on two separate power segments. This allows having the two segments powered differently. For example, Gigabit Ethernet ports 0 and 2 are on one 1.5V segment, running RGMII in HSTL mode. Meanwhile, port 1 is used as 8-bit FIFO interface powered with 2.5V supply.

Additionally, each 25 port pins can be configured at reset to act as HSTL pins (differential input) or regular CMOS pin.

The voltage levels of MDC/MDIO when interfacing MII or GMII phys are 3.3V. However, when interfacing with RGMII PHYs, the level is 2.5V or even 1.5V, in case of HSTL interface.

As long as the MV64441 interfaces a single PHY device (or multiple devices of the same type), it constantly drives MDC (also MDIO during an SMI write). However, when interfacing two different phys that work with different voltage levels (e.g., RGMII and MII), this drive is not appropriate.

When the reset strapping of the Gigabit Ethernet ports indicates that there is a combination of RGMII and MII/GMII/TBI phys, the MV64441 treats MDC/MDIO as open drain signals. The signals must be externally pulled up.

Note

Interfacing to two different phys that work with different pad types (e.g., RGMII-HSTL and MII-CMOS) isn't supported by the MV64440 MDC and MDIO pads.

For improved signal integrity and board timing design, the Gigabit Ethernet interface pads have a calibration mechanism to control pad drive and impedance. Connect the ETHER_CAL pin to V_ETH0 via a resistor. The resistor size must match the Gigabit Ethernet interface equivalent load. For recommended resistor values, see *TB-119 MV644xx Design Considerations*. After reset de-assertion, the auto-calibration logic tunes the Gigabit Ethernet interface output drivers.

The auto-calibration logic, tunes the entire 50 pins. If the upper PCI1 bus is also used as Gigabit Ethernet port, the auto-calibration mechanism also tunes these pins. It is possible after reset, for the software to change the calibration values via he Ethernet Unit Ports Pads Calibration (EUPCR0/1/2) register (see the Gigabit Ethernet Controller Interface Registers in the *MV64440/1/2 Datasheet User Manual*). This is useful for cases where different ports have different board topology.

Section 10. MV64442 Gigabit Ethernet Pins Multiplexing

The MV64440/1/2 contains one Gigabit Ethernet MACs / FIFO interfaces. These interfaces have 25 dedicated pins

10.1 Gigabit Ethernet Pins Multiplexing

Each port is separately configured at reset to one of the following modes, as described in Table 26

Table 26: Gigabit Ethernet Port/FIFO Interface Reset Configurations

Reset Sample	Mode
0x0	Unused
0x1	TBI
0x2	GMII/MII
0x3	MII only
0x4	8-bit FIFO
0x5	Reserved
0x6	Reserved
0x7	RGMII

Note

See Table 29 on page 84 for exact reset strapping configuration.

These reset configurations not only define the port operation mode, but also the entire 25 pins multiplexing. The entire set of configurations is narrowed down to the two muxing options, named MuxSel. See Table 27 for each pin functionality, per different MuxSel setting.

The possible configurations are:

- One MII/GMII/TBI Gigabit Ethernet ports 0 (MuxSel = 0x0)
- One 8-bit FIFO ports 0 (MuxSel = 0x0)
- One RGMII Gigabit Ethernet ports 0 (MuxSel = 0x1)

Note

It is the user responsibility to correctly set the reset configuration of each port to a valid configuration. Setting the ports to an unsupported configuration (e.g. configured to 16-bit FIFO interface) will have unpredictable results.

Table 27 shows the different Gigabit Ethernet (GbE) MAC/FIFO interface pins multiplexing.

Table 27: Gigabit Unit Pins Multiplexing

I/O	Mux Sel = 0x0		Mux Sel = 0x1
	GbE P0 (GMII/TBI/MII)	8-bit FIFO F0	GbE P0(RGMII)
O	P0_TXD[0]	F0_TXD[0]	P0_TXD[0]
O	P0_TXD[1]	F0_TXD[1]	P0_TXD[1]
O	P0_TXD[2]	F0_TXD[2]	P0_TXD[2]
O	P0_TXD[3]	F0_TXD[3]	P0_TXD[3]
O	P0_TXD[4]	F0_TXD[4]	
O	P0_TXD[5]	F0_TXD[5]	
O	P0_TXD[6]	F0_TXD[6]	
O	P0_TXD[7]	F0_TXD[7]	
O	P0_TXEN	F0_TXEN	P0_TXEN
I	P0_TXCLK	F0_TXFC	
O	P0_TXERR	F0_TXVALID	
O	P0_TXCLK_OUT	F0_TXCLK_OUT	P0_TXCLK_OUT
I	P0_COL		
I	P0_RXD[0]	F0_RXD[0]	P0_RXD[0]
I	P0_RXD[1]	F0_RXD[1]	P0_RXD[1]
I	P0_RXD[2]	F0_RXD[2]	P0_RXD[2]
I	P0_RXD[3]	F0_RXD[3]	P0_RXD[3]
I	P0_RXD[4]	F0_RXD[4]	
I	P0_RXD[5]	F0_RXD[5]	
I	P0_RXD[6]	F0_RXD[6]	
I	P0_RXD[7]	F0_RXD[7]	
I/O	P0_CRS (I)	F0_RXFC0 (O)	
I	P0_RXDV	F0_RXEN	P0_RXDV
I	P0_RXERR	F0_RXVALID	
I	P0_RXCLK	F0_RXCLK	P0_RXCLK

Notes

- When a Gigabit Ethernet or FIFO port is not used, its input signals must be pulled down.
- P0_CRS pins change direction in/out according to the port reset configuration. If Port0 is configured to FIFO interface, P0_CRS acts as an output. Otherwise, it is an input (requires a pull down if not used).

10.2 Gigabit Ethernet Ports I/Os

Each of the 25 Gigabit Ethernet pins can be configured at reset to act as HSTL pins (differential input) or regular CMOS pin.

The voltage levels of MDC/MDIO when interfacing MII or GMII PHYs are 3.3V. However, when interfacing RGMII PHY, the level is 2.5V or even 1.5V, in case of HSTL interface.

For improved signal integrity and board timing design, the Gigabit Ethernet interface pads have a calibration mechanism to control pad drive and impedance. Connect the ETHER_CAL pin to V_ETH0 via a resistor. The resistor size must match the Gigabit Ethernet interface equivalent load. For recommended resistor values, see *TB-119 MV644xx Design Considerations*. After reset de-assertion, the auto-calibration logic tunes the Gigabit Ethernet interface output drivers.

The auto-calibration logic, tunes the entire 50 pins. If the upper PCI1 bus is also used as Gigabit Ethernet port, the auto-calibration mechanism also tunes these pins. It is possible after reset, for the software to change the calibration values via he Ethernet Unit Ports Pads Calibration (EUPCR0/1/2) register (see the Gigabit Ethernet Controller Interface Registers in the *MV64440/1/2 Datasheet User Manual*). This is useful for cases where different ports have different board topology.

Section 11. Multi Purpose Pins Multiplexing

The MV64440/1/2 device contains 32 Multi Purpose Pins (MPP). Each one can be assigned to a different functionality through the MPP Control register. The MPP pins can be used as hardware control signals to the MV64440/1/2 device's different interfaces (e.g., DMA).

- GPIO: General Purpose In/Out Port, see the General Purpose I/O Port section in the *MV64440/1/2 Datasheet User Manual.*
- PCIx_REQn[5:0]/PCIx_GNTn[5:0]: PCI Arbitration Signals, see the PCI Interface section in the *MV64440/1/2 Datasheet User Manual.*
- Sx_TXD/Sx_RXD/Sx_CTS/Sx_CD/Sx_RTS/Sx_SCLK/Sx_TSCLK: Serial Port Signals, see the Multi Protocol Serial Controllers section in the *MV64440/1/2 Datasheet User Manual.*
- DEV_BURSTn: Device Bus Data Burst, see the Device Controller section in the MV64440/1/2 *Datasheet User Manual.*
- PCIx_PMEn: Power Management Event, see the PCI Interface section in the *MV64440/1/2 Datasheet User Manual.*
- INITACT: Serial Initialization Active, see Section 13.3 "Serial ROM Initialization" on page 90.
- DMA_REQn[3:0]/DMA_EOTn[3:0]/DMA_ACKn[3:0]: DMA Signals, see the IDMA Controller section in the *MV64440/1/2 Datasheet User Manual.*
- WD_NMIn/WD_En: Watchdog Timer, see the Watchdog Timer section in the *MV64440/1/2 Datasheet User Manual.*
- BCLK_IN/BCLK_OUT: Baud Regenerator Clock Input/Output, see the Baud Rate Generators section in the *MV64440/1/2 Datasheet User Manual*.
- TC_ENn[3:0]/TC_NTn[3:0]: Timer/Counter Signals, see the Timer/Counters section in the *MV64440/1/2 Datasheet User Manual*.
- DEBUG[31:0]: For Marvell usage.

11.1 MPP Multiplexing

Table 28 shows each MPP pins' functionality as determined by the MPP Multiplex register, see the Pins Multiplexing Interface Registers section in the *MV64440/1/2 Datasheet User Manual*.

Table 28: MPP Function Summary

MPP Pin	0x0	0x1	0x2	0x3	0x4	0xF
MPP[0]	GPIO[0]	PCI1_GNTn[0]	S0_TXD	S1_CD	DEV_BURSTn	DEBUG[0]
MPP[1]	GPIO[1]	PCI1_REQn[0]	S0_RXD	S1_SCLK	PCI1_PMEn	DEBUG[1]
MPP[2]	GPIO[2]	PCI1_GNTn[1]	S0_RTS	S1_TSCLK	DEV_BURSTn	DEBUG[2]
MPP[3]	GPIO[3]	PCI1_REQn[1]	S0_CTS	S1_TXD	INITACT	DEBUG[3]
MPP[4]	GPIO[4]	PCI1_GNTn[2]	S0_CD	S1_TXD	DEV_BURSTn	DEBUG[4]
MPP[5]	GPIO[5]	PCI1_REQn[2]	S0_SCLK	S1_RXD	PCI1_PMEn	DEBUG[5]
MPP[6]	GPIO[6]	PCI1_GNTn[3]	S0_TSCLK	S1_RTS	DEV_BURSTn	DEBUG[6]

Table 28: MPP Function Summary (Continued)

MPP Pin	0x0	0x1	0x2	0x3	0x4	0xF
MPP[7]	GPIO[7]	PCI1_REQn[3]	S0_TXD	S1_CTS	INITACT	DEBUG[7]
MPP[8]	GPIO[8]	PCI1_GNTn[4]	S0_TXD	S1_CD	DEV_BURSTn	DEBUG[8]
MPP[9]	GPIO[9]	PCI1_REQn[4]	S0_RXD	S1_SCLK	PCI1_PMEn	DEBUG[9]
MPP[10]	GPIO[10]	PCI1_GNTn[5]	S0_RTS	S1_TSCLK	DEV_BURSTn	DEBUG[10]
MPP[11]	GPIO[11]	PCI1_REQn[5]	S0_CTS	S1_RXD	INITACT	DEBUG[11]
MPP[12]	GPIO[12]	PCI1_GNTn[0]	S0_CD	S1_TXD	DEV_BURSTn	DEBUG[12]
MPP[13]	GPIO[13]	PCI1_REQn[0]	S0_SCLK	S1_RTS	PCI1_PMEn	DEBUG[13]
MPP[14]	GPIO[14]	PCI1_GNTn[1]	S0_TSCLK	S1_RXD	DEV_BURSTn	DEBUG[14]
MPP[15]	GPIO[15]	PCI1_REQn[1]	S0_RXD	S1_CTS	INITACT	DEBUG[15]
MPP[16]	GPIO[16]	PCI0_GNTn[0]	DMA_REQn[0]	INITACT	WD_NMIn	DEBUG[16]
MPP[17]	GPIO[17]	PCI0_REQn[0]	DMA_ACKn[0]	DMA_EOTn[3]	WD_En	DEBUG[17]
MPP[18]	GPIO[18]	PCI0_GNTn[1]	DMA_REQn[1]	PCI0_PMEn	WD_NMIn	DEBUG[18]
MPP[19]	GPIO[19]	PCI0_REQn[1]	DMA_ACKn[1]	DMA_EOTn[2]	WD_En	DEBUG[19]
MPP[20]	GPIO[20]	PCI0_GNTn[2]	DMA_REQn[2]	INITACT	BCLK_IN	DEBUG[20]
MPP[21]	GPIO[21]	PCI0_REQn[2]	DMA_ACKn[2]	DMA_EOTn[1]	BCLK_IN	DEBUG[21]
MPP[22]	GPIO[22]	PCI0_GNTn[3]	DMA_REQn[3]	PCI0_PMEn	BCLK_OUT	DEBUG[22]
MPP[23]	GPIO[23]	PCI0_REQn[3]	DMA_ACKn[3]	DMA_EOTn[0]	BCLK_OUT	DEBUG[23]
MPP[24]	GPIO[24]	PCI0_GNTn[4]	TC_ENn[0]	INITACT	WD_NMIn	DEBUG[24]
MPP[25]	GPIO[25]	PCI0_REQn[4]	TC_NTn[0]	DMA_EOTn[3]	WD_En	DEBUG[25]
MPP[26]	GPIO[26]	PCI0_GNTn[5]	TC_ENn[1]	PCI0_PMEn	WD_NMIn	DEBUG[26]
MPP[27]	GPIO[27]	PCI0_REQn[5]	TC_NTn[1]	DMA_EOTn[2]	WD_En	DEBUG[27]
MPP[28]	GPIO[28]	PCI0_GNTn[0]	TC_ENn[2]	INITACT	BCLK_IN	DEBUG[28]
MPP[29]	GPIO[29]	PCI0_REQn[0]	TC_NTn[2]	DMA_EOTn[1]	BCLK_IN	DEBUG[29]
MPP[30]	GPIO[30]	PCI0_GNTn[1]	TC_ENn[3]	PCI0_PMEn	BCLK_OUT	DEBUG[30]
MPP[31]	GPIO[31]	PCI0_REQn[1]	TC_NTn[3]	DMA_EOTn[0]	BCLK_OUT	DEBUG[31]

Note

Depending on its configured functionality, each pin might act as output or input pin. All MPP pins wake up after reset as GPIO input pins.

When programming the four MPP Control registers to 0xFFFF.FFFF, the 32-bit MPP bus is used as a debug port. The debug port gives visibility of internal signals on the external pins, and is reserved for Marvell usage.

11.2 MPP I/O Pads

The 32 MPPs are 5V tolerant. This is useful, when interfacing 5V legacy devices. For example, if the MPPs are used as a PCI bus arbiter PCIx_REQn/GNTn signals, and interfacing 5V PCI master. Another example would be, when used as GPIO input, registering external 5V interrupt inputs.

Note

The MPP pads have integrated clamping diodes as the PCI pads that clamp the input voltage to VREF. MPP[15:0] are clamped to PCI1_VREF and MPP[31:16] to PCI0_VREF. If VREF is 3.3V, the corresponding MPPs must not be used with 5V signaling. Also, if not using PCI at all, the VREF pins can be left unconnected, so to eliminate the MPPs clamping.

The MPPs pads have configurable output impedance. The MPPs are divided into two groups – MPP[15:0] and MPP[31:16]. Each group shares the same pad calibration logic. After reset:

- The MPP[15:0] pads output buffers are automatically tuned according to the impedance defined by an external resistor attached to pin PCI1_CAL (same tuning as the PCI1 pads).
- The MPP[31:16] pads drive is tuned according to the impedance defined by an external resistor attached to pin PCI0_CAL (same tuning as PCI0 pads).

Later, the MPPs drive strength can be changed via the PCI/MPP Pads Calibration register (see the PCI Interface Registers section in the *MV64440/1/2 Datasheet User Manual*.

Section 12. Clocking

The MV64440/1/2 device has multiple clock domains.

- SYS_CLK: The CPU bus clock, also used as the reference clock for the MV64440/1/2 DRAM clock. Up to 200 MHz.
- TCLK: The MV64440/1/2 core clock, also used as the reference clock for the MV64440/1/2 device bus and MPPs. Up to 133 MHz.

Notes

- Unlike the MV643xx device, the MV64440/1/2 does not support the CPU bus running at slower frequency than DRAM.
- Unlike the MV643xx device, the MV64440/1/2 SYS_CLK is powered from a separate power segment VDD_CLK, that enables driving the CPU and MV64440/1/2 from the same clock source.

- PCI0 clock: Up to 66 MHz in conventional PCI mode, and up to 133 MHz in PCI-X mode.
- PCI1 clock: Up to 66 MHz in conventional PCI mode, and up to 133 MHz in PCI-X mode.
- CLK125: This is the Gigabit Ethernet reference clock. Up to 125 MHz in GMII or TBI modes.
- FIFOCLK: FIFO interface reference clock. Up to 133 MHz.
- SCLK and TSCLK: MPSCs clocks, muxed on the MPP pins. Up to 50 MHz.
- SCK: TWSI clock. 400 KHz.

Notes

- The TCLK frequency must be greater than 83 MHz. The SYS_CLK frequency must be greater than 100 MHz. The SYS_CLK frequency cannot be more than twice as fast as the TCLK frequency.
- The PCI clock frequency must not exceed the TCLK frequency. Also, the TCLK clock frequency must not exceed the SYS_CLK frequency.

12.1 PLL and DLL

The MV64440/1/2 has the following on-chip de-skew PLL s and DLLs to improve its AC timing, to compensate on clock trees delays.

- SYS_CLK PLL: Drives the CPU/DRAM interface clock tree.
- TCLK PLL: Drives the core clock tree.
- PCI0/1 DLL: Used in 66 MHz conventional PCI mode and 133 MHz in PCI-X mode for driving the PClk clock tree.

12.2 PLL Power Supply

The MV64440/1/2 PLLs and DLLs uses the regular digital VDD and VSS power supplies, as well as the following analog quite power supplies:

- PLL0_VDDAH: SYS_CLK PLL analog power supply (2.5V)
- PLL0_VSSA: Quiet ground
- PLL1_VDDAH: TCLK PLL analog power supply (2.5V)
- PLL1_VSSA: Quiet ground
- DLL0_VDDAH: PCIx DLL Digital power supply (1.5V)
- DLL0_VSSA: Quiet ground
- DLL1_VDDAH: PCIx DLL analog power supply (1.5V)
- DLL1_VSSA: Quiet ground

Section 13. Reset Pins and Configuration

The MV64440/1/2 has three reset pins:

- SYSRSTn: Resets the entire MV64440/1/2 device
- PCI0_RSTn: Resets PCI0
- PCI1_RSTn: Resets PCI1

SYSRSTn assertion floats the rest of the chip interfaces, except for the following signals that are always driven:

- The DRAM interface's M_RASn, M_CASn, M_WEn, and M_CSn[3:0] signals.
- The TWSI interface's SDA and SCK signals.

While PCIx_RSTn is asserted, the corresponding PCI interface's I/Os are floated.

For additional information on PCI reset, see Table 7 on page 30 or Table 8 on page 33.

Note

Pad calibration takes 280 SYS_CLK cycles following SYSRSTn de-assertion. The CPU must not access the MV64440/1/2 device during calibration time. The CPU must be held in a reset state for 280 SYS_CLK cycles, following MV64440/1/2 SYS_RST de-assertion.

13.1 Reset Timing

One millisecond (1 ms) is the minimum period between power up and deactivating the MV644xx reset. The minimum reset active time unrelated to power up is 150 ns.

13.2 Pins Sample Configuration

The following configuration pins are sampled during SYSRSTn assertion. These signals must be kept pulled up or down until SYSRSTn de-assertion (zero Hold time in respect to SYSRSTn de-assertion).

Note

If external logic is used instead of pull up and pull down resistors, the logic must drive all of the signals to the desired values during SYSRSTn assertion. The external logic must float the bus no later than the third cycle after SYSRSTn de-assertion until normal operation occurs.

Table 29: Reset Configuration

Pin	Configuration Function
DEV_AD[0]	Serial ROM initialization
	0 = Disabled 1 = Enabled

Table 29: Reset Configuration (Continued)

Pin	Configuration Function
DEV_AD[1]	DRAM Pads Auto-calibration
	0 = Disable 1 = Enable
DEV_AD[3:2]	Serial ROM Address
	00 = ROM address is 1010000 01 = ROM address is 1010001 10 = ROM address is 1010010 11 = ROM address is 1010011 **NOTE:** If not using serial ROM initialization (DEV_AD[0] sampled LOW), DEV_AD[3:2] can be left with no pullup/pulldown
DEV_AD[4]	CPU Bus Endianess
	0 = Big endian 1 = Little endian
DEV_AD[5]	Default Internal Space Base
	0 = 0x1400.0000 1 = 0xF100.0000
DEV_AD[7:6]	CPU Bus Configuration
	00 = Reserved 01 = Reserved 10 = SysAD bus 11 = Reserved
DEV_AD[8]	CPU Pads Auto-calibration
	0 = Disable 1 = Enable
DEV_AD[9]	Reserved
	Must pull low.
DEV_AD[11:10]	Reserved
	Reserved **NOTE:**
DEV_AD[12]	PCI0 Pads Auto-calibration
	0 = Disable 1 = Enable

Table 29: Reset Configuration (Continued)

Pin	Configuration Function
DEV_AD[13]	PCI1 Pads Auto-calibration
	0 = Disable 1 = Enable
DEV_AD[15:14]	DEV_BOOTCSn Device Width
	00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = Reserved
DEV_AD[16]	PCI Retry
	0 = Disable 1 = Enable
DEV_AD[17]	CPU Interface Type
	0 = HSTL 1 = CMOS
DEV_AD[18]	Sync Mode
	Must pull low.
DEV_AD[19]	DDR SDRAM Address/Control Delay
	0 = DRAM address/control signals toggle on falling edge of DRAM clock. 1 = DRAM address/control signals toggle on rising edge of DRAM clock. The DEV_AD[19] setting depends on board topology and DRAM load. For detailed recommendations, see *TB-119: MV644xx Design Considerations*.
DEV_AD[20]	Reserved
	Must pull low.
DEV_AD[21]	Reserved
	Reserved for future use. Board design should support future pull up/pull down requirement on this pin. **NOTE:** Can be left with no pullup/pulldown.
DEV_AD[22]	SYS_CLK PLL Control (Depending on CPU interface signaling.)
	0 = VDD_CLK is tied to HSTL 1.5V 1 = VDD_CLK is tied to LVTTL 3.3V or LVCMOS 2.5V **NOTE:** Subject to change.

Table 29: Reset Configuration (Continued)

Pin	Configuration Function
DEV_AD[23]	Test
	Must pull high. 0 = Test. Reserved for Marvell usage. 1 = Normal operation
DEV_AD[24]	Test
	Must pull high. 0 = Test. Reserved for Marvell usage. 1 = Normal operation
DEV_AD[25]	**MV64440**: PCI_1 pins multiplexing **MV64441 and MV64442**: Pull Down
	0 = PCI_1 is a 64-bit interface. 1 = PCI1_AD[63:40] pins are used for Gigabit Ethernet port or FIFO interface.
DEV_AD[28:26]	PCI_1 DLL control
	100 for all modes. **NOTE:** Subject to change. For further details about the PCI re-sampling mode, see the notes after Table 30 on page 89.
DEV_AD[31:29]	PCI_0 DLL control
	100 for all modes. **NOTE:** Subject to change. For further details about the PCI re-sampling mode, see the notes after Table 30 on page 89.
P0_TXD[2:0]	Gigabit Ethernet Port0 Mode Select
	000 = Unused 001 = TBI 010 = GMII/MII 011 = MII only 100 = 8-bit FIFO 101 = 16-bit FIFO 110 = Reserved 111 = RGMII
P1_TXD[2:0]	Gigabit Ethernet port1 Mode Select
	Same as Gigabit Ethernet port0 Mode Select **NOTE:** Only valid for the MV64440 and MV64441 devices. Reserved in the MV64442 device.

Table 29: Reset Configuration (Continued)

Pin	Configuration Function
P1_TXD[5:3]	Gigabit Ethernet port2 Mode Select
	Same as Gigabit Ethernet port0 Mode Select **NOTE:** Relevant for the MV64440 device, reserved in the MV64442 and must be tied to pull-downs in the MV64441 device.
P0_TXD[7]	JTAG Pad Calibration Bypass
	0 = Normal Operation 1 = Bypass all pad calibration **NOTE:** When required to bypass the pad calibration sequence, for example in a JTAG operation, sampling this signal high results in a consistent value setting for all calibration interfaces, without calibrating the values according to the external resistors values.
DEV_WEn[0]	SYS_CLK PLL Bypass
	0 = Normal Operation 1 = Bypass PLL
DEV_WEn[3:1]	SYS_CLK PLL Control
	001 = VDD_CLK is tied to LVTTL 3.3V 010 = VDD_CLK is tied to LVCMOS 2.5V 011 = VDD_CLK is tied to HSTL 1.5V **NOTE:** Subject to change.
DEV_DP[0]	SYS_CLK Input Mode
	0 = HSTL 1 = CMOS
P0_TXD[3]	TCLK PLL Bypass
	0 = Normal Operation 1 = Bypass PLL
P0_TXD[6:4]	TCLK PLL Control
	Tuning of TCLK PLL clock tree. Set to 000. **NOTE:** May be changed following silicon testing
DEV_DP[3]	Gigabit Ethernet Port0 I/O Type
	0 = HSTL 1 = CMOS **NOTE:** Controls the pad type for the 25 Gigabit Ethernet port 0 pins.

Table 29: Reset Configuration (Continued)

Pin	Configuration Function
DEV_DP[2]	Gigabit Ethernet Port1 I/O Type **NOTE:** Only applies to the MV64440 and MV64441 devices. Reserved for the MV64442.
	0 = HSTL 1 = CMOS **NOTE:** Controls the pad type for the 25 Gigabit Ethernet port 1 pins.
DEV_BADR[0]	Must pull down
DEV_BADR[1]	Must pull down
	NOTE:
DEV_BADR[2]	Gigabit Ethernet Pads Auto-calibration
	0 = Disable 1 = Enable
DEV_DP[1]	Test
	Must pull high. 0 = Test mode. Reserved for Marvell usage. 1 = Normal operation
P1_TXD[7:6]	Reserved
	Reserved for future use. Board design should support future pull up/pull down requirement on these pins. **NOTE:** Can be left with no pullup/pulldown.

Note

All reset sampled values are registered in Reset Sample (Low) and Reset Sample (High) registers (see the CPU Interface Registers in the *MV64440/1/2 Datasheet User Manual*). This is useful for board debug.

Part of the PCI interface signals are also sampled on PCI reset de-assertion, as specified in the PCI specification.

Table 30: PCI Reset Configuration

Pin	Configuration Function
PCI0_64ENn	PCI0 64-bit Enable **NOTE:** Only applies to the MV64440 and MV64442 devices.
	0 = Enabled. PCI interface is working in 64-bit mode. 1 = Disabled. PCI interface is working in 32-bit mode.

Table 30: PCI Reset Configuration (Continued)

Pin	Configuration Function
PCI0_M66EN	PCI0 66 MHz Enable
	0 = Disabled 1 = Enabled **NOTE:** Relevant only to conventional PCI mode
PCI0_DEVSELn PCI0_STOPn PCI0_TRDYn	PCI0 Mode
	111 = Conventional PCI 110 = 66 MHz PCI-X 101 = 100 MHz PCI-X 100 = 133 MHz PCI-X All other combinations are Reserved
PCI1_REQ64n	PCI1 64-bit Enable
	Same as PCI0_64ENn. **NOTE:** Only applies to the MV64440 device.
PCI1_M66EN	PCI_1 66 MHz Enable
	Same as PCI0
PCI1_DEVSELn PCI1_STOPn PCI1_TRDYn	PCI1 Mode
	Same as PCI0 Mode

Notes

- When configured to 32-bit PCI (PCIx_64ENn sampled high), the MV64440 and MV64441 drives the upper side of the PCI bus (PCIx_AD[63:32], PCIx_CBEn[7:4], PCIx_PAR64).
- The correct values for PCIx_M66EN, PCIx_DEVSELn, PCIx_STOPn, and PCIx_TRDYn must be driven during SYSRSTn de-assertion. If PCIx_RST is de-asserted after SYSRSTn de-assertion, these pins must be driven with the correct configuration before SYSRSTn is de-asserted.
- When configured to conventional PCI mode, PCIx_M66EN is used to enable/disable the PCI interface internal DLL. The DLL is only enabled in 66 MHz PCI mode.

13.3 Serial ROM Initialization

The MV64440/1/2 device supports initialization of ALL its internal and configuration registers and other system components through the TWSI master interface. If serial ROM initialization is enabled, the MV64440/1/2 device TWSI master starts reading initialization data from the serial ROM and writes it to the appropriate registers (or to any of the MV64440/1/2 device interfaces, according to address decoding).

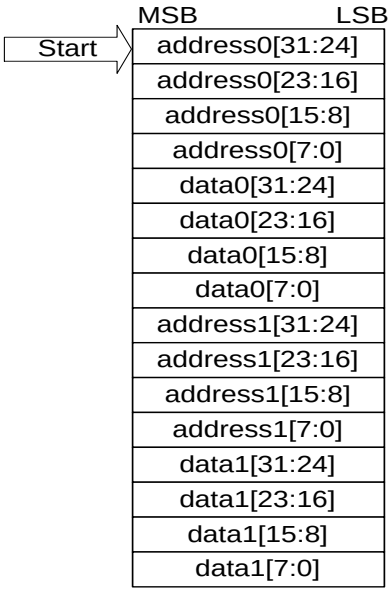
Notes

- While serial ROM is active the INITACT is driven high.
- Since INITACT signal is multiplex on the MPP interface, the code on the serial interface must make sure that the corresponding MPP pin is correctly configured to drive the INITACT signal.
- Since the INITACT signal is not driven before reset, the system must pull it to 1 (active state).

13.3.1 Serial ROM Data Structure

The serial ROM data structure consists of a 32-bit address and 32-bit data pairs sequence, as shown in Figure 13.

Figure 13: Serial ROM Data Structure



The serial ROM initialization logic shares the address decoding registers of the MPSCs. It reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on the address decoding result, writes the next four bytes to the required target. This scheme enables the programming of the MV64440/1/2 internal registers and the initialization of other system components. Its only limitation is that it supports only single 32-bit writes (no byte enables nor bursts are supported). For example, it is possible to:

- Program the MV64440/1/2 internal registers by setting addresses that match the internal registers space (default address is 0x14000XXX).
- Program the MV64440/1/2 PCI configuration registers using the PCI Configuration Address and PCI Configuration Data registers, see (see the PCI Interface Registers in the *MV64440/1/2 Datasheet User Manual*).
- Initialize other devices on the PCI bus by initiating PCI write transactions.

The Serial Init Last Data register (see the Serial Initialization Interface Registers in the *MV64440/1/2 Datasheet User Manual) contains* the expected value of last serial data item (default value is 0xffffffff). When the MV64440/1/2 reaches last data, it stops the initialization sequence.

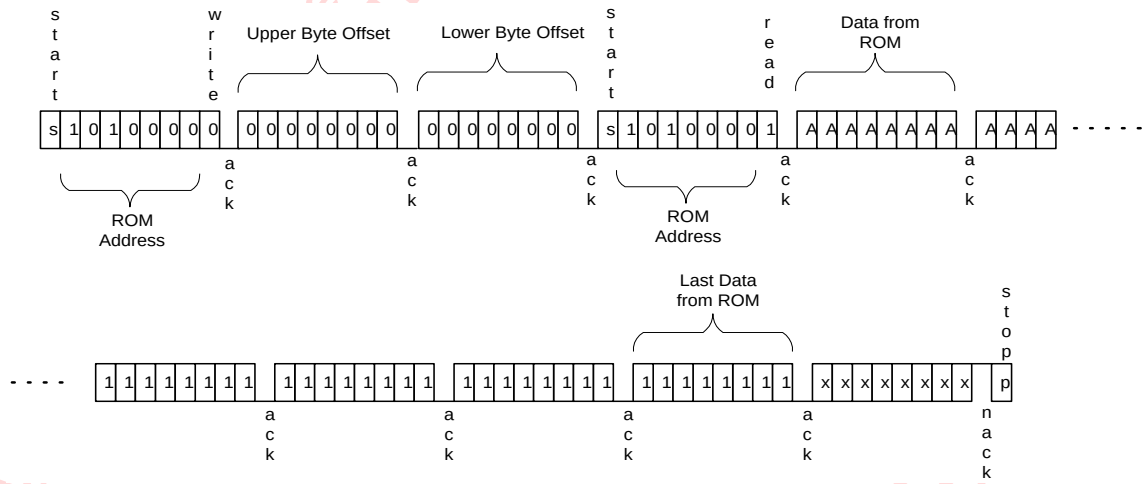
Notes

- Regardless of the CPU endianess setting, the serial ROM data must be set in Little Endian convention.
- While serial ROM is active the INITACT is driven high.
- Since INITACT signal is multiplex on the MPP interface, the code on the serial interface must make sure that the corresponding MPP pin is correctly configured to drive the INITACT signal.
- Since the INITACT signal is not driven before reset, the system must pull it to 1 (active state).

13.3.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the MV64440/1/2 starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, in order to set the ROM byte offset to 0x0. Then, it performs the sequence of reads, until it reaches last data item, as shown in Figure 14.

Figure 14: Serial ROM Read Example



For a detailed description of TWSI implementation, see the Two-Wire Serial Interface section in the *MV64440/1/2 Datasheet User Manual*.

Notes

- Initialization data must be programmed in the serial ROM starting at offset 0x0
- The MV64440/1/2 assumes 7-bit serial ROM address of 'b10100xx. The value of xx is sampled at reset.
- The MV64440/1/2 device supports only serial ROM with a byte offset wider than eight bits. Setting the ROM byte offset to 0 means the MV64440/1/2 performs a dummy write of two bytes. This is different than the GT-64240/60 device that also supports smaller byte offset.
- After receiving the last data identifier (default value is 0xffff.ffff), the MV64440/1/2 receives an additional byte of dummy data. It responds with no-ack and then asserts the stop bit.

13.4 MV64440/1/2 Initialization

Following power up and stable clock, there are some conditions that need to be met:

If using serial ROM initialization, it is desired to prevent access to the MV64440/1/2 device prior to initialization completion. Any PCI attempt to access the MV64440/1/2 during initialization results in a RETRY termination. Also, the DRAM initialization sequence is postponed until the serial initialization completes. This guarantees that the SDRAM Mode registers are updated to the right values prior to DRAM initialization.

The CPU access might also need to be postponed until serial initialization is done. This is achieved by using external hardware to keep the CPU under reset for the entire initialization period. To identify when initialization is done, configure one of the MPP pins, via the initialization code, to act as initialization active output, see Section 11. “Multi Purpose Pins Multiplexing” on page 79.

Section 14. Electrical Specifications

The HSTL, SSTL, and PCI electrical specifications meet the following standards.

- HSTL: EIA/JEDEC standard EIA/JESD8-6 (High Speed Transceiver Logic [HSTL], a 1.5V output buffer supply voltage based interface standard for digital integrated circuits).
- SSTL: EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5 volts, SSTL_2).
- PCI: PCI Local Bus Specification rev. 2.2 and PCI-X Addendum rev. 1.0b.

14.1 Power-Up Sequence Requirements

Note

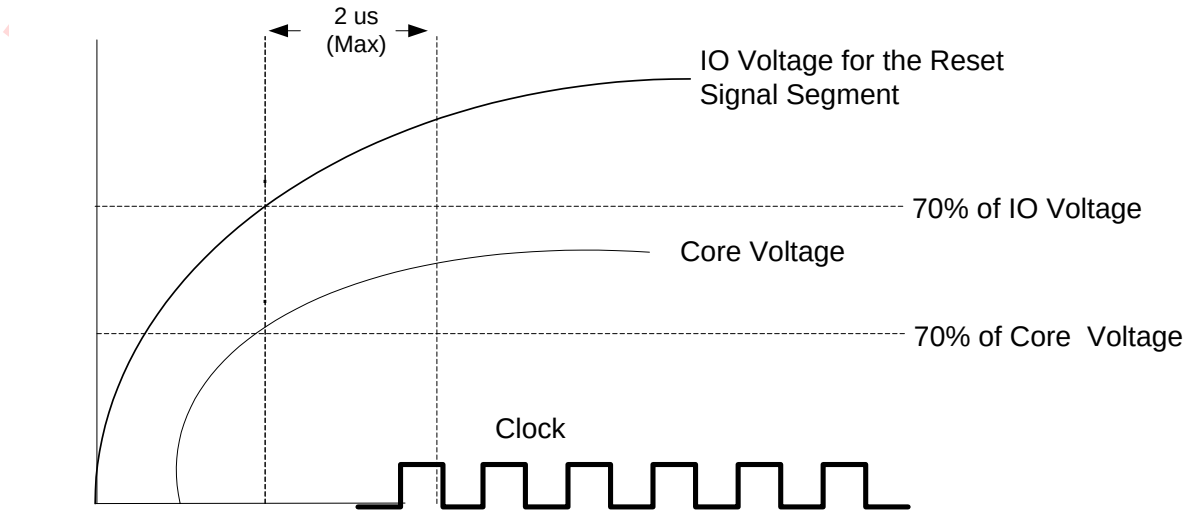
Table 31 provides details for all of the power domains described in the following requirements.

These guidelines must be applied to meet the MV64440/1/2 device power-up requirements:

- All of the following power domain supplies: VDD_V33, V_ETH0, V_ETH1, VDD_CPU, VDD_DRAM, VDD_CLK, PLLs and DLLs supply must be powered up before or up to 2 µs after VDD_CORE.
- No later than 2 µs after the above VDD_CORE reaches 70% of its voltage level, the reset signals SYSRSTn, PCI0_RSTn, and PCI1_RSTn must be asserted.
- No later than 2 µs after the above VDD_CORE reaches 70% of its voltage level, the clock signals SYS_CLK, and TCLK must be running.

Figure 15 shows an example of the power up sequence.

Figure 15: Power Up Sequence Example



Note

It is the designer's responsibility to verify that the power sequencing requirements of other components are also satisfied.

Table 31 summarizes the MV64440/1/2 power, reset, and clock domains and their functionality.

Table 31: MV64440/1/2 Power, Reset, and Clock Domains

Power Domain/Ball Name	Voltage	Functionality
VDD_CORE	1.5V	Core Supply
VDD_V33	3.3V	Voltage I/O Supply
V_ETH0	1.5/2.5/3.3V	I/O Supply for Ethernet Port 0 (Also used for RGMII mode)
V_ETH1	1.5V /2.5/3.3V	I/O Supply for Ethernet Port 1
NOTE: V_ETH1 only applies to the MV64440 and MV64441 devices.		
VDD_CPU	1.5V (HSTL)/2.5/ 3.3V	I/O Supply for CPU Interface
VDD_DRAM	2.5V	I/O Supply for DRAM Interface
VDD_CLK	1.5V (HSTL)/2.5/ 3.3V	I/O Reference Voltage Must be equal to the SYS_CLK input voltage level.
SYSRSTn	3.3V	System Reset
PCI0_RSTn	3.3V	PCI0 Reset
PCI1_RSTn	3.3V	PCI1 Reset
SYS_CLK	1.5V (HSTL)/2.5/ 3.3V	System Clock Domain Input Driven according to the VDD_CLK domain voltage.
TCLK	3.3V	T Clock Domain Clock Input
PCI0_CLK	3.3V	PCI Clock Input
PCI1_CLK	3.3V	PCI1 Clock Input
PLL0_VDDAH	2.5V	PLL supply
PLL1_VDDAH	2.5V	PLL supply
DLL0_VDDAH	1.5V	DLL supply
DLL1_VDDAH	1.5V	DLL supply
HSTL_VREF0	0.75V	CPU HSTL in Mode Vref Supply
HSTL_VREF1	0.75V	CPU HSTL in Mode Vref Supply
RGMII_VREF	0.75V	GbE in HSTL Mode Vref Supply

Table 31: MV64440/1/2 Power, Reset, and Clock Domains (Continued)

Power Domain/Ball Name	Voltage	Functionality
M_SSTLVREF_0	VDD_DRAM/2	Vref supply for DDR Interface
M_SSTLVREF_1	VDD_DRAM/2	Vref supply for DDR Interface

Note

In Hot Insertion applications, Vref must be floated (disconnected), if the PCI signals are active before the Vref is powered. Otherwise, any input to the PCI-X pads may result in a damage to the chip. The designer must connect the Vref (PCI Vi/o) to early power.

14.2 Power-Down Sequence Requirements

There are no special requirements for the core supply to go down first or for reset assertion when powering down.

14.3 Absolute and Recommended Operating Conditions

Caution

Exposure to conditions at or beyond the maximum rating may damage the device.

Table 32: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
VDD_CORE	Core Supply Voltage	-0.5	2.1	V
VDD_V33	I/O Supply for PCI and MPPH Interface	-0.5	4.6	V
VDD_V33_DEVICE	I/O Supply for Device Interface	-0.5	4.6	V
VDD_V33_MPPL	I/O Supply for MPPL Interface	-0.5	4.6	V
VDD_ETH	I/O Supply for Ethernet Port0/1	-0.5	4.6	V
VDD_CPU	I/O Supply for CPU Interface	-0.5	4.6	V
VDD_DRAM	I/O Supply for DRAM Interface	-0.5	3.5	V
VDD_CLK	I/O Reference Voltage	-0.5	4.6	V
PLLx_VDDAH	PLL Supply	-0.5	3.5	V
DLLx_VDDAH	DLL Supply	-0.5	2.1	V
T_{stg}	Storage Temperature	-40	125	C

Caution

Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Table 33: Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_CORE	Core Supply Voltage	1.43	1.5	1.58	V
VDD_CPU	CPU interface I/O Supply Voltage @ 2.5V	2.38	2.5	2.62	V
	CPU interface I/O Supply Voltage @ 3.3V	3.15	3.3	3.45	V
VDD_CPU @ HSTL	CPU interface I/O Supply Voltage @ HSTL	1.4	1.5	1.6	V
VDD_DRAM	DRAM interface I/O Supply Voltage (SSTL)	2.30	2.5	2.70	V
PLLx_VDDAH	PLL Supply Voltage	2.38	2.5	2.62	V
DLL_VDDAH	DLL Supply Voltage	1.43	1.5	1.58	V
VDD_ETHx	Ethernet Portx Gigabit Ethernet Controller Interface I/O Supply Voltage @ HSTL/RGMII	1.4	1.5	1.6	V
	Ethernet Portx Gigabit Ethernet Controller Interface I/O Supply Voltage @ 2.5V/RGMII	2.38	2.5	2.62	V
	Ethernet Portx Gigabit Ethernet Controller Interface I/O Supply Voltage @ 3.3V/GMII/MII/ TBI	3.15	3.3	3.45	V
VDD_V33	I/O Supply for PCI and MPPH Interface	3.15	3.3	3.45	V
VDD_V33_DEVICE	I/O Supply for Device Interface	3.15	3.3	3.45	
VDD_V33_MPPL	I/O Supply for MPPL Interface	3.15	3.3	3.45	
V_i CPU	I/O Supply for Ethernet Port0/1	0		1.9	V
	CPU interface Input Voltage @ 2.5V	0		2.62	V
	CPU interface Input Voltage @ 3.3V	0		3.45	V
V_i ETH	Gigabit Ethernet Input Voltage @ 2.5V/RMII	0		2.62	V
	Gigabit Ethernet Input Voltage @ 3.3V/MII, GMII, TBI	0		3.45	V
V_i 3.3V	Input Voltage (all other interfaces)	0		3.45	V
T_j	Junction Temperature	0		125	C

Table 34: Pin Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Unit
C	Pin Capacitance			6	pF

14.4 DC Electrical Characteristics Over Operating Range

Note

For the resistor values that match the test conditions values, see *TB-119: MV644xx Design Considerations.*

Table 35: DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{ih} CPU 2.5V	CPU interface Input HIGH level @ 2.5V		1.7		V
V_{il} CPU 2.5V	CPU interface Input LOW level @ 2.5V			0.7	V
V_{OH} CPU 2.5V	CPU interface output HIGH level @ 2.5V	I_{OH} = 10 mA	2		V
V_{OL} CPU 2.5V	CPU interface output LOW level @ 2.5V	I_{OL} = 16 mA		0.6	V
V_{ih} CPU 3.3V	CPU interface Input HIGH level @ 3.3V		2		V
V_{il} CPU 3.3V	CPU interface Input LOW level @ 3.3V			0.8	V
V_{OH} CPU 3.3V	CPU interface output HIGH level @ 3.3V	I_{OH} = 20 mA	2.4		V
V_{OL} CPU 3.3V	CPU interface output LOW level @ 3.3V	I_{OL} = 10 mA		0.4	V
V_{ih} CPU HSTL	CPU interface Input HIGH level @ HSTL		Vref + 0.1		V
V_{il} CPU HSTL	CPU interface Input LOW level @ HSTL			Vref - 0.1	V
V_{OH} CPU HSTL	CPU interface output HIGH level @ HSTL		Vdd - 0.4		V
V_{OL} CPU HSTL	CPU interface output LOW level @ HSTL			0.4	V
V_{ih} ETH 3.3V	Gigabit Ethernet interface Input HIGH level @ 3.3V		2		V
V_{il} ETH 3.3V	Gigabit Ethernet Input LOW level @ 3.3V			0.8	V
V_{OH} ETH 3.3V	Gigabit Ethernet output HIGH level @ 3.3V	I_{OH} = 20 mA	2.4		V
V_{OL} ETH 3.3V	Gigabit Ethernet output LOW level @ 3.3V	I_{OL} = 10 mA		0.4	V
V_{ih} ETH 2.5V	Gigabit Ethernet interface Input HIGH level @ 2.5V		1.7		V
V_{il} ETH 2.5V	Gigabit Ethernet Input LOW level @ 2.5V			0.7	V
V_{OH} ETH 2.5V	Gigabit Ethernet output HIGH level @ 2.5V	I_{OH} = 10 mA	2.0		V

Table 35: DC Electrical Characteristics Over Operating Range (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL} ETH 2.5V	Gigabit Ethernet output LOW level @ 2.5V	I_{OL} = 10 mA		0.4	V
V_{ih} ETH HSTL	Gigabit Ethernet interface Input HIGH level @ HSTL		Vref + 0.1		V
V_{il} ETH HSTL	Gigabit Ethernet interface Input LOW level @ HSTL			Vref - 0.1	V
V_{OH} ETH HSTL	Gigabit Ethernet interface output HIGH level @ HSTL	I_{OH} = 11 mA	Vdd-0.4		V
V_{OL} ETH HSTL	Gigabit Ethernet interface output LOW level @ HSTL	I_{OL} = 14 mA		0.4	V
$V_{ih(DC)}$ DRAM	DRAM interface Input HIGH level DC (SSTL)		Vref + 0.15	VDD_ DRAM +0.3	V
$V_{il(DC)}$ DRAM	DRAM interface Input LOW level DC (SSTL)		-0.3	Vref - 0.15	V
$V_{ih(AC)}$ DRAM	DRAM interface Input HIGH level AC (SSTL)		Vref + 0.31		V
$V_{il(AC)}$ DRAM	DRAM interface Input LOW level AC (SSTL)			Vref - 0.31	V
V_{OH} DRAM	DRAM interface output HIGH level (SSTL)	I_{OH} = 8.1 mA	Vdd - 0.4		V
V_{OL} DRAM	DRAM interface output LOW level (SSTL)	I_{OL} = 14 mA		0.4	V
V_{ih} PCI/MPP	PCI interface Input HIGH level		0.5* Vdd		V
V_{il} PCI/MPP	PCI interface Input LOW level			0.35* Vdd	V
V_{OH} PCI/MPP	PCI interface output HIGH level	I_{OH} = 6 mA	0.9* Vdd		V
V_{OL} PCI/MPP	PCI interface output LOW level	I_{OL} = 12 mA		0.1* Vdd	V
V_{ih}	Input HIGH level (all other interfaces)		2		V
V_{il}	Input LOW level (all other interfaces)			0.8	V
V_{oh}	Output HIGH Voltage (all other interfaces)	I_{OH} = 6 mA	2.4		V
V_{ol}	Output LOW Voltage (all other interfaces)	I_{OL} = 6 mA		0.4	V
I_{il}	Input Current			+/-10	uA

Table 35: DC Electrical Characteristics Over Operating Range (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{oz}	High Impedance Output Current for all pins except: CPU_SYSAD[63:0], CPU_SYSADC[7:0			+/-10	uA
	High Impedance Output Current for CPU_SYSAD[63:0], CPU_SYSADC[7:0]			-50 to +10	uA
Icc	Operating current			TBD	mA

Note

The MPP pins are using the same I/O pads (same DC characteristics) as the PCI interface

.

Table 36: Power Consumption

Description	Typical	Maximum	Unit
1. Maximum configuration: SYS_CLK @ 200 MHz TCLK @ 133 MHz CPU interface - 2.5V LVCMOS Two PCI-X interfaces @ 133 MHz MV64440: Three RGMII ports, MV64441: Two RGMII ports, MV64442: One RGMII ports	4		W
Same as maximum configuration, except that SYS_CLK is running @ 166 MHz.	3.6		W

The MV64440/1/2 power consumption depends on the frequency, the voltage, and the number of interfaces used.

Section 15. Thermal Data

Table 37 shows the package thermal data for the MV64440/1/2.

Note

It is recommended to read *AN-63: Thermal Management for Selected Marvell Products* and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 37: Thermal Data for the MV64440/1/2 in BAY 844

Parameter	Definition	Airflow Value		
		0 m/s	1 m/s	2 m/s
θ_{JA}	Thermal resistance: junction to ambient	12.2 C/W	10.4 C/W	9.7 C/W
Ψ_{JT}	Thermal characterization parameter: junction to top center	0.21 C/W	0.28 C/W	0.33 C/W
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	3.5 C/W		
Ψ_{JB}	Thermal characterization parameter: junction to bottom center	5.51 C/W	5.46 C/W	5.37 C/W
θ_{JB}	Thermal resistance: junction to board	8 C/W		

Section 16. AC Timing

Notes

- The AC timing parameters in this specification are preliminary and subject to change.
- The ouput delays are measured against a specific load as specified in the following tables. To determine the real board timing budget, run board timing simulation using the MV64440/1/2 IBIS model.

16.1 Clock Timing

Table 38: Clock AC Timing

Signals	Description	Min.	Max.	Units	Load
SYS_CLK	Frequency	100	200	MHz	
SYS_CLK	Cycle Time	5	10	ns	
SYS_CLK	Duty Cycle	40	60	%	
SYS_CLK	Slew Rate	1		V/ns	
SYS_CLK	Pk-Pk jitter		200	ps	
SYS_CLK	PLL Lock Time		1	ms	
SYS_CLK Spread Spectrum Requirements					
SYS_CLK	f_{mod} (Frequency Modulation)		33	Khz	
SYS_CLK	f_{spread}	-1	0	%	
TCLK	Frequency	83	133	MHz	
TCLK	Cycle Time	7.5	12	ns	
TCLK	Duty Cycle	40	60	%	
TCLK	Slew Rate	1		V/ns	
TCLK	Pk-Pk jitter		200	ps	
TCLK	PLL Lock Time		1	ms	

Table 38: Clock AC Timing (Continued)

Signals	Description	Min.	Max.	Units	Load
TCLK Spread Spectrum Requirements					
TCLK	f_{mod} (Frequency Modulation)		33	Khz	
TCLK	f_{spread}	-1	0	%	

16.2 MIPS CPU Interface

Notes

- All CPU interface Output Delays, Setup, and Hold times are referred to SYS_CLK rising edge, and measured on the MV64440/1/2 pins.
- The CPU interface timing was measured using a 30 Ohm pad calibration resistor.

Table 39: MIPS CPU Interface AC Timing

Signals	Description	Min.	Max.	Units	Load
CPU Interface - 3.3V LVTTL					
CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCTCEn, CPU_TCMATCH	Setup	1.4		ns	
CPU_SYSADC[7:0], CPU_SYSAD[63:0],	Setup	1.6		ns	
CPU_SYSADC[7:0], CPU_SYSAD[63:0], CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCTCEn, CPU_TCMATCH	Hold	0		ns	
CPU_SYSCMD[8:0], CPU_VALID_INn, CPU_SYSRDY_OUTn, CPU_PACKn, CPU_RSSWAPn, CPU_TCDOEn, CPU_TCWORD[1:0], CPU_SYSAD[63:0], CPU_SYSADC[7:0]	Output Delay	1.0	2.7	ns	5 pF
CPU Interface - 2.5V LVCMOS					
CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCTCEn, CPU_TCMATCH	Setup	1.4		ns	
CPU_SYSADC[7:0], CPU_SYSAD[63:0]	Setup	1.7		ns	

Table 39: MIPS CPU Interface AC Timing (Continued)

Signals	Description	Min.	Max.	Units	Load
CPU_SYSADC[7:0], CPU_SYSAD[63:0], CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCTCEn, CPU_TCMATCH	Hold	0		ns	
CPU_SYSCMD[8:0], CPU_VALID_INn, CPU_SYSRDY_OUTn, CPU_PACKn, CPU_RSSWAPn, CPU_TCDOEn, CPU_TCWORD[1:0], CPU_SYSAD[63:0], CPU_SYSADC[7:0]	Output Delay	1.0	2.8	ns	5 pF
CPU Interface - 1.5V HSTL					
CPU_TCTCEn, CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCMATCH, CPU_SYSADC[7:0], CPU_SYSAD[63:0]	Setup	1.95		ns	
CPU_SYSADC[7:0], CPU_SYSAD[63:0], CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, CPU_TCTCEn, CPU_TCMATCH	Hold	0		ns	
CPU_SYSAD[63:0], CPU_SYSADC[7:0], CPU_SYSRDY_OUTn, CPU_TCWORD[1:0], CPU_VALID_INn, CPU_SYSCMD[8:0], CPU_PACKn, CPU_RSSWAPn, CPU_TCDOEn	Output Delay	1.0	3.6	ns	5 pF

16.3 DDR SDRAM Interface

Notes

- For layout recommendations, see *TB-119: MV644xx Design Considerations*.
- The DRAM interface outputs are measured from M_CLK_OUT rising edge (M_CLK_OUT/ M_CLK_OUTn crossing point) to V_{TT}.
- Any percentage parameter in the SDRAM timing represents the percentage of the cycle time (cycle time of the SYS_CLK domain).
- DRAM timing is given for 200, 166, and 133 MHz frequencies. Table 41 and Table 42 shows the relaxed timing considerations when using a frequency below 200 MHz.

Table 40: DDR SDRAM AC Timing (200 MHz)

Signals	Description	Min.	Max.	Units	Load
M_CLK_OUT/M_CLK_OUTn	Frequency	100	200	MHz	
M_CLK_OUT/M_CLK_OUTn	Cycle Time	5	10	ns	
M_CLK_OUT/M_CLK_OUTn	Duty Cycle	46	54	%	
M_CLK_OUT/M_CLK_OUTn	Slew Rate	1		V/ns	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DSS} (M_DQS falling edge to CK rising - setup time)	42		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DSH} (M_DQS falling edge from CK rising - hold time)	48		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DQSL} (M_DQS output low pulse width)	46		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DQSH} (M_DQS output high pulse width)	49		%	
M_DA[13:0], M_BA[1:0], M_RASn, M_CASn, M_WEn, M_CSn[3:0], M_CKE0, M_CKE1	Address output delay	0.4	1.7	ns	
M_DQ[63:0], M_CB[7:0], DM[8:0]	t_{DS} (Data output setup relative to M_DQS.)	0.6		ns	
M_DQ[63:0], M_CB[7:0], DM[8:0]	t_{DH} (Data output hold relative to M_DQS.)	0.6		ns	

Table 40: DDR SDRAM AC Timing (200 MHz) (Continued)

Signals	Description	Min.	Max.	Units	Load
M_DQ[63:0], M_CB[7:0], DM[8:0]	t_{DIPW} (Data output pulse width.)	2		ns	
M_DQ[63:0], M_CB[7:0]	t_{DSi} (Data input setup relative to M_DQS input.)	-0.6		ns	
M_DQ[63:0], M_CB[7:0]	t_{DHi} (Data input hold relative to M_DQS input.)	1.5		ns	

Table 41: DDR SDRAM AC Timing (166 Mhz)

Signals	Description	Min.	Max.	Units	Load
M_CLK_OUT/M_CLK_OUTn	Frequency	100	166	MHz	
M_CLK_OUT/M_CLK_OUTn	Cycle Time	6	10	ns	
M_CLK_OUT/M_CLK_OUTn	Duty Cycle	46	54	%	
M_CLK_OUT/M_CLK_OUTn	Slew Rate	1		V/ns	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DSS} (M_DQS falling edge to CK rising - setup time)	43		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input)	t_{DSH} (M_DQS falling edge from CK rising - hold time)	49		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input)	t_{DQSL} (M_DQS output low pulse width)	46		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input)	t_{DQSH} (M_DQS output high pulse width)	49		%	
M_DA[13:0], M_BA[1:0], M_RASn, M_CASn, M_WEn, M_CSn[3:0], M_CKE0, M_CKE1	Address output delay	0.4	1.7	ns	

Table 41: DDR SDRAM AC Timing (166 Mhz) (Continued)

Signals	Description	Min.	Max.	Units	Load
M_DQ[63:0], M_CB[7:0], DM[8:0]	t_{DS} (Data output setup relative to M_DQS.)	0.65		ns	
M_DQ[63:0], M_CB[7:0], DM[8:0]	t_{DH} (Data output hold relative to M_DQS.)	0.65		ns	
M_DQ[63:0], M_CB[7:0], DM[8:0]	t_{DIPW} (Data output pulse width.)	2		ns	
M_DQ[63:0], M_CB[7:0]	t_{DSi} (Data input setup relative to M_DQS input.)	-0.65		ns	
M_DQ[63:0], M_CB[7:0]	t_{DHi} (Data input hold relative to M_DQS input.)	1.75		ns	

Table 42: DDR SDRAM AC Timing (133 Mhz)

Signals	Description	Min.	Max.	Units	Load
M_CLK_OUT/M_CLK_OUTn	Frequency	100	133	MHz	
M_CLK_OUT/M_CLK_OUTn	Cycle Time	7.5	10	ns	
M_CLK_OUT/M_CLK_OUTn	Duty Cycle	46	54	%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **Note:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DSS} (M_DQS falling edge to CK rising - setup time)	44		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DSH} (M_DQS falling edge from CK rising - hold time)	49		%	
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **NOTE:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DQSL} (M_DQS output low pulse width)	47		%	

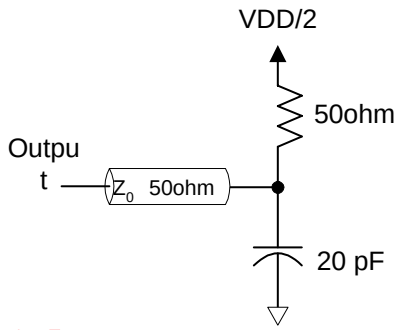
Table 42: DDR SDRAM AC Timing (133 Mhz) (Continued)

Signals	Description	Min.	Max.	Units	Load
M_DQS[8:0], M_DM[8:0]/M_DQS[17:9] **Note:** Refers to MV64440/1/2 output on write transactions (Memory input).	t_{DQSH} (M_DQS output high pulse width)	49		%	
M_DA[13:0], M_BA[1:0], M_RASn, M_CASn, M_WEn, M_CSn[3:0], M_CKE0, M_CKE1	Address output delay	0.4	1.7	ns	
M_DQ[63:0], M_CB[7:0], M_DM[8:0]	t_{DS} (Data output setup relative to M_DQS.)	0.7		ns	
M_DQ[63:0], M_CB[7:0], M_DM[8:0]	t_{DH} (Data output hold relative to M_DQS.)	0.7		ns	
M_DQ[63:0], M_CB[7:0], M_DM[8:0]	t_{DIPW} (Data output pulse width.)	2		ns	
M_DQ[63:0], M_CB[7:0]	t_{DSi} (Data input setup relative to DQS input.)	-0.7		ns	
M_DQ[63:0], M_CB[7:0]	t_{DHi} (Data input hold relative to M_DQS input.)	2.1		ns	

Notes

- M_CLK_OUT can drive up to 2 loads. If interfacing with additional devices (using un-buffered DIMMs or multiple DRAM devices on board), the M_CLK_OUT/M_CLK_OUTn pair must be distributed via a zero delay (PLL) clock buffer.
- The DRAM interface outputs are measured from M_CLK_OUT rising edge (M_CLK_OUT/ M_CLK_OUTn crossing point) to V_{TT}.

Figure 16: DRAM SSTL I/O Pads Output Delay Test Load



Note

The DRAM load applies to both M_CLK/M_CLKn and to DRAM address and control outputs

Figure 17: DDR Output Delay Timing Diagram

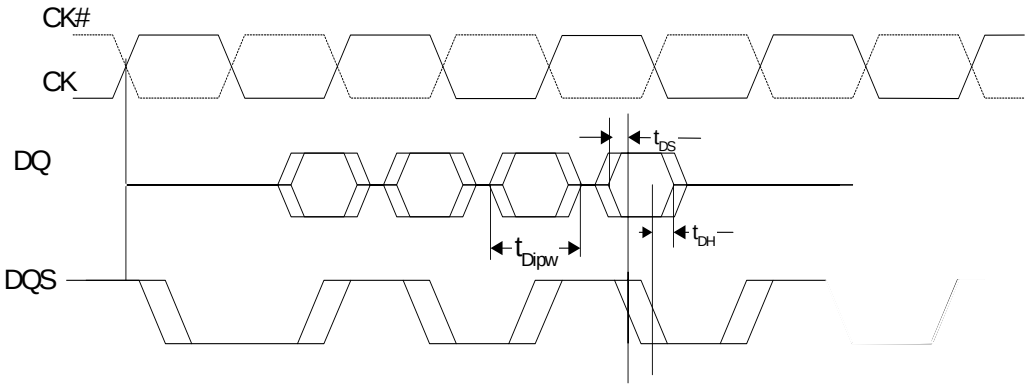
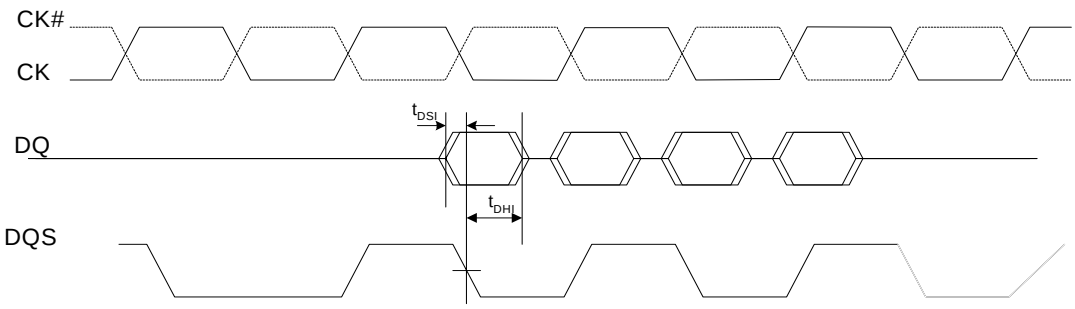


Figure 18: DDR Setup Timing Diagram



16.4 Device Interface

Note

All Device interface setup, hold, and output delay times are referred to the TCLK rising edge.

Table 43: Device Interface AC Timing

Signals	Description	Min.	Max.	Units	Load
DEV_AD[31:0], DEV_DP[3:0], DEV_READYn	Setup	1.5		ns	
DEV_AD[31:0], DEV_DP[3:0], DEV_READYn	Hold	0		ns	
DEV_CSTIMINGn, DEV_WEn[3:0], DEV_ALE, DEV_BADR[2:0]	Control output delay	1.2	3.7	ns	20 pF
DEV_AD[31:0], DEV_DP[3:0]	Data output delay	0.85	3.15	ns	20 pF

16.5 PCI Interface in PCI-X Mode

Notes

- In this mode, the PCI interface DLL is enabled.
- All PCI interface setup, hold, and output delay times are referred to the PCLK's rising edge.
- The PCI interface was measured using a 22 Ohm pad calibration resistor.
- The following signals do not apply in the MV64441 device: PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_AD[63:32], PCI1_CBEn[7:4].
- The following signals do not apply in the MV64442 device: PCI1_REQ64n, PCI1_ACK64n, PCI1_PAR64, PCI1_AD[63:32], PCI1_CBEn[7:4].

Table 44: PCI Interface in PCI-X Mode AC Timing

Signals	Description	Min.	Max.	Units	Load
PCIx_CLK	Frequency	66	133	MHz	
PCIx_CLK	Cycle Time	7.5	15	ns	
PCIx_CLK	Duty Cycle	40	60	%	
PCIx_CLK	Slew Rate	1.5	4	V/ns	
FMod	Frequency Modulation		33	Khz	
FSpread	Frequency Spread	-1	0	%	
PCIx_RSTn	Active Time	1.0		ms	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_GNTn **NOTE:** PCIx_GNTn is only relevant when using an external PCI bus arbiter.	Setup	1.2		ns	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_GNTn **NOTE:** PCIx_GNTn is only relevant when using an external PCI bus arbiter.	Hold	0.8		ns	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_SERRn, PCIx_REQn **NOTE:** PCIx_REQn is only relevant when using an external PCI bus arbiter.	Output Delay	1.0	3.8	ns	

16.6 PCI Interface in Conventional PCI Mode at 66 MHz

Notes

- In this mode, the PCI interface DLL is enabled.
- All PCI interface setup, hold, and output delay times are referred to the PCLK's rising edge.
- The PCI interface was measured using a 22 Ohm pad calibration resistor.
- The following signals do not apply in the MV64441 device: PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_AD[63:32], PCI1_CBEn[7:4].
- The following signals do not apply in the MV64442 device: PCI1_REQ64n, PCI1_ACK64n, PCI1_PAR64, PCI1_AD[63:32], PCI1_CBEn[7:4].

Table 45: PCI Interface in Conventional PCI Mode at 66 MHz AC Timing

Signals	Description	Min.	Max.	Units	Note
PCIx_CLK	Frequency	33	66	MHz	
PCIx_CLK	Cycle Time	15	30	ns	
PCIx_CLK	Duty Cycle	40	60	%	
PCIx_CLK	Slew Rate	1.5	4	V/ns	
PCIx_RSTn	Active Time	1.0		ms	
FMod	Frequency Modulation		33	Khz	
FSpread	Frequency Spread	-1	0	%	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR	Setup (Bused Signals)	3.0		ns	
PCIx_GNTn **NOTE:** PCIx_GNTn is only relevant when using an external PCI bus arbiter.	Setup (Point-to-Point Signals)	4.0		ns	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_GNTn	Hold	1.0		ns	

Table 45: PCI Interface in Conventional PCI Mode at 66 MHz AC Timing (Continued)

Signals	Description	Min.	Max.	Units	Note
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_SERRn, PCIx_REQn **NOTE:** PCIx_REQn is only relevant when using an external PCI bus arbiter.	Output Delay	2.0	6.0	ns	

16.7 PCI Interface in Conventional PCI Mode at 33 MHz

Notes

- The PCI interface was measured using a 22 Ohm pad calibration resistor.
- The following signals do not apply in the MV64441 device: PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_AD[63:32], PCI1_CBEn[7:4].
- The following signals do not apply in the MV64442 device: PCI1_REQ64n, PCI1_ACK64n, PCI1_PAR64, PCI1_AD[63:32], PCI1_CBEn[7:4].

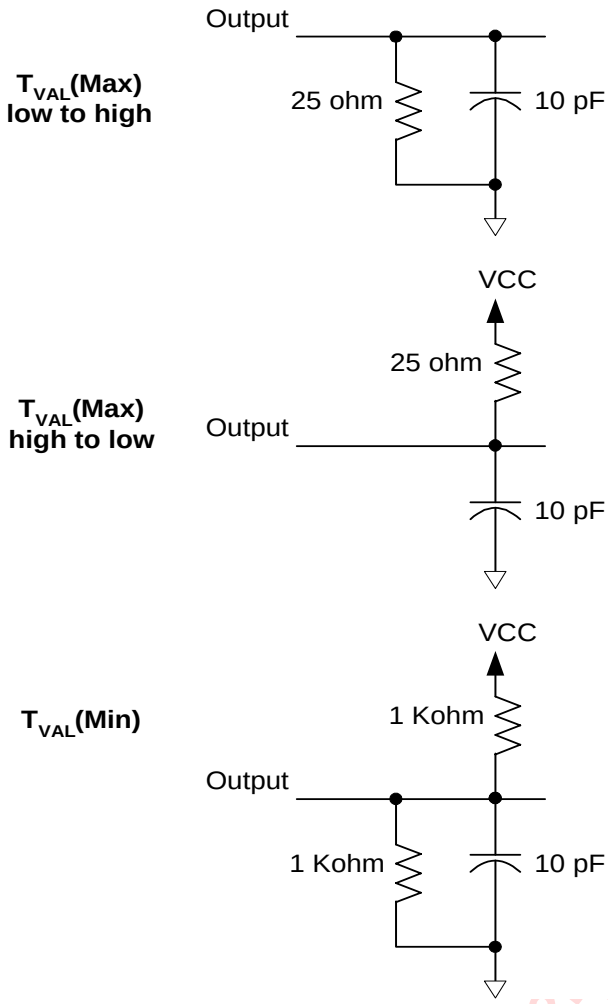
Table 46: PCI Interface in Conventional PCI Mode at 33 MHz AC Timing

Signals	Description	Min.	Max.	Units	Load
PCIx_CLK	Frequency	0	33	MHz	
PCIx_CLK	Cycle Time	30	DC	ns	
PCIx_CLK	Duty Cycle	40	60	%	
PCIx_CLK	Slew Rate	1	4	V/ns	
PCIx_RSTn	Active Time	1		ms	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR	Setup (Bused Signals)	3.5		ns	
PCIx_GNTn **NOTE:** PCIx_GNTn is only relevant when using an external PCI bus arbiter.	Setup (Point-to-Point Signals)	5		ns	

Table 46: PCI Interface in Conventional PCI Mode at 33 MHz AC Timing (Continued)

Signals	Description	Min.	Max.	Units	Load
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_IDSEL, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_GNTn	Hold	0.75		ns	
PCIx_FRAMEn, PCIx_IRDYn, PCIx_TRDYn, PCIx_STOPn, PCIx_DEVSELn, PCIx_REQ64n, PCIx_ACK64n, PCIx_PAR64, PCIx_PERRn, PCIx_AD[63:0], PCI1_CBEn[7:0], PCIx_PAR, PCIx_GNTn, PCIx_SERRn	Output Delay (Bused Signals)	2	6.5	ns	
PCIx_REQn **NOTE:** PCIx_REQn is only relevant when using an external PCI bus arbiter.	Output Delay (Point-to-Point Signals)	2	12	ns	

Figure 19: PCI I/O Pads Output Delay Test Load



16.8 MPP Interface

Notes

- All MPP pins setup, hold, and output delay times are referred to the SYS_CLK rising edge, unless stated otherwise.
- PCIx_PMEn, WD_En, WD_NMIn are asynchronous outputs.

Table 47: MPP Interface AC Timing

Signals	Description	Min.	Max.	Units	Load
MPP[31:0]	Setup	1.6		ns	
MPP[31:0]	Hold	0.1		ns	
MPP[31:0]	Output Delay	1.5	4.35	ns	20 pF
PCIx_REQn[5:0]	Setup	5.0		ns[1]	
		4.0		ns[2]	
		1.2		ns[3]	
PCIx_REQn[5:0]	Hold	0.75		ns[1]	
		1.0		ns[2]	
		0.8		ns[3]	
PCIx_GNTn[5:0]	Output Delay	3.1	6.5	ns[1]	
		2.2	4.7	ns[2]	
		1.8	3.85	ns[3]	
DMA_REQ[3:0], DMA_EOTn[3:0], TC_ENn[3:0]	Setup	1.65		ns	
DMA_REQ[3:0]n, DMA_EOTn[3:0], TC_ENn[3:0]	Hold	0.1		ns	
DMA_ACKn[3:0], TC_NTn[3:0]n, DEV_BURSTn, INITACT	Output Delay	1.5	4.35	ns	20 pF
Sx_SCLK, Sx_TSCLK	Frequency		50	MHz	
Sx_SCLK, Sx_TSCLK	Cycle Time	20		ns	
Sx_TXD	Output Delay	5.2	12.3	ns	20 pF
Sx_RTS **NOTE:** Numbers refer to TCLK rising edge.	Output Delay	5.6	12	ns	20 pF
Sx_RXD	Setup	4		ns	
Sx_RXD	Hold	1		ns	
Sx_CTS	Setup	3.4		ns	

Table 47: MPP Interface AC Timing (Continued)

Signals	Description	Min.	Max.	Units	Load
Sx_CTS	Hold	0.8		ns	
Sx_CD	Setup	2		ns	
Sx_CD **NOTE:** Sx_RXD, Sx_CTS and Sx_CD are relative to TSCLK rising edge.	Hold	1		ns	

1 33 MHz conventional PCI. PCI interface DLL is disabled. Numbers are referred to PCLK rising edge. Output delays are measured with load as specified in the PCI spec.
2 66 MHz conventional PCI. PCI interface DLL is enabled. Numbers are referred to PCLK rising edge. Output delays are measured with load as specified in the PCI spec.
3 133MHz PCI-X. PCI interface DLL is enabled. Numbers are referred to PCLK rising edge. Output delays are measured with load as specified in the PCI spec.

16.9 Gigabit Ethernet Interface AC Timing

Table 48: Gigabit Ethernet Interface AC Timing

Signals	Description	Min.	Max.	Units	Load
Ethernet RGMII (RGMII and RGMII-ID) Interface **NOTE:** Inputs setup/hold times refer to the Px_RXCLK rising and falling edges. Output delays, are referred to the Px_TXCLK_OUT rising and falling edges. For different RGMII modes, see Figure 20 and Figure 21.					
CLK125	Frequency	125 (-50 PPM)	125 (+50 PPM)	MHz	
CLK125	Duty Cycle	45	55	%	
CLK125	Period	7.2	8.8	ns	
Px_RXCLK (1000/100/10 Mbps)	Frequency	125/25/2.5 (-50 PPM)	125/25/2.5 (+50 PPM)	MHz	
Px_RXCLK	Duty Cycle	40	60	%	
Px_RXCLK	Period	7.2	8.8	ns	
Px_TXCLK_OUT (1000/100/10 Mbps)	Frequency	125/25/2.5 (-50 PPM)	125/25/2.5 (+50 PPM)	MHz	

Table 48: Gigabit Ethernet Interface AC Timing (Continued)

Px_TXCLK_OUT	Duty Cycle	45	55	%	
Px_TXCLK_OUT	Period	7.2	8.8	ns	
CLK125, Px_RXCLK, Px_TXCLK_OUT	Rise / Fall Time (20-80%)		0.75	ns	
Px_RXD[3:0], Px_RXDV	Input Setup Original RGMII	1.0	2.6	ns	
	Input Setup RGMII-ID	-0.9		ns	
Px_RXD[3:0], Px_RXDV	Input Hold Original RGMII	0.8		ns	
	Input Hold RGMII-ID	2.7		ns	
Px_TXD[3:0], Px_TXEN	Output Skew Original RGMII	- 0.5	+ 0.5	ns	10 pF
	Output Setup RGMII-ID	1.2		ns	10 pF
	Output Hold RGMII-ID	1.2		ns	10 pF
Ethernet PCS Interface (10 bit interface, TBI) **NOTE:** Inputs setup/hold times refer to the Px_RXCLK[1:0] rising edges. Output delays, are referred to the Px_TXCLK_OUT rising edge.					
CLK125	Frequency		125	MHz	
CLK125	Duty Cycle	45	55	%	
Px_RXCLK[1:0]	Frequency		62.5	MHz	
Px_TXCLK_OUT	Period	7.5	8.5	ns	
Px_RX[9:0]	Input Setup	2		ns	
Px_RX[9:0]	Input Hold	1		ns	
Px_TX[9:0]	Output Delay	1.3	5.0	ns	

Table 48: Gigabit Ethernet Interface AC Timing (Continued)

Ethernet GMII Interface **NOTE:** Inputs setup/hold times refer to the Px_RXCLK rising edge. Output delays, are referred to the Px_TXCLK_OUT rising edge.					
CLK125	Frequency		125	MHz	
CLK125	Duty Cycle	45	55	%	
Px_RXCLK	Period	7.5		ns	
Px_TXCLK_OUT	Period	7.5	8.5	ns	
Px_RXD[7:0], Px_RXDV, Px_RXERR	Input Setup	2		ns	
Px_RXD[7:0], Px_RXDV, Px_RXERR	Input Hold	0.15		ns	
Px_TXD[7:0], Px_TXEN, Px_TXERR	Output Delay	0.5	5.0	ns	10 pf
Ethernet MII Interface **NOTE:** Inputs setup/hold times refer to the Px_RXCLK rising edge. Output delays, are referred to the Px_TXCLK rising edge.					
Px_RXCLK	Frequency		25	MHz	
Px_TXCLK	Frequency		25	MHz	
Px_RXD[3:0], Px_RXDV, Px_RXERR	Input Setup	2		ns	
Px_RXD[3:0], Px_RXDV, Px_RXERR	Input Hold	1		ns	
Px_TXD[3:0], Px_TXEN, Px_TXERR	Output Delay	2	11	ns	10 pf
Marvell SyncFIFO Interface **NOTE:** Inputs setup/hold times refer to the Fx_RXCLK rising edge. Output delays, are referred to the Fx_TXCLK_OUT rising edge.					
FIFOCLK **NOTE:** FIFOCLK and Fx_RXCLK frequency should be less or equal to TCLK Frequency	Frequency		133	MHz	
FIFOCLK	Duty Cycle	45	55	%	
Fx_RXCLK **NOTE:** FIFOCLK and Fx_RXCLK frequency should be less or equal to TCLK Frequency	Frequency		133	MHz	
Fx_TXCLK_OUT	Frequency		133	MHz	

Table 48: Gigabit Ethernet Interface AC Timing (Continued)

Fx_RXD[15:0], Fx_RXEN, Fx_RXVALID, Fx_RXLBE	Input Setup	2		ns	
Fx_RXD[15:0], Fx_RXEN, Fx_RXVALID, Fx_RXLBE	Input Hold	0.0		ns	
Fx_TXD[15:0], Fx_TXEN, Fx_TXVALID, Fx_TXLBE	Output Delay	0.5	5.0	ns	10 pF

Figure 20: RGMII Input Timing Diagram

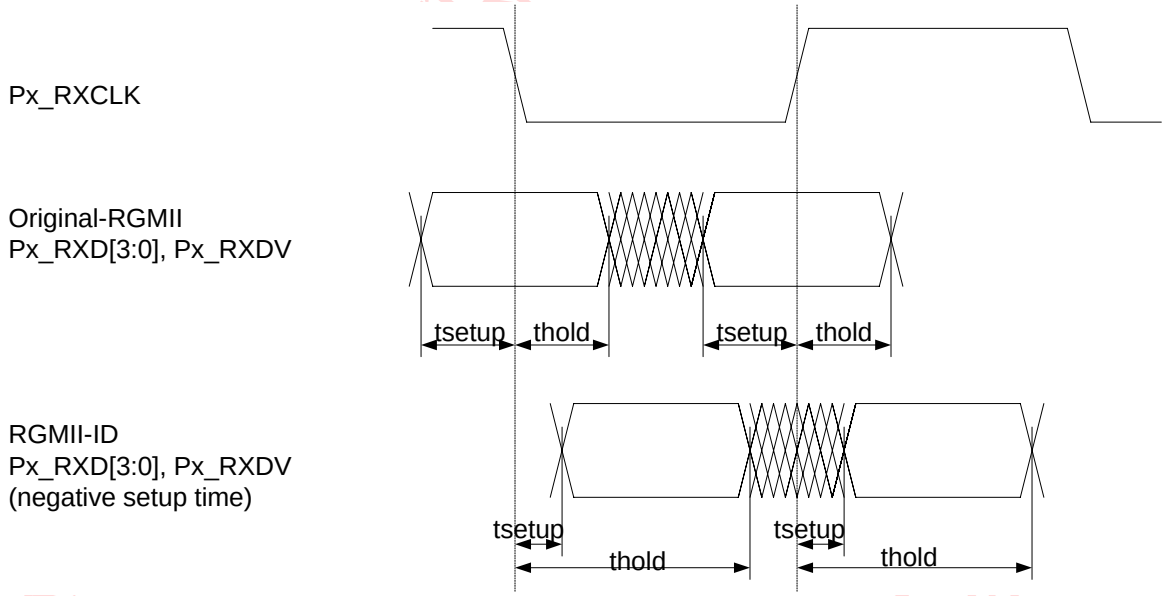
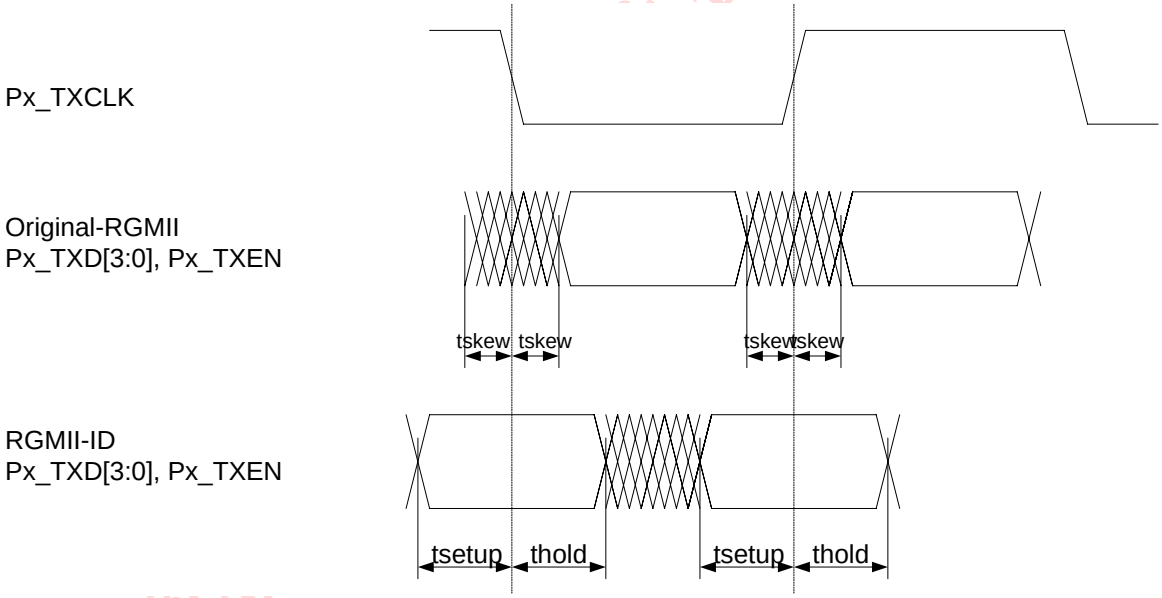


Figure 21: RGMII Output Timing Diagram



16.10 TWSI Interface AC Timing

Notes

- SDA setup and output delay timing is in reference to the SCK rising edge.
- SDA hold time is referred to the SCK rising edge.

Table 49: TWSI Interface AC Timing

Signals	Description	Min.	Max.	Units	Load
SCK	Frequency		100	KHz	
SCK	Clock Cycle	10		us	
SDA	Setup	250		ns	
SDA	Hold	0		ns	
SDA	Output Delay	6	7	µs	20 pF

16.11 JTAG Interface AC Timing

Note

JT_DI and JT_MS setup and hold times, and JT_DO output delay, are referred to JT_CLK falling edge.

Table 50: JTAG Interface AC Timing

Signals	Description	Min.	Max.	Units	Load
JT_CLK	Frequency		1	MHz	
JT_CLK	Clock Cycle	1000		ns	
JT_DI, JT_MS	Boundary scan data setup	75		ns	
JT_DI, JT_MS	Boundary scan data h old	10		ns	
JT_DO	Boundary scan data output delay	1	75	ns	

Section 17. 844 PBGA Package Mechanical Information

Figure 22: 844 PBGA Package Diagram

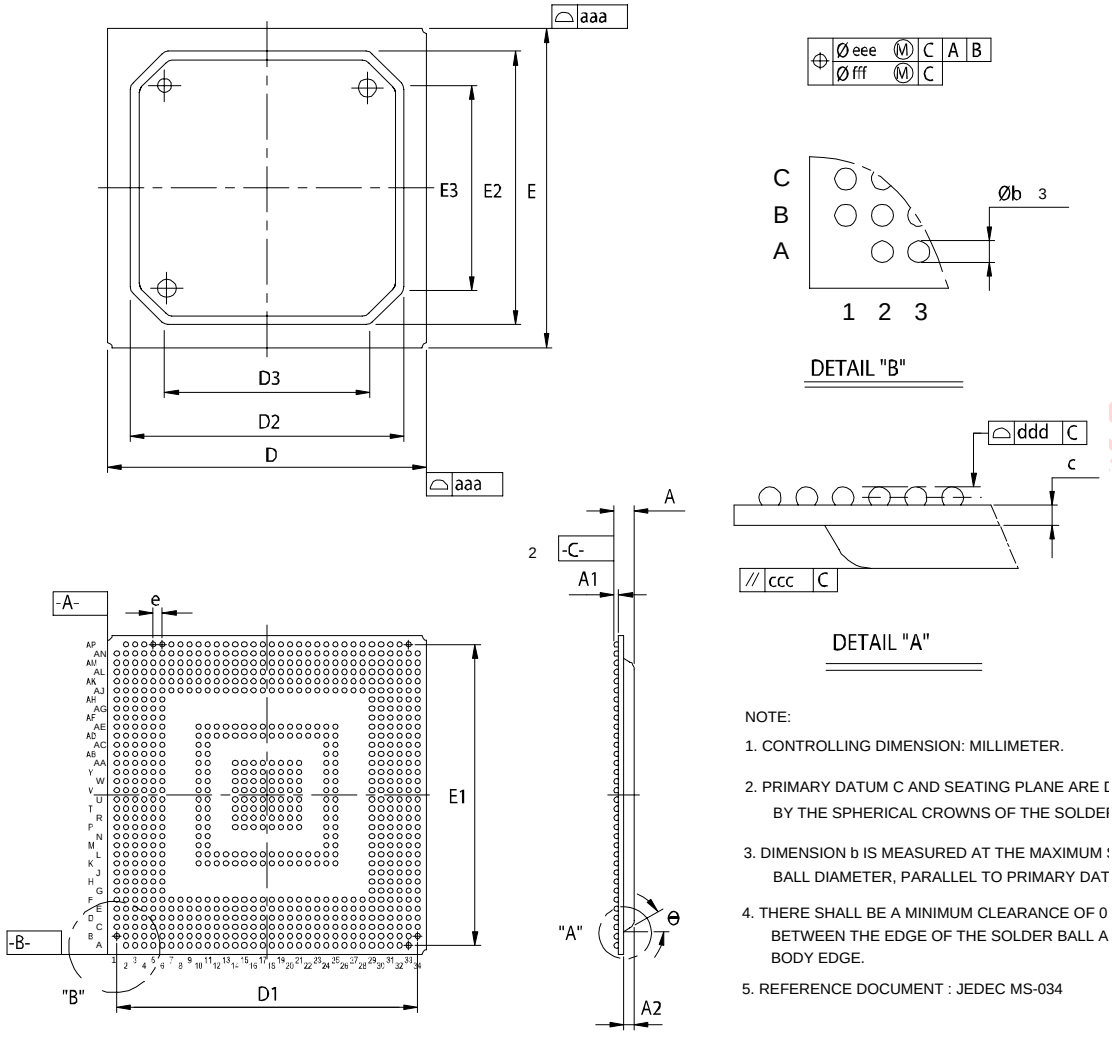


Table 51: Package Dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.00	2.13	2.26	0.079	0.084	0.089
A1	0.30	0.40	0.50	0.012	0.016	0.020
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.40	0.50	0.60	0.016	0.020	0.024
c	0.51	0.56	0.61	0.020	0.022	0.024
D	34.80	35.00	35.20	1.370	1.378	1.386
D1	---	33.00	---	---	1.299	---
D2	29.80	30.00	30.20	1.173	1.181	1.189
D3	---	22.50	---	---	0.886	---
E	34.80	35.00	35.20	1.370	1.378	1.386
E1	---	33.00	---	---	1.299	---
E2	29.80	30.00	30.20	1.173	1.181	1.189
E3	---	22.50	---	---	0.886	---
e	---	1.00	---	---	0.039	---
aaa	0.20			0.008		
ccc	0.20			0.008		
ddd	0.15			0.006		
eee	0.30			0.012		
fff	0.15			0.006		
θ	30° TYP			30° TYP		

Section 18. Part Order Numbering/Package Marking

Figure 23 is an example of the part order numbering scheme for the MV64440/1/2

Figure 23: Sample Part Number

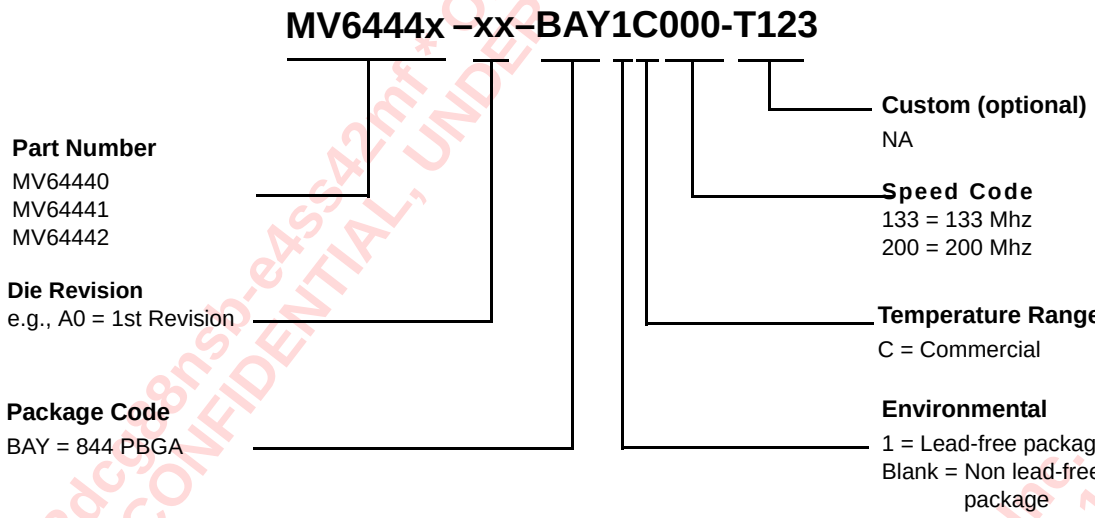
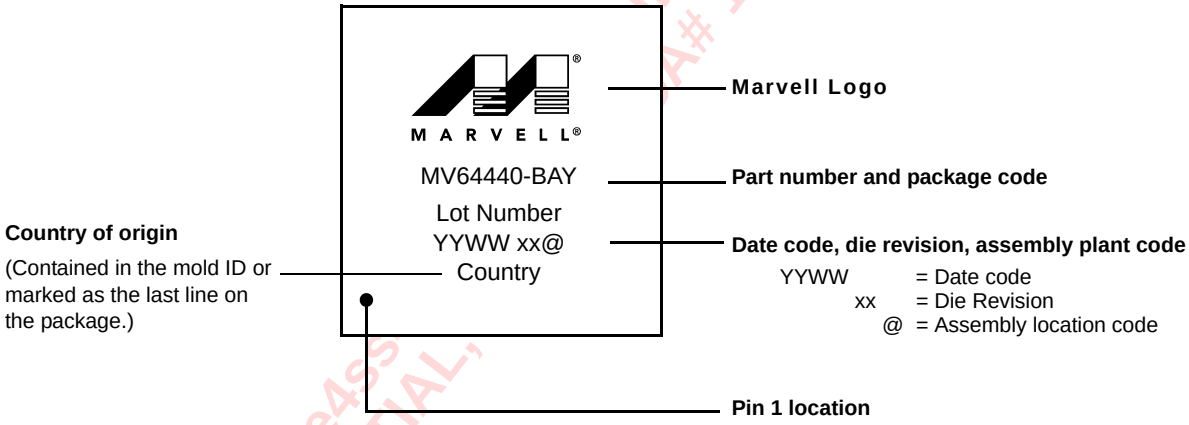


Table 52: MV64440/1/2 Part Order Options

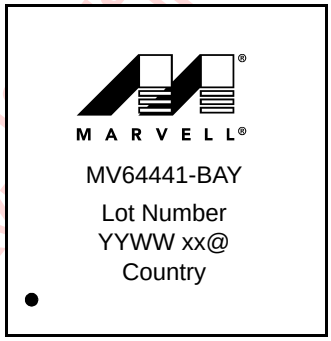
Package Type	Part Order Number
PBGA (844 pins; 35 x 35 mm)	MV64440-xx-BAY1C133
	MV64440-xx-BAY1C200
	MV64441-xx-BAY1C133
	MV64441-xx-BAY1C200
	MV64442-xx-BAY1C133
	MV64442-xx-BAY1C200

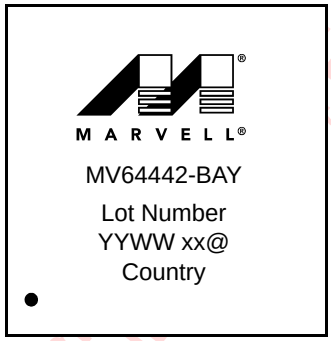
Figure 24 is an example of the package marking and pin 1 location for the MV64440/1/2 package.

Figure 24: Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.





Appendix A. Revision History

Table 53: Revision History

Document Type	Revision	Date
Datasheet	Rev. A	June 19, 2003

NOTE: Revision history items separated between new Hardware Specifications and User Manual.

1. Added additional voltage information in Table 4, “Pin Supply Voltage Levels,” on page 27.
2. Included recommended resistor value for CPU_CAL, PCIx_CAL, and ETHER_CAL in Section 4.3 "Interface Pin Assignments" on page 27.
3. Added the following note to Px_CRS in Table 12, “Ethernet Port0 Interface Pin Assignments,” on page 39 and Table 13, “Ethernet Port1 Interface Pin Assignments,” on page 42:

NOTE: Px_CRS is an I/O when configured to SyncFIFO interface.

4. Added RGMII_VREF to Table 14, “Ethernet Control Interface Pin Assignments,” on page 45. Also, revised the description for CLK125. Added the following note to FIFOCLK:

NOTE: Must not exceed TCLK (core clock) frequency.

When not using the FIFO interface, connect to V_ETH0/1.

5. Revised the descriptions in Table 17, “JTAG Pin Assignment,” on page 46.
6. Added the following note to Section 13. “Reset Pins and Configuration” on page 84:

NOTE: Pad calibration takes 280 SYS_CLK cycles following SYS_RST de-assertion. The CPU must not access the MV64440/1/2 device during calibration time. The CPU must be held in a reset state for 280 SYS_CLK cycles, following MV64440/1/2 SYS_RST de-assertion.

7. Revised the following note in Section 12. “Clocking” on page 82:

NOTE: The TCLK frequency must be greater than 83 MHz. The SYS_CLK frequency must be greater than 100 MHz. The SYS_CLK frequency cannot be more than twice as fast as the TCLK frequency.

8. Added the following note to Dev_AD [18] Sync Mode in Table 29, “Reset Configuration,” on page 84:

NOTE: The synchronizers bypass does not affect the DRAM controller to crossbar synchronization. To bypass the DRAM controller to crossbar synchronization, set the CRdSyncEn bit [8] in the Dunit Control (Low) register.

9. Revised DEV_AD [22] in Table 29, “Reset Configuration,” on page 84. It is now used for SYS_CLK PLL Control. Also, added DEV_WEn [3:1] for SYS_CLK PLL 1, 2, and 3 Control.
10. Revised the parameters in Section 14. “Electrical Specifications” on page 94.
11. Revised the parameters in Section 16. “AC Timing” on page 102.
12. New package diagram in Section 17. “844 PBGA Package Mechanical Information” on page 123.The new drawing does not include a heat slug.

Table 53: Revision History

Document Type	Revision	Date
Datasheet	Rev. B	July 22, 2004

1. No longer supports FCRAM technology. Deleted this information from:
   - Section 4. “Pin Information” on page 21, including Table 10, “DDR SDRAM Interface Pin Assignments,” on page 36.
   - Table 29, “Reset Configuration,” on page 84 (DEV_AD[20] is now reserved. Must be set to 0.)
2. References to the correct resistor value to use have been replaced with the following note:

NOTE: See *TB-119: MV644xx Design Considerations* for the recommended values of the calibration resistors.

This change also applies to:
   - The descriptions of CPU_CAL, PCIx_CAL, M_DCAL, M_ACAL, and ETHER_CAL signal descriptions in Section 4. "Pin Information" on page 21.
   - The Gigabit Ethernet Port I/O descriptions in the following sections:
     Section 8.2 "Gigabit Ethernet Ports I/Os" on page 71
     Section 9.2 "Gigabit Ethernet Ports I/Os" on page 74
     Section 10.2 "Gigabit Ethernet Ports I/Os" on page 77
   - Section 16.3 "DDR SDRAM Interface" on page 105
3. Removed the MPSC Bisync support from the Hardware Specification.
4. Revised Table 4, “Pin Supply Voltage Levels,” on page 27. Added the following note for the Gigabit Ethernet interface:

NOTE: If working with a RGMII 3-port configuration, Port2 uses V_ETH0 segment.

5. Changed the voltage for PLL0_VDDAH and PLL1_VDDAH in Table 5, “Clock Pin Assignments,” on page 27. The quiet power supply is 2.5V. This change also applies to Section 12.2 "PLL Power Supply" on page 83.
6. Revised the note in the PCI_GNT0/1 description (Table 7, “PCI Bus 0 Interface Pin Assignments,” on page 30 and Table 8, “PCI Bus 1 Interface Pin Assignments,” on page 33) as follows:

NOTE: When using the internal PCI arbiter, a pull down is required.

7. Changed the description for the MDC signal in Table 14, “Ethernet Control Interface Pin Assignments,” on page 45. MDC is the CLK input divided by 128.
8. Deleted the M_FBCLK_OUT to M_FBCLK_IN pins from the SDRAM unused interface information in Table 18, “Unused Interface Strapping,” on page 47. These pins don’t exist in this device.
9. Revised pinout map for MV64441 in Section 6. “MV64441 Pinout Map and Table, 844 Pin BGA” on page 54. The following signals were changed.
   - AK23 was PCI0_REQ64n replaced with Pull Up.
   - AP25 was pull-up replaced with NC
10. Revised pinout map for MV64442 in Section 7. “MV64442 Pinout Map and Table, 844 Pin BGA” on page 60. The following NC signals are now pull down: W1, W2, W3, W4, W5, V1.
11. Revised note in Section 12. “Clocking” on page 82 to:

NOTE: The PCI clock frequency must not exceed the TCLK frequency. Also, the TCLK clock frequency must not exceed the SYS_CLK frequency.

Table 53: Revision History

Document Type	Revision	Date

12. In Table 29, “Reset Configuration,” on page 84, made the following changes:
    - Revised the following note for P1_TXD[5:3].

NOTE: Relevant for the MV64440 device, reserved in the MV64442 and must be tied to pull-downs in the MV64441 device.

- Changed the DEV_AD description to:
  000 = PCI33
  100 = PCI66 and PCI-X
- Changed the SYS_CLK PLL Control description for DEV_WEn[3:1] to:
  101 = VDD_CLK is tied to 3.3V
  000 = VDD_CLK is tied to 2.5V
  001 = VDD_CLK is tied to 1.8V
  001 = VDD_CLK is tied to HSTL

13. Added the following notes after Table 30, “PCI Reset Configuration,” on page 89.

NOTE: The correct values for PCIx_M66EN, PCIx_DEVSELn, PCIx_STOPn, and PCIx_TRDYn must be driven during SYSRSTn de-assertion. If PCIx_RST is de-asserted after SYSRSTn de-assertion, these pins must be driven with the correct configuration before SYSRSTn is de-asserted.

Synchronizers bypass is only allowed if the external TCLK and SYS_CLK inputs come from the same clock source, and have equal trace lengths from the clock source to the clock inputs (zero skew). The SYS_CLK PLL control (DEV_WEn[3:1]) must have the same value as the TCLK PLL control (P0_TXD[6:4]), to avoid skew between the two clocks. The sync mode may only be used when the CPU interface is configured to 2.5V or 3.3V, avoid when working with 1.8V.

The synchronizers bypass does not affect the DRAM controller to crossbar synchronization. To disable the DRAM controller to crossbar synchronization, reset the CRdSyncEn bit [8] in the Dunit Control (Low) register (see Table 208 on page 373).

14. Expanded Section 14.1 "Power-Up Sequence Requirements" on page 94 with additional device specific details.

15. Changed the operating case temperature in Table 32, “Absolute Maximum Ratings,” on page 96 to:
- Minimum: -40C
- Maximum: 125C

16. In Table 31, “MV64440/1/2 Power, Reset, and Clock Domains,” on page 95, made the following changes:
    - The PLLX_VDDAH voltage is now to 2.5V.
    - The voltage for M_SSTLVREF_0/1 is VDD_DRAM.

17. Revised Table 33, “Recommended Operating Conditions,” on page 97.

18. Added test condition for DC characteristic values to Table 35, “DC Electrical Characteristics Over Operating Range,” on page 98.

19. Added values to Table 36, “Power Consumption,” on page 100.

20. Revised the thermal data in Table 37, “Thermal Data for the MV64440/1/2 in BAY 844,” on page 101.

Table 53: Revision History

Document Type	Revision	Date
21. Made the following changes to Table 38, “Clock AC Timing,” on page 102: • Revised the following note: **NOTE:** The AC timing parameters in this specification are preliminary and subject to change, except for the following interfaces for which the AC timing values are final: CPU interface at 2.5V, PCI interface, and device bus interface. • The jitter timing for SYS_CLK and TCLK parameter is 200 ps and defined as peak to peak jitter. • The PLL lock time for SYS_CLK and TCLK as 1 ms. • Added spread spectrum requirements, ^{f}mod and ^{f}spread, for the SYS_CLK and TCLK signals. 22. Added information about working in Synch mode to 16.2 “MIPS CPU Interface” on page 103. 23. Revised hold and output delay in Table 16.5, “PCI Interface in PCI-X Mode,” on page 110 and Table 16.6, “PCI Interface in Conventional PCI Mode at 66 MHz,” on page 112 24. Added the following diagrams to 16.3 DDR SDRAM Interface: • Figure 17: "DDR Output Delay Timing Diagram", on page 109 • Figure 18: "DDR Setup Timing Diagram", on page 110 25. Added ^{t}DSS, ^{t}DSH, ^{t}DQSL, and ^{t}DQSH to Table 40, “DDR SDRAM AC Timing (200 MHz),” on page 105, Table 41, “DDR SDRAM AC Timing (166 Mhz),” on page 106, and Table 16.7, “PCI Interface in Conventional PCI Mode at 33 MHz,” on page 113. 26. Added spread spectrum ^{f}mod and ^{f}spread parameters to Table 44, “PCI Interface in PCI-X Mode AC Timing,” on page 111 and Table 45, “PCI Interface in Conventional PCI Mode at 66 MHz AC Timing,” on page 112. 27. Revised Table 48, “Gigabit Ethernet Interface AC Timing,” on page 117. 28. Revised the package diagram in Figure 22: "844 PBGA Package Diagram", on page 123.		
Datasheet	Rev. C	January 18, 2005
1. Throughout specification, M_DQSn was changed to M_DQS. 2. According to the errata document, Sync Mode in the CPU interface is no longer supported. 3. According to the errata document, deleted Multi-MV support in the device. This includes deleting: • Support for up to four slave devices (MV64440/1/2 or other slave devices) on the same CPU bus. • SYS_READY_INn from Table 6, “CPU Interface Pin Assignments,” on page 28. 4. Added the following notes in Table 14, “Ethernet Control Interface Pin Assignments,” on page 45: • To the CLK125 signal description: **NOTE:** When all of the used Ethernet ports are configured to MII only mode, tie it to pull down. Any other configuration requires an input of 125 MHz clock from the PHY. • To the MDIO signal description: **NOTE:** When at least one of the GbE ports is used, it is highly recommended to connect the MDIO signal to a pull up resistor. 5. Added the following note to Table 16, “TWSI Pin Assignment,” on page 46: **NOTE:** These pins are driven low during reset assertion. 6. Added the following note to Table 17, “JTAG Pin Assignment,” on page 46: **NOTE:** The JTAG pins are not 5V tolerant.		

Table 53: Revision History

Document Type	Revision	Date
7. Added the following note to Table 18, “Unused Interface Strapping,” on page 47: **NOTE:** When the Ethernet port is not used, tie MDC/MDIO and CLK125 to pull down. 8. Revised Table 27: "Gigabit Unit Pins Multiplexing", on page 77 to show that P0_TXEN also is available GbE P0(RGMII). 9. Changed pins H31, H32, and J34 to VSS in Section 5. "MV64440 Pinout Map and Table, 844 Pin BGA" on page 48, Section 6. "MV64441 Pinout Map and Table, 844 Pin BGA" on page 54, and Section 7. "MV64442 Pinout Map and Table, 844 Pin BGA" on page 60. These pins were previously SYS_READY_INn and used for the Multi-MV mode, only. 10. The following changes were made in Table 29, “Reset Configuration,” on page 84: • DEV_AD[18] must pull low. • DEV_AD[22] setting 0 is now VDD_CLK tied to HSTL. • For DEV_WEn[3:1], corrected the setting for VDD_CLK is tied to HSTL to 011. • Revised the reset configuration for DEV_AD[28:26] and DEV_AD[31:29]. Instead of settings ’000’ (PCI33) and ’100’ (PCI66 and PCI-X), only use setting '100’ for all modes. Also, added the following note: **NOTE:** Subject to change. For further details about the PCI re-sampling mode, see the notes after Table 30 on page 89. • Added the following note to P0_TXD[7]: **NOTE:** When required to bypass the pad calibration sequence, for example in a JTAG operation, sampling this signal high results in a consistent value setting for all calibration interfaces, without calibrating the values according to the external resistors values. 11. Added the following notes to Section 13.3 "Serial ROM Initialization" on page 90. **NOTE:** While serial ROM is active the INITACT is driven high. Since INITACT signal is multiplex on the MPP interface, the code on the serial interface must make sure that the corresponding MPP pin is correctly configured to drive the INITACT signal. Since the INITACT signal is not driven before reset, the system must pull it to 1 (active state).		

Table 53: Revision History

Document Type	Revision	Date
12. Finalized AC timing. See Section 16. "AC Timing" on page 102 for the latest AC parameters. The changes to these parameters include: • CPU Interface – 3.3V LVTTL CPU_SYSCMD[8:0], CPU_VALID_INn, CPU_SYSRDY_OUTn, CPU_PACKn, CPU_RSSWAPn, CPU_TCDOEn, and CPU_TCWORD[1:0]: Maximum delay modified from 2.5 ns to 2.7 ns. All Multi-MV dedicated signals timing were removed. • CPU Interface – 2.5V LVCMOS CPU_SYSCMD[8:0], CPU_VALID_INn, CPU_SYSRDY_OUTn, CPU_PACKn, CPU_RSSWAPn, CPU_TCDOEn, and CPU_TCWORD[1:0]: Maximum delay modified from 2.6 ns to 2.8 ns. All Multi-MV dedicated signals timing were removed. • CPU Interface – 1.5V HSTL CPU_TCTCEn, CPU_SYSCMD[8:0], CPU_VALID_OUTn, CPU_RELEASEn, CPU_PREQn, and CPU_TCMATCH: Minimum setup modified from 1.7 ns to 1.95 ns. CPU_SYSAD[63:0], CPU_SYSADC[7:0], CPU_SYSRDY_OUTn, CPU_TCWORD[1:0], CPU_VALID_INn, CPU_SYSCMD[8:0], CPU_PACKn, CPU_RSSWAPn, and CPU_TCDOEn: Maximum delay modified from 3.4/3.55 ns to 3.6 ns. All Multi-MV dedicated signals timing were removed. • DDR SDRAM AC Timing (200 MHz/166 Mhz/133 Mhz) t_{DS}, t_{DH}, t_{DIPW}, t_{DSi}, t_{DHi}: Timing finalized and meets DDR JEDEC specifications. • Ethernet RGMII (RGMII and RGMII-ID) Interface Px_RXD[3:0], Px_RXDV: Input hold modified from 0.64 ns to 0.8 ns. Added 10 pF load for the Px_TXD[3:0] and Px_TXEN output timing. • Ethernet PCS Interface (10 bit interface, TBI) Px_TX[9:0]:Minimum delay modified from 1.5 ns to 1.3 ns. • Ethernet GMII Interface Px_RXD[7:0], Px_RXDV, Px_RXERR: Input hold modified from 0 ns to 0.15 ns. • Sync FIFO interface: Added 10 pF load for the Fx_TXD[15:0], Fx_TXEN, Fx_TXVALID, Fx_TXLBE output timing. • The TWSI interface timing was revised with new frequency, clock cycle, setup, hold and output parameters. The previous values were mistakenly measured in reference to the TCLK domain, not SCK. 13. Revised the package dimensions in Table 51, “Package Dimensions,” on page 124. 14. Added lead free package information to Figure 23: "Sample Part Number", on page 125.		

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