Broadcom BCM912500A (SWARM) Evaluation Board for the BCM12500 Broadband Processor

User Manual

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Product Overview

The BCM912500A is an evaluation board for the BCM12500 dual processor SOC (system-on-chip) and has been implemented in the standard ATX form factor. The board makes use of all the interfaces of the BCM12500. To provide examples for both hardware and software designers, wherever possible configurable interfaces are used in all their modes.

The board comes in an box with its own ATX power supply. Common, off-the-shelf peripherals can be added, such as PCI graphics adapters, USB keyboards and mice, and ATA hard disks. In addition, the board has provisions for a few specialized applications including PCMCIA and HyperTransport (formerly LDT) peripherals.

Hardware Features

- ***66MHz PCI local bus*** (rev. 2.2 compliant): There are two 3.3V only, 32 bit slots directly interfaced to the BCM12500. Each slot can handle master or slave devices. Central arbitration is handled by the BCM12500.
- ***Two serial ports***: Serial port 0 is configured as a standard asynchronous UART with an RS232 interface. Serial port 1 is multiplexed to be either an additional UART with RS232, or an Audio Codec utilizing a synchronous protocol.
- ***Four DDR SDRAM slots***: Each slot can accept a two bank, 184 pin DDR DIMM, with 64 bit data path and optionally 8 bit ECC. A 133MHz clock rate (266MHz data) with all DIMM's fully populated yields a peak bandwidth of 32Gbit/s. Maximum available memory is 2GB when using 256Mbit DRAM. As denser memories become available, memory size can scale to 8GB total. The board comes with two 128MB single-sided ECC-protected DIMMs, one in each channel.
- ***LDT to LDT and PCI Bridge***: This device provides a bridge from the BCM12500 LDT interface to two additional 64 bit 66MHz PCI slots and an LDT socket.
- ***Two Gigabit Ethernet Ports***: The ports support the 1000BASE-T/100BASE-TX/10BASE-T connection on standard CAT 5 UTP cable.
- ***NTSC/PAL Video Decoder***: S-video and RCA connectors allow for connection to standard sources such as video cameras and VCRs. This is used to demonstrate the 8 bit Packet Fifo interface option of the BCM12500.
- ***Four USB ports***: Dual USB host controllers housed in one multi-function PCI device provide the ability to connect USB peripherals such as keyboards, mice, and any other USB rev. 1.1 compliant devices.
- ***JTAG, EJTAG*** headers for debug and test.
- ***16Mbit (2Mx8) FLASH ROM*** for boot code. In parallel, a header is provided to allow connection to a PROMICE ROM emulator to allow fast development of bootstrap code.
- ***4 character LED display*** for system boot error codes.
- ***IDE interface***. Standard 40 pin connector allows connection of IDE devices that are ATA/ATAPI PIO

Mode3 compliant.

- ***PCMCIA interface*** supporting a single memory or I/O card.
- ***Two SMBus interfaces*** for simple 2 wire devices. Connected to this bus is an RTC(real time clock), an E2PROM that can be used as an alternate boot device, and a temperature sensor that works in conjunction with the BCM12500's internal temperature diode. The DIMM serial presence detect (SPD) configuration devices are also on this interface.

Firmware

The BCM912500A board can use both the 32 bit PMON firmware, which is based on an open source project, or CFE which was developed at Broadcom to support 32 and 64 bit operation and is optimized for the BCM12500 and its successors.
Both firmware solutions initialize the CPUs, including their caches, and the peripherals on the BCM12500 including the L2 cache, memory controller, Ethernet MACs and UARTs. They configure the HyperTransport fabric and PCI bus devices on the board. Furthermore, they provide an environment for downloading and booting an Operating System. While PMON can download the OS only via the network, CFE can also use a disk or flash memory as its boot device. CFE includes support for starting and stopping the second CPU core on the BCM12500.
For additional information on CFE in conjunction with the BCM912500A board, please refer to the Common Firmware Environment (CFE) Functional Specification.

Operating System Support

Three operating systems are provided for the BCM912500A. Device drivers are provided giving examples of how the many modes of the BCM12500 interfaces are used.

- ***VxWorks version 5.4*** with 64 bit support for data. VxMP, i.e. a VxWorks kernel running independently on each core, is an available option. Users will need to use the Tornado tools version 2.1 for 64 bit or VxMP support. The BSP for the BCM912500A board is a supported product by Wind River Systems, although initially the BSP in source form will be available only from Broadcom.
- ***NetBSD version 1.5*** running in 32 bit mode. This kernel runs on a single CPU. Full source code is available initially from Broadcom, but will be contributed back into the public domain.
- ***Linux version 2.4.2*** running in 64 bit SMP (symmetric multiprocessing) mode. Full source code is available initially from Broadcom, but will be contributed back into the public domain.

Jumper and Switch Settings

The following pages describe in short the various jumper and switch settings on the BCM912500A board. Among other functions, the jumpers and switches are used to set the boot configuration of the BCM12500, configure the JTAG chain, control the PCI clocks, the USB controller, the power supplies and so on.

Before changing any of the default values set by Broadcom, please carefully review the tables below, look at the BCM912500A schematics and review the user manual and datasheet for the BCM12500. If you have questions or comments, please send them to hardware-support@sibyte.com.

Jumper Switch	Description (installed / not installed) Factory default in ***italics***	BCM912500A Schematic Page
J1	***big endian*** / little endian	6
J2	**Boot Mode** SMBus / ***generic bus ROM***	6
SW2, J3	PLL div[4, 2..0], PLL div[3] see Table 2: PLL Switch Settings	6
J4	**IOB Clock Divisor** IOB1: *2* / 3 IOB0: *3* / 4	6
SW1	Set config[5..3] to selected value (0..7 = 8..F) Software can read these values, check CFE manual for their meaning ***default: 2 for UART0 console, PCI/LDT initialization***	6
J5	PLL bypass / ***PLL enabled***	8
J6, J7	**PCI Clock Select** ***Nothing: run at slowest PCI card*** speed 1-2: force 33 MHz **Use the following only without any PCI cards in the slots!** 2-4: Force 66 MHz 1-2, 3-4: Tristate, Clock Gen disable 3-4: DON'T USE	8
J57, J58 J61, J62	Enable JTAG / ***normal operation***	16, 17
J19	***Enable USB*** (all 32-bit PCI cards at 33 MHz) / disable USB **Caution: always install/remove all 4 jumpers together!**	20
J63-66	Sturgeon reference clock time tunnel Short 1-2, 3-4 to add delay Cut trace to 3 and from 1 and short 2-4 to reduce delay	22
SW6-8	**Sturgeon LDT-PCI bridge link speed select** see Table 3: Sturgeon Data Rate Selects *0 is default for 800 Mbps*	22
J31	*1-3, 2-4: select FLASH for main ROM (flash0); PROMICE is secondary (flash1)* 1-2, 3-4: select PROMICE for main ROM (flash0); FLASH is secondary (flash1)	26
J40	JTAG chain setup, see Table 4: JTAG Configuration *Default: BCM12500 as only member of chain*	32
J41	Permanent COLD_RESET / ***COLD_RESET controlled by SW9 and power button on case***	33
J42	If J43 installed: Permanent WARM_RESET / ***WARM_RESET controlled by SW10 and reset button on case***	33
J43	***Allow J42, SW10 to control WARM_RESET*** / only allow EJTAG_RESET to control WARM_RESET	33
J44	Permanent non-maskable interrupt (GPIO3) / ***NMI controlled by SW11***	33
J45	Permanent SYS_RESET (rest of board) / ***SYS_RESET controlled by BCM12500***	33
SW9-12	Pushbuttons for resets and interrupts	33
J47	***2-4: 2.5V, 1.25V come up together*** removed: 2.5V, 1.25V come up individually 1-2: disable 2.5V 3-4: disable 1.25V	34
SW13	**Board power supply switch** ON: towards the edge of the board OFF: middle or towards the CPU position	35
SW14	**VDDCore setting (default 9)** 0-7: 25mV increments from 1.1V 8-F: 50mV increments from 1.25V	36

Table 1: Jumpers and Switches

IO_ AD[11..7]	J3 1=Installed	SW2	Multiplier	Core CLK
00000	1	0	UNDEF	UNDEF
00001	1	1	UNDEF	UNDEF
00010	1	2	UNDEF	UNDEF
00011	1	3	UNDEF	UNDEF
00100	1	4	2	200
00101	1	5	2.5	250
00110	1	6	3	300
00111	1	7	3.5	350
01000	0	0	4	400
01001	0	1	4.5	450
01010	***0***	***2***	***5***	***500***
01011	0	3	5.5	550
01100	0	4	6	600
01101	0	5	6.5	650
01110	0	6	7	700
01111	0	7	7.5	750
10000	1	8	8	800
10001	1	9	8.5	850
10010	1	A	9	900
10011	1	B	9.5	950
10100	1	C	10	1000
10101	1	D	10.5	1050
10110	1	E	11	1100
10111	1	F	UNDEF	UNDEF
11000	0	8	UNDEF	UNDEF
11001	0	9	UNDEF	UNDEF
11010	0	A	UNDEF	UNDEF
11011	0	B	UNDEF	UNDEF
11100	0	C	UNDEF	UNDEF
11101	0	D	UNDEF	UNDEF
11110	0	E	UNDEF	UNDEF
11111	0	F	UNDEF	UNDEF

Table 2: PLL Switch Settings

SW6 (for Link0 to BCM12500) SW7 (for link1 to connector)	Sel	SW8 0/4/8/C	SW8 1/5/9/D	SW8 2/6/A/E	SW8 3/7/B/F
0	VCO	***800***	1066	1600	REFCLK
1	DIV2	400	533	800	REFCLK
2	VCO	800	1066	1600	REFCLK
3	DIV4	200	266	400	REFCLK
4	VCO	800	1066	1600	REFCLK
5	DIV2	400	533	800	REFCLK
6	VCO	800	1066	1600	REFCLK
7	BYP	REFCLK			
8-F = 0-7					

Table 3: Sturgeon Data Rate Selects

J40	JTAG chain
1-2	***BCM12500 at head of chain***
3-4	CPLD at head of chain (bypass BCM12500)
5-6	CPLD after BCM12500
5-6 .. 13-14	Install/remove jumpers to insert/remove additional parts in chain. Note: install J57, J58, J61, J62 to make PHYs part of chain
17-18	***Install for shortcut after BCM12500***
19-20	Install for shortcut after CPLD
21-22 .. 27-28	Add additional parts to end of chain

Table 4: JTAG Configuration

Connectors

The back panel has from-left to right

- 2 UARTs (UART0 bottom, UART1 top)
- Audio in
- Audio out
- 4 USB ports (TBD)
- composite video IN
- SVideo IN
- 2 3.3V only 32-bit, 66 MHz PCI slots
- 2 3.3V only 64-bit, 66 MHz PCI slots
- 1 HyperTransport slot

The front side of the board has from left to right

- Gigabit Ethernet port 1
- Gigabit Ethernet port 0
- ATX power connector

UART/Serial Console

A standard 9-pin RS232 null-modem cable to the PC should be used to hookup port UART0 to the terminal. Set the baud rate to 115200, 8-bit, no parity. CFE supports devices uart0: and uart1: for downloading software. Alternatively, you can use promice0:, if you hook up a write line from the PROMICE emulator to pin 1 of J67. If you set the configuration switch SW1 to 1, promice0: will be used by CFE as its serial console.