SSC Address Map

Region	Virtual	Physical	Size	Region	Path	Notes
Internal registers	00.b000.0000	00.1000.0000	256MB	kseg1	-	
Local memory	00.1000.0000	00.0000.0000	256MB	TLB -- cached	Mem controller	512MB is populated on SSC
	00.2000.0000	00.8000.0000	256MB	TLB -- cached	Mem controller	
	n/a	00.9000.0000	256MB	Reserved	Mem controller	
	n/a	00.c000.0000	256MB	Reserved	Mem controller	
TXRX Shared Memory	00.4000.0000	f8.1a00.0000	16MB	TLB -- cached	PCI	
FP Shared Memory	00.4200.0000	f8.1b00.0000	16MB	TLB -- cached	PCI	
BM-FPGA	00.5000.0000	f8.1f40.0000	2MB	TLB -- uncached	PCI	
CF Controller I/O	00.5200.0000	00.dc00.0000	2MB	TLB -- uncached	PCI	
CF Controller Memory	00.5480.0000	f8.0080.0000	2MB	TLB -- uncached	PCI	
RTC	00.bf00.0000	00.1f00.0000	2MB	kseg1	Generic bus	
Non-boot PROM	00.bec0.0000	00.1f60.0000	2MB	kseg1	Generic bus	
PROM	00.bfc0.0000	00.1f80.0000	2MB	kseg1	Generic bus	

Notes:

See BCM1125 User's Manual for more information on physical addresses
Other addressing, e.g. xkphys, may be used to access physical addresses
TLB accesses to memory are preferred because the TLB can use contiguous addressing to non-contiguous physical addresses

TXRX Address Map

Region	Virtual	Physical	Size	Region	Path	Notes
SSC Shared Memory	00.4000.0000	10.6000.0000	16MB	TLB -- cached	PCI	
FP Shared Memory	00.4200.0000	10.1b00.0000	16MB	TLB -- cached	PCI	
BM-FPGA	00.5000.0000	10.1f40.0000	2MB	TLB -- uncached	PCI	
HT Config	00.6000.0000	00.fe00.0000	16MB	TLB -- uncached	HT internal	
High Speed Port Config	00.6200.0000	00.df00.0000	16MB	TLB -- uncached	High speed internal	
Internal registers	00.b000.0000	00.1000.0000	256MB	kseg1	-	
Non-boot PROM	00.bec0.0000	00.1ec0.0000	2MB	kseg1	Generic bus	
PROM	00.bfc0.0000	00.1f80.0000	2MB	kseg1	Generic bus	
Local memory	10.0000.0000	00.0000.0000	256MB	TLB -- cached	Mem controller	Upper 4GB is reserved for larger memory system
	10.1000.0000	00.8000.0000	256MB	TLB -- cached	Mem controller	
	10.2000.0000	00.9000.0000	256MB	TLB -- cached	Mem controller	
	10.3000.0000	00.c000.0000	256MB	TLB -- cached	Mem controller	
	10.4000.0000	01.4000.0000	3GB	TLB -- cached	Mem controller	
	11.0000.0000	20.0000.0000	4GB	TLB -- cached	Mem controller	
Local memory	40.0000.0000	40.0000.0000	64GB	TLB -- cached	ccNUMA	
FP Shared Memory	50.0000.0000	50.0000.0000	64GB	TLB -- cached	HT port 2	

Notes:

See BCM1480 User's Manual for more information on physical addresses
Other addressing, e.g. xkphys, may be used to access physical addresses
TLB accesses to memory are preferred because the TLB can use contiguous addressing to non-contiguous physical addresses

FP/FC Address Map

Region	Virtual	Physical	Size	Region	Path	Notes
SSC Shared Memory	00.4000.0000	10.6000.0000	16MB	TLB -- cached	PCI	
TXRX Shared Memory	00.4200.0000	10.1a00.0000	16MB	TLB -- cached	PCI	
BM-FPGA	00.5000.0000	10.1f40.0000	2MB	TLB -- uncached	PCI	
HT Config	00.6000.0000	00.fe00.0000	16MB	TLB -- uncached	HT internal	
High Speed Port Config	00.6200.0000	00.df00.0000	16MB	TLB -- uncached	High speed internal	
QLogic registers	00.7000.0000	f0.0000.0000	256MB	TLB -- uncached	HT port 0	
Internal registers	00.b000.0000	00.1000.0000	256MB	kseg1	-	
Non-boot PROM	00.bec0.0000	00.1ec0.0000	2MB	kseg1	Generic bus	
PROM	00.bfc0.0000	00.1f80.0000	2MB	kseg1	Generic bus	
Local memory	10.0000.0000	00.0000.0000	256MB	TLB -- cached	Mem controller	Upper 4GB is reserved for larger memory system
	10.1000.0000	00.8000.0000	256MB	TLB -- cached	Mem controller	
	10.2000.0000	00.9000.0000	256MB	TLB -- cached	Mem controller	
	10.3000.0000	00.c000.0000	256MB	TLB -- cached	Mem controller	
	10.4000.0000	01.4000.0000	3GB	TLB -- cached	Mem controller	
	11.0000.0000	20.0000.0000	4GB	TLB -- cached	Mem controller	
TXRX Shared Memory	40.0000.0000	40.0000.0000	64GB	TLB -- cached	HT port 2	
Local memory	50.0000.0000	50.0000.0000	64GB	TLB -- cached	ccNUMA	

Notes:

See BCM1480 User's Manual for more information on physical addresses
Other addressing, e.g. xkphys, may be used to access physical addresses
TLB accesses to memory are preferred because the TLB can use contiguous addressing to non-contiguous physical addresses

SSC Reset Initialization

Bit	Value	Definition	Settings
0	0	reserved	
1	1	clk100_src	Clock source is 100MHz reference clock
2	0	ldt_minrstcnt	Must be 0
3	0	ldt_bypass_pll	Must be 0
4	0	pci_test_mode	Must be 0
5	1	iob0_div	0
6	1	iob1_div	Dd data rate
11:7	01100	pll_div	01000 (400 MHz)
			01000 (450 MHz)
			01010 (500 MHz)
			01100 (600 MHz)
			01101 (650 MHz)
			01110 (700 MHz)
			01111 (750 MHz)
			10000 (800 MHz)
12	0	ser0_enable	Serial port 0 is UART A
13	0	ser0_rstb_en	GPIO0 is GPIO PIN
14	0	ser1_enable	Serial port 1 is UART B
15	0	ser1_rstb_en	GPIO1 is GPIO PIN
16	0	pcmcia_enable	PCMCIA disabled
17	1	boot_mode[0]	IO_CS_L0 is configured as non-muxed bus with 8 bits of data and 24 bits of address
18	0	boot_mode[1]	Boot ROM on generic bus
19	1	pci_host	Host bridge enabled on PCI
20	1	pci_arbiter	PCI arbiter enabled
21	0	southOnLDT	South Bridge on PCI
22	0	big_endian	Little endian enabled
23	1	genclk_en	Enabled io_clk100 output
24	0	ldt_test_en	Must be 0
25	0	gen_parity_en	No parity on generic bus
31:26	000111	config	User config

SSC GPIO bits

Bit	Dir	Description	Notes
1:0	O	SSC Cluster	
3:2	I	SSC Cluster	
4	O	FP Cluster	
5	I	FP Cluster	
6	O	TX Cluster	
7	I	TX Cluster	
8	I	TDO	Used for programming XCF02S PROM for BM-FPGA
9	O	TDI	
10	O	TMS	
11	O	TCK	
12	I	Status interrupt	Configure as edge-sensitive interrupt
13	I	Message interrupt	Configure as edge-sensitive interrupt
14	O	PCI Reset (0 = reset, 1 = enable)	
15	O	Spread spectrum enable (0 = disable, 1 = enable)	

See section 13 GPIO of BCM1250/1125 User's Manual

SSC Registers

Generic Bus Chip Select Address Register

Pin	Address	Value	Description
IO_CS_L0	0xb0061200	0x1fc0	Boot ROM
IO_CS_L1	0xb0061208	0x1f00	RTC
IO_CS_L2	0xb0061210	-	Spare
IO_CS_L3	0xb0061218	-	Spare
IO_CS_L4	0xb0061220	0x1ec0	Non Boot ROM
IO_CS_L5	0xb0061228	-	Spare
IO_CS_L6	0xb0061230	-	Spare
IO_CS_L7	0xb0061238	-	Spare

Generic Bus Region Timing 0

Pin	Address	Value
IO_CS_L0	0xb0061600	0x3824
IO_CS_L1	0xb0061608	0x3824
IO_CS_L2	0xb0061610	-
IO_CS_L3	0xb0061618	-
IO_CS_L4	0xb0061620	0x3824
IO_CS_L5	0xb0061628	-
IO_CS_L6	0xb0061630	-
IO_CS_L7	0xb0061638	-

Generic Bus Region Timing 1

Pin	Address	Value
IO_CS_L0	0xb0061700	0x0677
IO_CS_L1	0xb0061708	0x0677
IO_CS_L2	0xb0061710	-
IO_CS_L3	0xb0061718	-
IO_CS_L4	0xb0061720	0x06f7
IO_CS_L5	0xb0061728	-
IO_CS_L6	0xb0061730	-
IO_CS_L7	0xb0061738	-

Generic Bus Region Size

Pin	Address	Value
IO_CS_L0	0xb0061100	0x003f
IO_CS_L1	0xb0061108	0x000f
IO_CS_L2	0xb0061110	-
IO_CS_L3	0xb0061118	-
IO_CS_L4	0xb0061120	0x003f
IO_CS_L5	0xb0061128	-
IO_CS_L6	0xb0061130	-
IO_CS_L7	0xb0061138	-

Generic Bus Region Configuration

Pin	Address	Value
IO_CS_L0	0xb0061000	0x0880
IO_CS_L1	0xb0061008	0x0080
IO_CS_L2	0xb0061010	-
IO_CS_L3	0xb0061018	-
IO_CS_L4	0xb0061020	0x0080
IO_CS_L5	0xb0061028	-
IO_CS_L6	0xb0061030	-
IO_CS_L7	0xb0061038	-

GPIO Registers

Register	Address	Value
Clear edge	0xb0061a80	Write 1 to bit position to clear edge detector
Interrupt type	0xb0061a88	0x1000
Read	0xb0061aa0	Reads value of register
Input invert	0xb0061a90	Write 1 to invert value when read
Glitch filter select	0xb0061a98	Use default values
Direction	0xb0061aa8	0xc050
Pin Clear	0xb0061ab0	Write 1 to bit position to clear value
Pin Set	0xb0061ab8	Write 1 to bit position to set value

TXRX Reset Initialization

Bit	Value	Definition	Settings
0	1	reserved	Pullup/pulldown depopulated
1	0	ht_minrstcnt	Must be 0
2	0	reserved	Pullup/pulldown depopulated
3	0	reserved	Pullup/pulldown depopulated
4	0	reserved	Pullup/pulldown depopulated
5	1	iob_div	IOB clock is ZCLK / 1.5
10:6	10000	pll_div	01100 (600 MHz)
			01101 (650 MHz)
			01110 (700 MHz)
			01111 (750 MHz)
			10000 (800 MHz)
			10001 (850 MHz)
			10010 (900 MHz)
			10011 (950 MHz)
			10100 (1000 MHz)
15:11	00100	sw_div	00100 (div 1)
			00101 (div 1.25)
			00110 (div 1.5)
			01000 (div 2)
16	0	pcmcia_enable	PCMCIA disabled
17	1	duart1 enable	DUART1 enabled
18	1	boot_mode[0]	IO_CS_L0 is configured as non-muxed bus with 8 bits of data and 24 bits of address
19	0	boot_mode[1]	Boot ROM on generic bus
20	0	pci_host	Device mode on PCI
21	0	pci_arbiter	External arbiter used
22	0	big_endian	Little endian
23	1	genclk_en	Enable output of IO_CLK100
24	0	gen_parity_en	Parity disabled on generic bus
25	1	reserved	Pullup/pulldown depopulated
31:26	000111	config	User config -- bit 29 = 0 => TXRX

TXRX GPIO bits

Bit	Dir	Description	Notes
0	I	TXRX Cluster	
1	O	TXRX Cluster	
3:2	I	Reserved	
4	O	SFP Rate Select	Set to 0
5	O	SFP Transmit Disable	Set to 0
11:6	I	Reserved	
12	I	TXRX Status Interrupt	Configure as edge-sensitive interrupt
13	I	TXRX Message Interrupt	Configure as edge-sensitive interrupt
15:14	I	Reserved	

See section 13 GPIO of BCM1250/1125 User's Manual

TXRX Registers

Generic Bus Chip Select Address Register

Pin	Address	Value	Description
IO_CS_L0	0xb0061200	0x1fc0	Boot ROM
IO_CS_L1	0xb0061208	0x1f00	RTC
IO_CS_L2	0xb0061210	-	Spare
IO_CS_L3	0xb0061218	-	Spare
IO_CS_L4	0xb0061220	0x1ec0	Non Boot ROM
IO_CS_L5	0xb0061228	-	Spare
IO_CS_L6	0xb0061230	-	Spare
IO_CS_L7	0xb0061238	-	Spare

Generic Bus Region Timing 0

Pin	Address	Value
IO_CS_L0	0xb0061600	0x3824
IO_CS_L1	0xb0061608	0x3824
IO_CS_L2	0xb0061610	-
IO_CS_L3	0xb0061618	-
IO_CS_L4	0xb0061620	0x3824
IO_CS_L5	0xb0061628	-
IO_CS_L6	0xb0061630	-
IO_CS_L7	0xb0061638	-

Generic Bus Region Timing 1

Pin	Address	Value
IO_CS_L0	0xb0061700	0x0677
IO_CS_L1	0xb0061708	0x0677
IO_CS_L2	0xb0061710	-
IO_CS_L3	0xb0061718	-
IO_CS_L4	0xb0061720	0x06f7
IO_CS_L5	0xb0061728	-
IO_CS_L6	0xb0061730	-
IO_CS_L7	0xb0061738	-

Generic Bus Region Size

Pin	Address	Value
IO_CS_L0	0xb0061100	0x003f
IO_CS_L1	0xb0061108	0x000f
IO_CS_L2	0xb0061110	-
IO_CS_L3	0xb0061118	-
IO_CS_L4	0xb0061120	0x003f
IO_CS_L5	0xb0061128	-
IO_CS_L6	0xb0061130	-
IO_CS_L7	0xb0061138	-

Generic Bus Region Configuration

Pin	Address	Value
IO_CS_L0	0xb0061000	0x0880
IO_CS_L1	0xb0061008	0x0080
IO_CS_L2	0xb0061010	-
IO_CS_L3	0xb0061018	-
IO_CS_L4	0xb0061020	0x0080
IO_CS_L5	0xb0061028	-
IO_CS_L6	0xb0061030	-
IO_CS_L7	0xb0061038	-

GPIO Registers

Register	Address	Value
Clear edge	0xb0061a80	Write 1 to bit position to clear edge detector
Interrupt type	0xb0061a88	0x1000
Read	0xb0061aa0	Reads value of register
Input invert	0xb0061a90	Write 1 to invert value when read
Glitch filter select	0xb0061a98	Use default values
Direction	0xb0061aa8	0x0033
Pin Clear	0xb0061ab0	Write 1 to bit position to clear value
Pin Set	0xb0061ab8	Write 1 to bit position to set value

FP Reset Initialization

Bit	Value	Definition	Settings
0	1	reserved	Pullup/pulldown depopulated
1	0	ht_minrstcnt	Must be 0
2	0	reserved	Pullup/pulldown depopulated
3	0	reserved	Pullup/pulldown depopulated
4	0	reserved	Pullup/pulldown depopulated
5	1	iob_div	IOB clock is ZCLK / 1.5
10:6	10000	pll_div	01100 (600 MHz)
			01101 (650 MHz)
			01110 (700 MHz)
			01111 (750 MHz)
			10000 (800 MHz)
			10001 (850 MHz)
			10010 (900 MHz)
			10011 (950 MHz)
			10100 (1000 MHz)
15:11	00100	sw_div	00100 (div 1)
			00101 (div 1.25)
			00110 (div 1.5)
			01000 (div 2)
16	0	pcmcia_enable	PCMCIA disabled
17	1	duart1 enable	DUART1 enabled
18	1	boot_mode[0]	IO_CS_L0 is configured as non-muxed bus with 8 bits of data and 24 bits of address
19	0	boot_mode[1]	Boot ROM on generic bus
20	0	pci_host	Device mode on PCI
21	0	pci_arbiter	External arbiter used
22	0	big_endian	Little endian
23	1	genclk_en	Enable output of IO_CLK100
24	0	gen_parity_en	Parity disabled on generic bus
25	1	reserved	Pullup/pulldown depopulated
31:26	001111	config	User config -- bit 29 = 1 => FP

FP GPIO bits

Bit	Dir	Description	Notes
0	I	FP Cluster	
1	O	FP Cluster	
2	I	HT21000 Alert	
3	I	HT21000 Fatal Error	
4	I	HT21000 PME	
5	I	HT21000 Interrupt	
6	I	PCI-e Lane 4 interrupt	Configure as edge-sensitive interrupt
7	I	PCI-e Lane 3 interrupt	Configure as edge-sensitive interrupt
8	I	PCI-e Lane 2 interrupt	Configure as edge-sensitive interrupt
9	I	PCI-e Lane 1 interrupt	Configure as edge-sensitive interrupt
10	I	PCI-e Lane 0 interrupt	Configure as edge-sensitive interrupt
11	I	Reserved	
12	I	FP Status Interrupt	Configure as edge-sensitive interrupt
13	I	FP Message Interrupt	Configure as edge-sensitive interrupt
15:14	I	Reserved	

See section 13 GPIO of BCM1250/1125 User's Manual

FP Registers

Generic Bus Chip Select Address Register

Pin	Address	Value	Description
IO_CS_L0	0xb0061200	0x1fc0	Boot ROM
IO_CS_L1	0xb0061208	0x1f00	RTC
IO_CS_L2	0xb0061210	-	Spare
IO_CS_L3	0xb0061218	-	Spare
IO_CS_L4	0xb0061220	0x1ec0	Non Boot ROM
IO_CS_L5	0xb0061228	-	Spare
IO_CS_L6	0xb0061230	-	Spare
IO_CS_L7	0xb0061238	-	Spare

Generic Bus Region Timing 0

Pin	Address	Value
IO_CS_L0	0xb0061600	0x3824
IO_CS_L1	0xb0061608	0x3824
IO_CS_L2	0xb0061610	-
IO_CS_L3	0xb0061618	-
IO_CS_L4	0xb0061620	0x3824
IO_CS_L5	0xb0061628	-
IO_CS_L6	0xb0061630	-
IO_CS_L7	0xb0061638	-

Generic Bus Region Timing 1

Pin	Address	Value
IO_CS_L0	0xb0061700	0x0677
IO_CS_L1	0xb0061708	0x0677
IO_CS_L2	0xb0061710	-
IO_CS_L3	0xb0061718	-
IO_CS_L4	0xb0061720	0x06f7
IO_CS_L5	0xb0061728	-
IO_CS_L6	0xb0061730	-
IO_CS_L7	0xb0061738	-

Generic Bus Region Size

Pin	Address	Value
IO_CS_L0	0xb0061100	0x003f
IO_CS_L1	0xb0061108	0x000f
IO_CS_L2	0xb0061110	-
IO_CS_L3	0xb0061118	-
IO_CS_L4	0xb0061120	0x003f
IO_CS_L5	0xb0061128	-
IO_CS_L6	0xb0061130	-
IO_CS_L7	0xb0061138	-

Generic Bus Region Configuration

Pin	Address	Value
IO_CS_L0	0xb0061000	0x0880
IO_CS_L1	0xb0061008	0x0080
IO_CS_L2	0xb0061010	-
IO_CS_L3	0xb0061018	-
IO_CS_L4	0xb0061020	0x0080
IO_CS_L5	0xb0061028	-
IO_CS_L6	0xb0061030	-
IO_CS_L7	0xb0061038	-

GPIO Registers

Register	Address	Value
Clear edge	0xb0061a80	Write 1 to bit position to clear edge detector
Interrupt type	0xb0061a88	0x1000
Read	0xb0061aa0	Reads value of register
Input invert	0xb0061a90	Write 1 to invert value when read
Glitch filter select	0xb0061a98	Use default values
Direction	0xb0061aa8	0x0003
Pin Clear	0xb0061ab0	Write 1 to bit position to clear value
Pin Set	0xb0061ab8	Write 1 to bit position to set value

PCI Memory Map

Physical Address	Size	Function	Notes
0000.0400	256	CF Controller I/O socket A	Accessed at base of 0xdc000000; set in ExCA i/o 0
0000.0800	256	CF Controller I/O socket B	Accessed at base of 0xdc000000; set in ExCA i/o 0
0001.0000	64KB	CF Controller I/O ExCA	Accessed at base of 0xdc000000; uses base/index scheme
0080.0000	64KB	CF Controller Memory	Socket memory accesses (set in ExCA memory 0); accessed at base of 0xf8.0000.0000
0081.0000	64KB	CF Controller Socket A / ExCA base	Socket A memory accesses; ExCA mapped at 0x800 offset; accessed at base of 0xf8.0000.0000
0082.0000	64KB	CF Controller Socket B / ExCA base	Socket B memory accesses; ExCA mapped at 0x800 offset; accessed at base of 0xf8.0000.0000
1a00.0000	16MB	TXRX Shared Memory	TXRX accesses this locally at 0x9000.0000
1b00.0000	16MB	FP Shared Memory	FP accesses this locally at 0x9000.0000
1f40.0000	64KB	BM FPGA	
6000.0000	16MB	SSC Shared Memory	SSC accesses this locally at 0x8300.0000

PCI ID

Device	ID
FP	0012166d
TXRX	0012166d
CF	ac55104c
BM FPGA	c00610ee

PCI Configuration

Device	Dev #	IDSEL	Notes
Primary Bus (0)			
FP	5	16	
TXRX	6	17	
CF Controller	7	18	
BM FPGA	8	19	

PCI Reset Configuration

Pin	Value	Description
REQ641_L	1	Disable 64-bit mode
M66EN1	0	Disable 66MHz operation
DEVSEL0_L,	111	Pullups select conventional PCI operation

PCI Interrupts

Interrupt	Function
INTA_L	CF Socket A interrupt
INTB_L	CF Socket B interrupt
INTC_L	Unused
INTD_L	Unused

HyperTransport Connectivity

FP

Bus	Width	Connection	Description
HT0	16	HT21000	
HT1	8	Expansion connector	
HT2	16	TXRX HT2	

TXRX

Bus	Width	Connection	Description
HT0	8	Expansion connector	
HT1	n/a	Unused	
HT2	16	TXRX HT2	

HT21000

Bus	Width	Connection	Description
HT0	16	FP HT0	HT-to-PCIe bridge
HT1	n/a	Unused	

HyperTransport ID

Device	ID
TXRX / FP Primary	0014166d
TXRX / FP Port	0011166d
HT21000 EXB0	01401166
HT21000 EXB1	01421166
HT21000 EXB2	01441166
HT21000 EXB3	01421166
HT21000 EXB4	01421166

HyperTransport Configuration

TXRX

Device	Bus	Device	Notes
Primary Bus (0)			
TXRX Primary Bridge	0	4	
TXRX HT Port 0 Bridge	0	0	Expansion port
TXRX HT Port 1 Bridge	0	1	Unused
TXRX HT Port 2 Bridge	0	2	Connects to FP
Secondary Bus (1)			
FP HT Port 2 Bridge	1	3	
Secondary Bus (2)			
FP Primary Bridge	2	4	

FP

Device	Bus	Device	Notes
Primary Bus (0)			
FP Primary Bridge	0	4	
FP HT Port 0 Bridge	0	0	Connects to HT21000
FP HT Port 1 Bridge	0	1	Unused
FP HT Port 2 Bridge	0	2	Connects to TXRX
Secondary Bus (5)			
HT21000 EXB0	5	0	PCI-e Bridge to LAN expansion
HT21000 EXB1	5	1	PCI-e Bridge to Qlogic ports 0 and 1
HT21000 EXB2	5	2	PCI-e Bridge to Qlogic ports 2 and 3
HT21000 EXB3	5	3	PCI-e Bridge to SAN expansion
HT21000 EXB4	5	4	PCI-e Bridge to SAN expansion

PCI-e Hardware Configuration

HT21000	Lanes	Connection	Notes
A_PCIE_[7:0]	8	Expansion	Hooks to left midplane connectors
A_PCIE_[11:8]	4	QLogic EP2432	FC ports 0 and 1 on main board
A_PCIE_[15:12]	4	QLogic EP2432	FC ports 2 and 3 on main board
B_PCIE_[3:0]	4	Expansion	Hooks to right midplane connectors
B_PCIE_[7:4]	4	Expansion	Hooks to right midplane connectors

PCI-e Memory Map

Physical Address	Size	Function	Notes
00.0000.0000	16MB	QLogic port 0	HT21000 EXB1 passes 0000.0000 - f0.0200.0000
00.0100.0000	16MB	QLogic port 1	
00.0200.0000	16MB	QLogic port 2	HT21000 EXB2 passes 0000.0000 - f0.0400.0000
00.0300.0000	16MB	QLogic port 3	
50.0000.0000	64GB	FP Memory	FP HT0 bridge passes to memory controller

PCI-e ID

Device	ID
QLogic EP2432	64321077

PCI-e Configuration

Device	Bus	Device	Notes
Secondary Bus (6)			
QLogic EP2432	6	0	Port 0 is function 0, port 1 is function 1
Secondary Bus (7)			
QLogic EP2432	7	0	Port 0 is function 0, port 1 is function 1
Secondary Bus (8)			
Expansion	8	0	
Secondary Bus (9)			
Expansion	9	0	
Secondary Bus (10)			
Expansion	10	0	

HT21000 Reset Init

Signal	Value	Settings
STRP_BCN_EN	0	Must be pulled down
STRP_DBG_32	open	
STRP_HOT_PLUG	0	Must be pulled down
STRP_HT_16X	open	
STRP_HT_BERT	open	
STRP_HT_FREQ[2:0]	open	
STRP_HT_LPBK	open	
STRP_I2C_ADDR	open	I2C address = 0xC8
STRP_PCIE_A[1:0]	1,0	A_PCI-e is 8x,4x,4x
STRP_PCIE_B[1:0]	1,0	B_PCI-e is 4x,4x
STRP_PLL_PWRD	open	
TEST_MODE_EN	0	Must be pulled down
TEST_MODE[7:4]	0,0,0,0	Must be pulled down
TEST_MODE[3:0]	open	
TEST_MODE8	open	
TEST[3:0]	00100	Must be pulled down

All signals listed above can be pulled up or down

BM-FPGA Address Map

Register	Offset
Board Status	0x000
GPP	0x004
LED Control	0x008
Test Register	0x00c
SSC/TXRX Control	0x010
SSC/TXRX Control (Expansion)	0x014
SSC/TXRX Status	0x018
SSC/TXRX Status (Expansion)	0x01c
SSC/TXRX Power Usage Out	0x020
SSC/TXRX Power Usage In	0x024
SSC/TXRX Mailbox Message Out	0x028
SSC/TXRX Mailbox Message In	0x02c
SSC/FP Control	0x030
SSC/FP Control (Expansion)	0x034
SSC/FP Status	0x038
SSC/FP Status (Expansion)	0x03c
SSC/FP Power Usage	0x040
SSC/FP Power Usage In	0x044
SSC/FP Mailbox Message Out	0x048
SSC/FP Mailbox Message In	0x04c
TXRX/SSC Control	0x050
TXRX/SSC Control (Expansion)	0x054
TXRX/SSC Status	0x058
TXRX/SSC Status (Expansion)	0x05c
TXRX/SSC Power Usage	0x060
TXRX/SSC Power Usage In	0x064
TXRX/SSC Mailbox Message Out	0x068
TXRX/SSC Mailbox Message In	0x06c
FP/SSC Control	0x070
FP/SSC Control (Expansion)	0x074
FP/SSC Status	0x078
FP/SSC Status (Expansion)	0x07c
FP/SSC Power Usage	0x080
FP/SSC Power Usage In	0x084
FP/SSC Mailbox Message Out	0x088
FP/SSC Mailbox Message In	0x08c

Board Status Register (RO)

Bit	Definition	Notes
0	Diag Select (0 = normal, 1 = diags)	
1	Prom Select (0 = normal, 1 = recovery)	
2	Slot ID (0 = top, 1 = bottom)	
3	Backplane ID (0 = expansion, 1 = low cost)	
4	TXRX Status Interrupt	
5	TXRX Message Interrupt	
6	FP Status Interrupt	
7	FP Message Interrupt	
8	Temperature status (0 = temp ok, 1 = temp above threshold)	If status = 1, SSC is interrupted via status interrupt (1125 GPIO bit 12)
9	Temperature status (0 = temp ok, 1 = temp above threshold)	If status = 1, SSC is interrupted via status interrupt (1125 GPIO bit 12)
10	Fan Status (0 = fan problem, 1 = all fans ok)	If fan status = 0, SSC is interrupted via status interrupt (1125 GPIO bit 12); chassis manager polls each fan controller via I2C to mezzanine board
11	PCI system error (0 = ok, 1 = error)	
12	PS0 OK (0 = error, 1 = ok)	If status = 0 on any of the power supply signals, SSC is interrupted via status interrupt (1125 GPIO bit 12)
13	PS0 Alert (0 = error, 1 = ok)	
14	PS1 OK (0 = error, 1 = ok)	
15	PS1 Alert (0 = error, 1 = ok)	
17:16	Cluster_in	0,1 = primary, present
	(hardware controlled)	1,1 = secondary, present
		x,0 = other board not present or down
19:18	Cluster_out	0,1 = primary, present
	(hardware controlled)	1,1 = secondary, present
		x,0 = other board not present or down
20	Cluster state (0 = secondary, 1 = primary)	Hardware controlled
23:21	Reserved (read as 0)	
31:24	BM-FPGA version	

General Purpose Register (RW)

Bit	Definition	Notes
0	TXRX Cold Reset (1 = reset)	Default to 1
1	TXRX Warm Reset (1 = reset)	Default to 1
2	FP Cold Reset (1 = reset)	Default to 1
3	FP Warm Reset (1 = reset)	Default to 1
4	HT21000 Reset (1 = reset)	Default to 1
5	HT21000 Power OK (0 = power ok)	Default to 1
6	HT21000 Power On Rst (1 = reset)	Default to 1
7	GigE Serdes Reset (1 = reset)	Default to 1
8	Mgmt Port PHY Reset (1 = reset)	Default to 1
11:9	Reserved	Default to 1
15:12	GigE Port Enable (1 = enable)	Default to 1, must be set for port LEDs
19:16	FC Port Enable (1 = enable)	Default to 1, must be set for port LEDs
20	Power Supply LED control (0 = hardware, 1 = software)	Defaults to 0, software control for test purposes only
21	Fan LED control (0 = hardware, 1 = software)	Defaults to 0, software control for test purposes only
22	System LED control (0 = hardware, 1 = software)	Defaults to 0, software control for test purposes only
23	Reserved	
24	Boot enable (1 = system booting)	Set by hardware
25	System up (1 = up)	Set by chassis manager
26	Crash enable (1 = enable)	Set by chassis manager
30:27	Reserved	
31	Fan all on (1 = enable)	Set if temperature condition or fan event is seen

LED Register (RW)

Bit	Definition	Notes
1:0	CF Socket A LED	00 = off, 01 = red, 10 = green, 11 = amber
3:2	CF Socket B LED	00 = off, 01 = red, 10 = green, 11 = amber
5:4	Frontpanel Fan LED	00 = off, 01 = green, 10 = red, 11 = off; Fan LED control must be set in GPP register
7:6	Frontpanel PS LED	00 = off, 01 = green, 10 = red, 11 = off; Power Supply LED control must be set in GPP register
9:8	Frontpanel System LED	00 = off, 01 = green, 10 = red, 11 = off; System LED control must be set in GPP register
11:10	Fan Module 0	00 = off, 01 = red
13:12	Fan Module 1	00 = off, 01 = red
15:14	Fan Module 2	00 = off, 01 = red
16	FC LED Sel	Reserved
17	Port LED Test Mode	0 = disabled, 1 = enabled
18	PS0 enable (0 = off, 1 = on)	Reserved
19	PS1 enable (0 = off, 1 = on)	Reserved
20	LED enable (1 = enable)	Must be primary SSC to control system LEDs
21	LED blink enable	Blink system, PS, and fan LEDs
22	FC LED Invert	Reserved
23	GigE LED Invert	Reserved
31:24	Port LED Test Pattern	Used when LED Test Mode is enabled

BM-FPGA Register Routing

CPU	Register Written	CPU	Register Read	Notes
SSC	SSC/TXRX Control	TXRX	TXRX/SSC Status	
SSC	SSC/TXRX Control (Expansion)	TXRX	TXRX/SSC Status (Expansion)	Not currently implemented
SSC	SSC/TXRX Power Usage Out	TXRX	TXRX/SSC Power Usage In	Not currently implemented
SSC	SSC/TXRX Mailbox Message Out	TXRX	TXRX/SSC Mailbox Message In	
SSC	SSC/FP Control	FP	FP/SSC Status	
SSC	SSC/FP Control (Expansion)	FP	FP/SSC Status (Expansion)	Not currently implemented
SSC	SSC/FP Power Usage Out	FP	FP/SSC Power Usage In	Not currently implemented
SSC	SSC/FP Mailbox Message Out	FP	FP/SSC Mailbox Message In	
TXRX	TXRX/SSC Control	SSC	SSC/TXRX Status	
TXRX	TXRX/SSC Control (Expansion)	SSC	SSC/TXRX Status (Expansion)	Not currently implemented
TXRX	TXRX/SSC Power Usage Out	SSC	SSC/TXRX Power Usage In	Not currently implemented
TXRX	TXRX/SSC Mailbox Message Out	SSC	SSC/TXRX Mailbox Message In	
FP	FP/SSC Control	SSC	SSC/FP Status	
FP	FP/SSC Control (Expansion)	SSC	SSC/FP Status (Expansion)	Not currently implemented
FP	FP/SSC Power Usage Out	SSC	SSC/FP Power Usage In	Not currently implemented
FP	FP/SSC Mailbox Message Out	SSC	SSC/FP Mailbox Message In	

SSC I2C Addresses

Device	I2C #0	I2C #1	Notes
Board SEEP	1010000		Board parameters and info
DIMM Socket SEEP	1010100		1125 memory parameters
Temperature Sensor	1001101		Board temperature
Temperature Sensor	1001110		Board temperature (exhaust)
FP Temp Sensor	0011010		Depopulated
TXRX Temp Sensor	0011011		Depopulated
Mezzanine I2C Mux		1111000	
Mezzanine I2C Fan Controller Mux		1110000	
Fan Controller 0, 2, 4		1001000	Located behind I2C Fan Controller Mux
Fan Controller 1, 3, 5		1001011	Located behind I2C Fan Controller Mux
Mezzanine RTC		11010xx	See DS1388 spec for addressing info
Mezzanine SEEP		1010000	change to 1010111
PS0		1010000	
PS0		1011000	
PS1		1010010	
PS1		1011010	

SSC MDIO Addresses

Device	Address	Master
Frontpanel PHY0	00001	1125 MDIO registers for Ethernet 0
Frontpanel PHY1	00010	1125 MDIO registers for Ethernet 1

TXRX I2C Addresses

Device	I2C #0	I2C #1	Notes
Board SEEP	1010000		Board parameters and info
DIMM Socket SEEP J3102	1010100		1125 memory parameters
DIMM Socket SEEP J3101	1010101		1125 memory parameters
DIMM Socket SEEP J3301	1010110		1125 memory parameters
DIMM Socket SEEP J3302	1010111		1125 memory parameters
SFP Mux		1110000	SFP identification

TXRX MDIO Addresses

Device	Address	Master
Frontpanel SERDES Port 0	00100	1480 MDIO registers for Ethernet 0
Frontpanel SERDES Port 1	00101	1480 MDIO registers for Ethernet 1
Frontpanel SERDES Port 2	00110	1480 MDIO registers for Ethernet 2
Frontpanel SERDES Port 3	00111	1480 MDIO registers for Ethernet 3

FP I2C Addresses

Device	I2C #0	I2C #1	Notes
Board SEEP	1010000		Board parameters and info
DIMM Socket SEEP J3102	1010100		1125 memory parameters
DIMM Socket SEEP J3101	1010101		1125 memory parameters
DIMM Socket SEEP J3301	1010110		1125 memory parameters
DIMM Socket SEEP J3302	1010111		1125 memory parameters
SFP Mux (expansion)		1110000	SFP identification

FP MDIO Addresses

Device	Address	Master
Frontpanel SERDES Port 0	00100	1480 MDIO registers for Ethernet 0
Frontpanel SERDES Port 1	00101	1480 MDIO registers for Ethernet 1
Frontpanel SERDES Port 2	00110	1480 MDIO registers for Ethernet 2
Frontpanel SERDES Port 3	00111	1480 MDIO registers for Ethernet 3

Board Configuration Jumpers

Jumper	Description	Pos 1-2	Pos 2-3
J6007	Prom Select	*Normal*	Recovery
J6008	Diagnostics mode	*Normal*	Diagnostics
J7903	BM-FPGA config	*Normal*	Disable init
J7904	JTAG Enable	JTAG	*Normal*
J7905	Corelis Select	*Normal*	Corelis

Default setting is in italics

Debug headers

Header	Description	Location
J1501	FP Core 0	Back right
J1502	FP Core 1	Back right
J1503	FP Core 2	Back right
J1504	FP Core 3	Back right
J1601	FP Corelis	Middle right
J3401	TXRX Core 0	Middle left
J3402	TXRX Core 1	Middle left
J3403	TXRX Core 2	Middle middle
J3404	TXRX Core 3	Middle middle
J3501	TXRX Corelis	Middle left
J4201	SSC Corelis	Front left
J4503	SSC Core 0 DB9	Front right
J4504	SSC Core 0	Front middle
J4505	SSC Debug	Front middle
J6002	Xilinx PROM config	Front left

Board LEDs

LED	Behavior	Notes
GigE Port LED	Green = link up	LED is under hardware control; port enable is under software control via BM-FPGA GPP register
	Flashing Green = activity	
	Amber = port enabled, link down	
	Off = port disabled	
FC Port LED	Green = link up	LED is under Qlogic firmware control; port enable is under software control via BM-FPGA GPP register
	Flashing Green = activity	
	Amber = port enabled, link down	
	Off = port disabled	
System LED	Flashing green = system booting	Flashing green is under hardware control; chassis manager sets 'system_up' bit in GPP register when all processors are up and 'crash_enable' bit in GPP register if one or more processors is not up
	Green = all processors up in runtime	
	Red = not all processors up in runtime	
Power Supply LED	Green = both supplies ok	LED is under hardware control; if supply is bad, BM-FPGA will assert status interrupt to SSC; chassis manager then polls BM-FPGA status register to determine which supply is bad; chassis manager may also poll PS0 and PS1 via i2c for more information
	Red = one supply not up	
Fan LED	Green = all fans at normal speed	LED is under hardware control; if one or more fans has locked rotor, BM-FPGA will assert status interrupt to SSC; chassis manager then polls BM-FPGA status register to determine that a fan has a locked rotor and/or temperature condition exists; if a fan has a locked rotor, then chassis manager polls fan controllers to determine which fan is bad; chassis manager then drives the appropriate fan system LED (see below) via BM-FPGA LED register to indicate which fan module to replace
	Red = one or more fans have locked rotor and/or fans at full speed due to temperature condition	

Compact Flash	Green = ok to eject	LED is under software control via BM-FPGA LED register
	Amber = active, do not eject	

System LEDs

The System LEDs may only be driven by one motherboard. This is determined by a hardware handshake that is part of the BM-FPGA.

LED	Behavior	Notes
Frontpanel System LED	Flashing green = system booting	Flashing green is under hardware control; chassis manager sets 'system_up' bit in GPP register when all processors are up and 'crash_enable' bit in GPP register if one or more processors is not up; this LED will go green when the controlling motherboard has all processors up; this LED will go red if any processor (including the non-controlling motherboard) is down
	Green = all processors up in runtime	
	Red = not all processors up in runtime	
Frontpanel Power Supply LED	Green = both supplies ok	LED is under hardware control; if supply is bad, BM-FPGA will assert status interrupt to SSC; chassis manager then polls BM-FPGA status register to determine which supply is bad; chassis manager may also poll PS0 and PS1 via I2c for more information
	Red = one supply not up	

Frontpanel Fan LED	Green = all fans at normal speed	LED is under hardware control; if one or more fans has locked rotor, BM-FPGA will assert status interrupt to SSC; chassis manager then polls BM-FPGA status register to determine that a fan has a locked rotor and/or temperature condition exists; if a fan has a locked rotor, then chassis manager polls fan controllers to determine which fan is bad; chassis manager then drives the appropriate fan system LED (see below) via BM-FPGA LED register to indicate which fan module to replace
	Red = one or more fans have locked rotor and/or fans at full speed due to temperature condition	
Fan Module LEDs	Off = fan module OK	Chassis manager drives the fan module LED as defined in the BM-FPGA LED register
	Red = locked rotor with one of both fans	
Backlit Logo	On when 12V present from at least one of the power supplies	