RM9220, RM9222, RM9224
RM9120, RM9122, RM9124

Reference Board

Specifications

Issue No. 1: May 2004

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Definitions

Term	Definition
2BI	Two-bit Interface
Bridal Veil	Daughter Card for the RM9x20 Devices
CPLD	Complex Programmable Logic Device
DDR	Dual Data Rate
DIMM	Dual Inline Memory Module
DUART	Dual UART
DUT	Device Under Test
ECC	Error Correction Code
EEPROM	Electronically Erasable Programmable Read Only Memory
EJTAG	Enhanced Joint Test Action Group
FPGA	Field Programmable Gate Array
GE MAC	Gigabit Ethernet Media Access Controller
GPI	Generic Packet Interface
Half Dome	Daughter Card for the RM9x24 Devices
HT	HyperTransport
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
Mariposa	Daughter Card for the RM9x22 Devices
MDIO	MII Data Input/Output
NVRAM	Nonvolatile Random Access Memory
PMON	Performance Monitor
SEEP	Serial EEPROM
SRAM	Synchronous RAM
UART	Universal Asynchronous Receiver/Transmitter
Yosemite	Main Reference Board

1 Overview

1.1 Scope

This document provides information about the reference boards for the dual core RM922x and the single core RM912x RM9000x2GL microprocessors.

This document provides an overview and the jumper settings for the:

- Yosemite (main board).
- Half Dome (daughter card for the RM9224/RM9124 microprocessors).
- Mariposa (daughter card for the RM9222/RM9122 microprocessors).
- Bridal Veil (daughter card for the RM9220/RM9120 microprocessors).

1.2 Purpose

The Yosemite reference board along with the appropriate daughter card and PMON provides a platform to develop user applications for the RM922x/RM912x products and serves as an evaluation/initial prototyping platform. A Linux port for this board is also available from PMC-Sierra.

1.3 Yosemite Board Features

General features of the Yosemite board are:

- Support for the dual core (RM922x) or single core (RM912x) microprocessors, which contain cache coherent MIPS-based™ CPUs, are compatible with the MIPS IV instruction set, and operate up to 1.0 GHz. Each microprocessor supports a separate processor daughter card: Half Dome (RM9224), Mariposa (RM9222), and Bridal Veil (RM9220).
- Standard ATX form factor.
- One of two jumper-selectable Flash devices:
  - Socketed (32-pin PLCC) AMD AM29F040B (4 Mbits).
  - AMD AM29F160B (16 Mbits).
- Single-chip Watch Dog timer and Real Time Clock (STMicroelectronics M48T37Y) with 32 Kbytes of NVRAM.
- Three Gigabit Ethernet RJ-45 ports (10/100/1000BaseT) using the microprocessor's GE MAC interface.
- Three 32-bit 33/66 MHz PCI slots. (Two PCI slots are 3.3 V and one is 5 V.)
- Support for HyperTransport mezzanine cards via two different HyperTransport connectors:
  - 160-pin HyperTransport committee standard connector.
  - 80-pin HyperTransport connector (compatible with the RM9000x2 Jaguar reference board).

- Two RS-232 communication ports driven by microprocessor's native serial ports or an external DUART (SC16C2552IA44) through the local bus. Uses a null modem cable to connect to a PC.
- EJTAG emulator access to the microprocessor.
- Support for alternate mode bits via an FPGA (not implemented yet).
- Power good and reset LED indicators.
- Two user-controlled LED indicators.
- GE Port LEDs for 10/100/1000 activity and link status indication.
- Power and Reset pushbuttons:
  - The power pushbutton is compatible with remote power control.
- Microprocessor temperature sensor pins supported by the Maxim MAX1619 chip.
- PMON boot firmware and Linux operating systems.

1.4 Daughter Card Features

The key features of the Half Dome, Mariposa, and Bridal Veil daughter cards are:

- Support for two registered or unbuffered DDR SDRAM DIMMs (with ECC) up to 1 Gbyte each.
- Dual footprint for clock generation and support for PMC-Sierra or ICS clock devices.
- Serial EEPROM for mode bits.
- Support for a 64-bit SysAD bus, if enabled, using a SysAD connector. Appropriate optional SysAD module must be provided.
- Configurable master clock frequency in the ~100 to 200 MHz range.

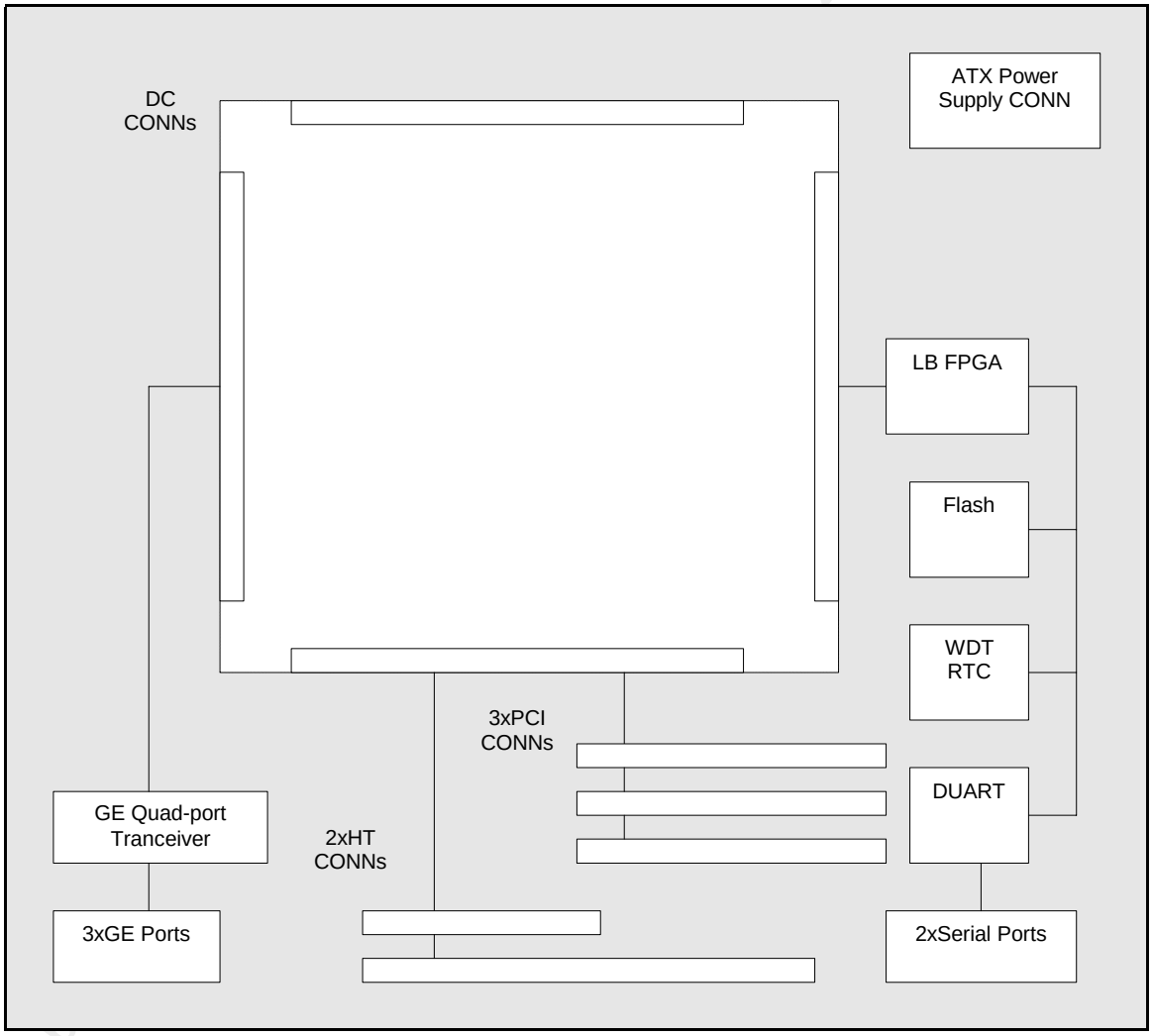
For additional details on specific daughter cards, please refer to the appropriate section in this document.

2 Functional Description (Yosemite)

2.1 Block Diagrams

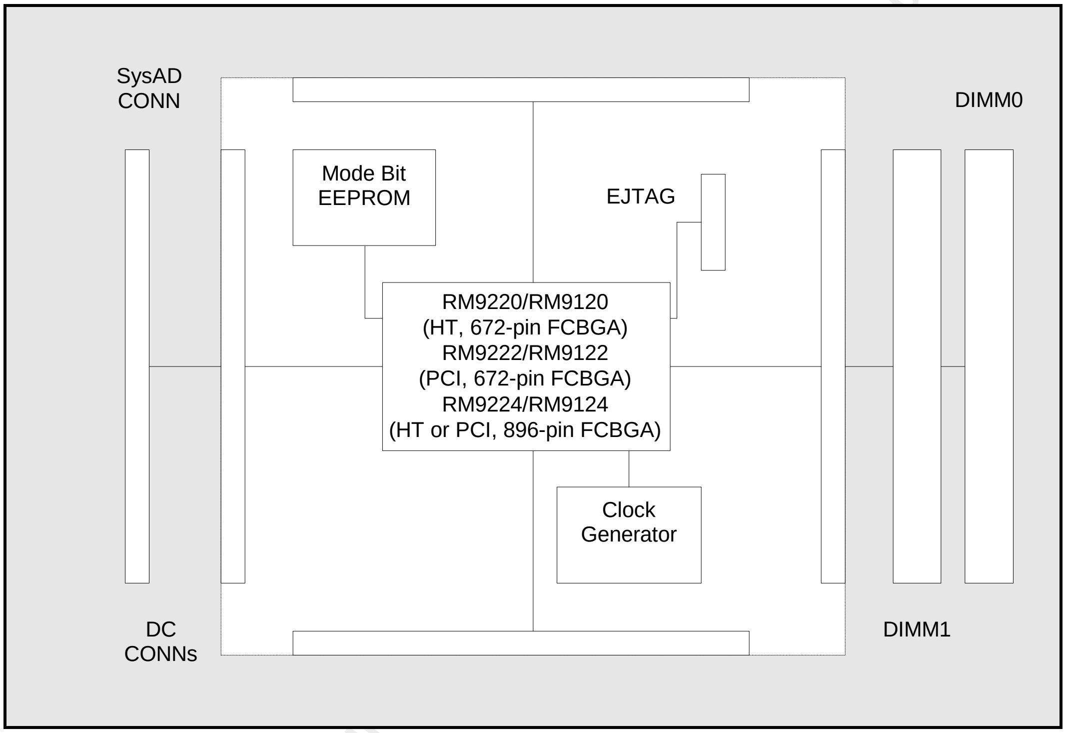
Figure 1 shows the major elements of the Yosemite reference board.

Figure 1 RM922x/RM912x Yosemite Main Board



The daughter card block diagram is shown in Figure 2.

Figure 2 RM922x/RM912x Processor Daughter Cards for Yosemite



2.2 HyperTransport Interface

The RM922x/RM912x Yosemite board uses one HyperTransport-standard connector (Samtec 160-pin QSE-080-01-F-D-A Male connector), and one non-standard HyperTransport connector (Samtec 80-pin QSE-040-01-F-D-A-K). All HyperTransport CAD, clock, and control signals for an 8-bit interface are provided via these connectors.

The connectors also provide 3.3 V DC voltage. The maximum current supported by the connector depends on the capacity of the externally connected supply (typically an ATX style power supply).

2.3 PCI Interface

The Yosemite has three 32 bit 33/66 MHz PCI slots (two 3.3 V and one 5 V). The mapping of the IDSEL and REQ#/GNT# lines is as shown Table 1.

Table 1 PCI Device Mapping

PCI Device	REQ#/GNT# Pair	IDSEL
RM922x/RM912x	0	AD17
Slot 1	1	AD18
Slot 2	2	AD19
Slot 3	0	AD20

The PCI interrupt signals from slot 1 (3.3 V, J12), slot 2 (3.3 V, J13), and slot 3 (5 V, J23) are tied to the microprocessor's INTB0, INTB1 and INTB2 interrupt pins respectively. The DUART interrupt and 5 V PCI interrupt signals share the INTB2 pin. See Section 4 for switch and jumper descriptions.

The PCI interface will automatically operate at 33 or 66 MHz depending on the capability of the installed PCI expansion card(s). Installing an R842 card allows the user to restrict the PCI bus frequency to 33 MHz.

2.4 Local Bus Interface

An FPGA provides the interface between the microprocessor's local bus and various peripheral devices including SRAM, Flash, a watchdog timer, an off-board LCD display, the Reset Control CPLD, and a DUART. The local bus operates at 16 MHz and supports parity.

2.5 Gigabit Ethernet Ports

The main board supports three 10/100/1000BaseT Gigabit Ethernet ports. The microprocessor's GMII is connected to the Marvell Alaska Quad-Port 88E1041 transceiver.

2.6 2BI/MDIO and UART Interfaces

The two 2BI/MDIO interfaces provided on the microprocessors are connected as follows:

- The first interface (configured as MDIO) is connected to the Ethernet PHY device's MDIO port.
- The second interface (configured as 2BI) is connected to a serial EEPROM AT24C64, a temperature sensor MAX1619, and the two DDR DIMM devices on the daughter card. The address assignment of the devices is as shown Table 2.

Table 2 2BI Address Assignment

2BI Address	Device Accessed	Notes
0 0 0	DIMM 0	Farthest from CPU
0 0 1	DIMM 1	
X 1 0	MAX1619	JP33: Installed, JP34 Open

2BI Address	Device Accessed	Notes
1 1 1	AT24C64	JP35: Open, JP36: Open, JP37: Open
1 0 0	Reserved	
1 0 1	Reserved	
X 1 0	Image of MAX1619	
1 1 1	Reserved	

The microprocessor's UART interfaces are routed to RS-232 transceivers. Either the internal UART or the external UART can be used depending on the resistor stuffing option on the Yosemite board.

2.7 LCD Readout

An optional external LCD display can be connected to the Yosemite board using a flat ribbon cable.

2.8 Debug Interface

EJTAG interface connectivity to the microprocessor is provided via a header.

2.9 Reset and Power Monitor

A power monitoring circuit provides under-voltage lockout protection. This circuit, in conjunction with the Reset Control CPLD, provides the necessary reset signals to the microprocessor and other Yosemite components. Both hard S1 and soft S3 resets are provided.

Note: It is advisable to use only the hard reset switch, S1. In future board assemblies, S3 will be designated "Do Not Install".

2.10 Interrupt Signals

The microprocessors support 10 interrupt signals, INTB00 through INTB09, as well as a non-maskable interrupt (NMI). Table 3 shows the board's interrupt routing, which is dependent on the selected mode and jumper setting.

Table 3 Interrupt Routing

Interrupt	JP26 (1,2) SysAD Bus	JP26 (2,3) Main Board and SysAD Bus	
INTB00	SAD_INTB0	PCI_INTAB	
INTB01	SAD_INTB1	PCI_INTBB	
INTB02	SAD_INTB2	**JP45 (1,2)** PCI_INTCB	**JP45 (2,3)** DUARTINTN
INTB03	SAD_INTB3	SAD_INTB3	
INTB04	SAD_INTB4	SAD_INTB4	
INTB05	SAD_INTB5	PROC_PCI_INTB	
INTB06	SAD_INTB6	PHY0_nINT	

Interrupt	JP26 (1,2) SysAD Bus	JP26 (2,3) Main Board and SysAD Bus
INTB07	SAD_INTB7	PHY1_nINT
INTB08	SAD_INTB8	PHY2_nINT
INTB09	SAD_INTB9	SAD_INTB9
NMINTB	SAD_ NMINTB	SAD_ NMINTB

2.11 Miscellaneous Interfaces

The Yosemite board provides 12 V JP1 and 5 V JP2 fan connection headers, and a connection for the microprocessor's BASEN and EMITTERP signals, which are used for remote on-chip diode temperature sensing.

2.12 Clock Distribution

The clock generation for the Yosemite and the associated daughter card assembly is largely implemented on the daughter card. The clock generation logic for each daughter card is identical. For clarity, all clock descriptions are documented in this section of the document.

The complete (main board and daughter card) clock logic block diagram is shown in Figure 3. The boundaries between the main board and the daughter card clock logic are also shown in the block diagram.

The clock generation complex outputs the following clocks:

- CPU master clock: MCLK/MCLKB.
- Ethernet/GPI reference clock: EREFCLK.
- GPI-16 reference clock: PREFCLK.
- HyperTransport clock: HTCLK/HTCLKB.
- PCI-33/66 clock: PCI_CLK_RM9K and PCI_CLK_S#.
- PLX HyperTransport daughter card reference clock: HT_REF_CLK_66M.
- SysAD clock: SyAD_CLK.
- SysAD PCI-33 clock: SysAD_PCI_33M.
- SysAD SDRAM clock: SysAD_SDRAM_66M.

2.12.1 Daughter Card Clock Generation

The Ethernet/GPI reference clock and GPI-16 reference clock are derived from their respective independent oscillators.

Two clock generation options are provided to generate the CPU master clock, the CPU HyperTransport clock, the PLX HyperTransport clock, and the single-ended SysAD clock. The recommended solution is the PMC-Sierra CM5391L Gen-M9K-20 and CM5371 Gen-M7K-20 Flexible Clock Generators, as this solution provides reduced component count, space, and power savings over the other possible implementation. Only one of these options should be used at any time:

- Primary Solution: PMC-Sierra's CM5391L GEN-M9K-20 and CM5371 GEN-M7K-20 Flexible Clock Generator solution tailored for PMC-Sierra MIPS-based processor applications.
- Secondary Solution: ICS8624/CY7C9440V.

Primary Solution: CM5391L Gen-M9K-20 and CM5371 Gen-M7K-20

A 25 MHz single-ended clock source drives the CM5391L, which generates a differential clock to drive the CPU master clock, and two single-ended clocks. The single-ended clocks drive the HyperTransport interface (via LVTTL-LVDS conversion) and the SysAD clock. These three in-phase clocks can range from 50 to 200 MHz at eight specific frequencies. The synchronous PLX HyperTransport daughter card reference clock is derived from a CM5371 device that in turn is driven by the same 25 MHz clock source.

Secondary Solution: ICS8624/CY7C9440V

A 33 MHz crystal oscillator drives the CY7C9440V device, which generates three single-ended clocks. The single ended clocks drive the CPU master clock via ICS8624 LVTTL-HSTL conversion, the HyperTransport interface (via LVTTL-LVDS conversion) and the SysAD clockThese three in-phase clocks can range from 33 to 198 MHz in increments of 33 MHz. The synchronous PLX HyperTransport daughter card reference clock is derived from the same 33 MHz source using a CY2308SC-2 device.

2.12.2 Main Board Clock Generation

A 33 MHz clock source is used to generate the PCI-33 clock (33 MHz) tied to SysAD connector and the SDRAM clock (66 MHz) tied to SDRAM clock, which is fixed in frequency. The PCI-33/66 clock driven to the microprocessor and the PCI connectors can either be 33 MHz or 66 MHz depending on the frequency select control signal from the PCI connector.

The 25 MHz clock required by the Ethernet device, the Marvell Alaska Quad-Port 88E1041 transceiver, is derived from an independent oscillator.

2.12.3 Clock Distribution

The generated clocks are distributed on the daughter card or the main board as described below.

The following clocks are input to the microprocessor: the CPU master clock, the Ethernet/GPI reference clock, the HyperTransport clock, the GPI-16 reference clock, and the PCI-33/66 clock. The microprocessor drives the local bus clock, the DDR SDRAM clock, and the HyperTransport transmit and receive clocks.

The PLX HyperTransport daughter card reference clock is tied to the HyperTransport daughter card connector. The PLX HyperTransport daughter card reference clock must be between 55.6 to 66.7 MHz, synchronous with the CPU master clock.

The following clocks are tied to the SysAD connector: the SysAD clock, the PCI-33 clock, and the SDRAM clock.

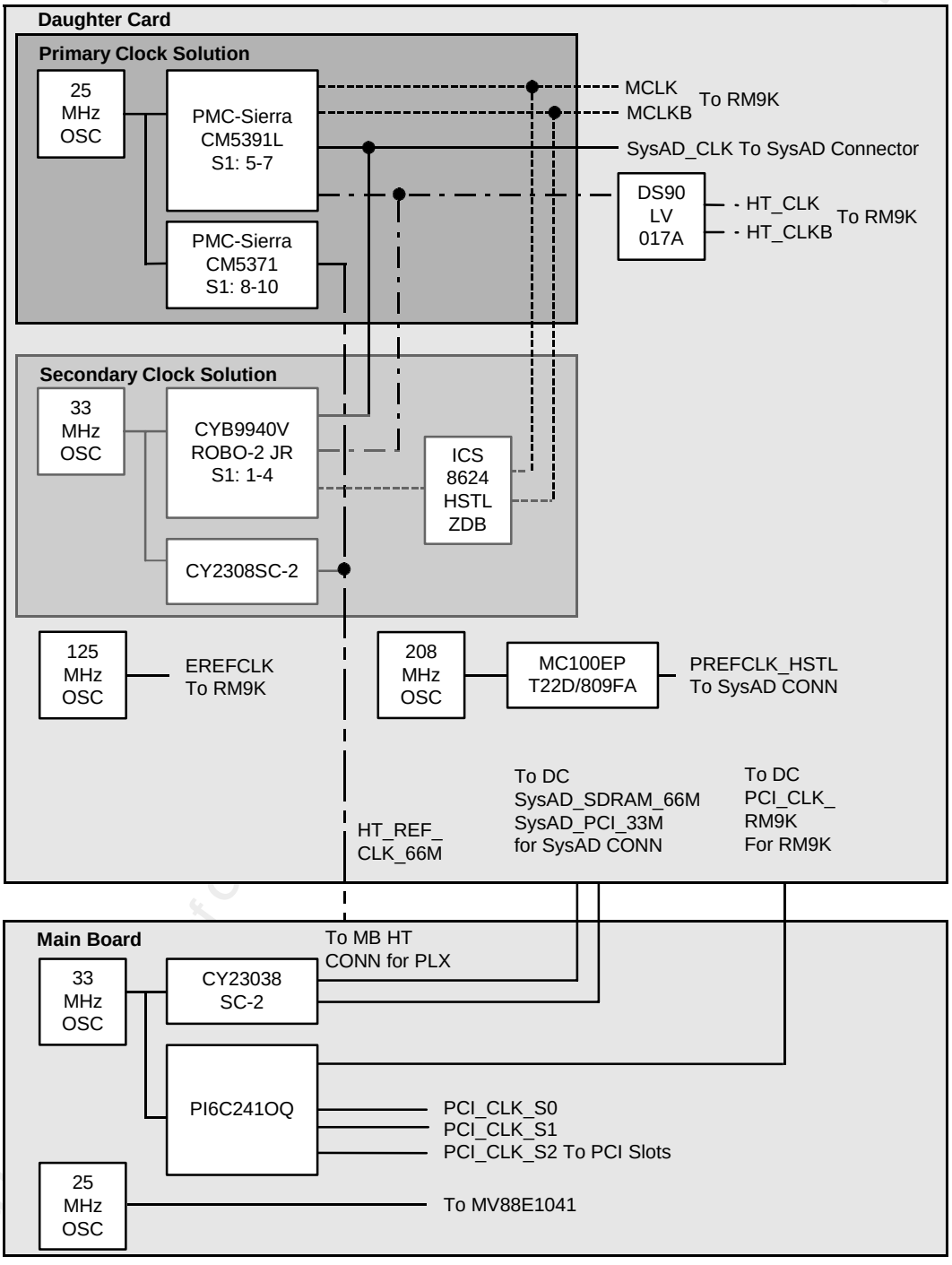
Table 4 summarizes the clocks. Figure 3 shows a block diagram of the clock generation complex.

Table 4 Clocks

Name	Frequency	Logic	Impedance	Description
MCLK/ MCLKB	100–200 MHz	LVDS/ HSTL/ LV PECL (2.5V)/ X1	50 Ω	Master clock input to the microprocessor. Sourced from a PLL frequency generator and routed to the microprocessor's MASTERCLOCK/MASTERCLOCKB inputs.
EREFCLK	125 MHz	LVTTL	50 Ω	Ethernet reference clock. Routed to the microprocessor's EREFCLK input.
PREFCLK	208 MHz	LVTTL/ HSTL	50 Ω	Protocol reference clock. Routed to the microprocessor's PREFCLK input. This clock is 208 MHz and is only used in GPI-16 mode.
HTCLOCK/ HTCLOCKB	100 MHz	LVDS	100 Ω	HyperTransport reference clock. Sourced from a PLL Zero-Delay Buffer/Multiplier and routed to the microprocessor's HTCLOCK/HTCLOCKB inputs.
PCI_CLK	33/66 MHz	LVTTL	50 Ω	PCI Clock: A 33 or 66 MHz PCI clock is routed to the microprocessor's and to each of the PCI slots.
LBCLK	16 MHz	LVTTL	50 Ω	Local Bus Clock: The clock for the microprocessor's local bus. Used to clock the boot-mode configuration serial EEPROM. It is sourced by the microprocessor and routed to the boot mode serial EEPROM and the Local Bus control FPGA. A delayed version of this clock generated by the Local Bus control FPGA is routed to the Reset Control CPLD.
ENETCLK	25 MHz	LVTTL	50 Ω	25 MHz clock routed to the Marvell Alaska Quad-Port 88E1041 transceiver.
SysAD_Clk	100–200 MHz	LVTTL	50 Ω	The optional SysAD Daughter Card requires a system clock that is the same frequency as the master clock.

Name	Frequency	Logic	Impedance	Description
SysAD_ SDRAM_ CLK_66M	66 MHz	LVTTL	50 Ω	The optional SysAD Daughter Card requires a 66 MHz clock for SDRAM.
SysAD_PCI _CLK 33M	33 MHz	LVTTL	50 Ω	The optional SysAD Daughter Card requires a 33 MHz clock for PCI slot.

Figure 3 Clock Generation and Distribution



2.13 Power Supply

The Yosemite is powered by an ATX power supply that provides the following voltages:

+12 V
–12 V
+5 V
-5 V
+3.3 V

The microprocessor requires the following voltages:

+3.3V
+2.5 V
+1.25 V
+1.2 V
+0.75 V

Note: The microprocessor's voltages are generated using adjustable voltage regulators with the outputs set to the values shown above as default for shipment.

Other components on the board require the following voltages:

+5.0 V
+3.3 V

2.14 Reset CPLD

The reset logic controls a Reset CPLD, which in turn controls the microprocessor and local bus FPGA resets. The reset logic monitors local power and also supports external hard reset soft reset switches.

A 12-pin JTAG header, JP15, is provided for programming the CPLD if necessary.

2.15 Local Bus FPGA

The local bus control FPGA contains the glue logic necessary to interface the microprocessor to the various local bus peripherals and provides the following functions:

- Multiplexed address/data local bus to de-multiplexed the I/O bus interface logic.
- General purpose I/O.
- Address decode logic.
- Flash CS0, Miscellaneous CS1, DUART and LCD CS2, Watchdog timer and NVRAM CS3.
- Interface to Optrex DMC20481 LCD module.

The FPGA is configured via an on-board serial configuration EEPROM or the MasterBlaster using the provided header, JP18.

2.16 Miscellaneous CPLD

The CPLD provides the following functions:

- Mode bit programming support for the AT7LV65 Serial EEPROM device. Note: This functionality is not implemented.
- A 12-pin header, JP42, for programming the CPLD.

2.17 Board LEDs

Table 5 shows the LEDs provided on the board and their function.

Table 5 LEDs

LEDs	Function
DS1 and DS2	When both LEDs are lit, the Local Bus FPGA programming is complete and normal board function can continue. If either of these LEDs is off, the Local Bus FPGA programming has failed and the board will not function.
DS22	When this LED is lit, the hard reset signal to the microprocessor has been de-asserted. If this LED is off, the hard reset logic has not completed the reset sequence and the board will not function.
DS23	When this LED is lit, the power is on. This LED is located on the solder side of the board.
DS24	When this LED is lit, the soft reset signal to the microprocessor has been de-asserted. If this LED is off, the soft reset logic has not completed the reset sequence and the board will not function. In future revisions of the board, this LED may not be installed.
DS4-DS9 DS10-DS15 DS16-DS21	Each GE port has a bank of six LEDs that indicate RX, TX, DPLX, Link speed 10, 100, and 1000 status.

3 Daughter Cards

Three different daughter cards provide support for the microprocessors:

- RM9224/RM9124 (896-pin FCBGA package): Half Dome.
- RM9222/RM9122 (672-pin FCBGA package): Mariposa.
- RM9220/RM9120 (672-pin FCBGA package): Bridal Veil.

The following sections describe the three options, which have different interface configurations.

3.1 RM9x24 Half Dome Daughter Card

The RM9x24 microprocessors' SysAD pins are multiplexed with the GE MAC/GPI interface and have different functions depending on the selected operating mode. The RM9x24 microprocessors have 11 different operating modes as shown in Table 6.

Table 6 RM9x24 (HyperTransport, PCI, Local Bus, SysAD, MAC) Configuration

Mode		SysAD	10/100/1000 MAC	GPI-8	GPI-16	GPI-32	UART	2BI	MDIO	HT	PCI
0	SysAD	1	0	0	0	0	0	0	0	1 or 0	0 or 1
1	1xGPI-32 + 1xMAC	0	1	0	0	1	2	1	1	1 or 0	0 or 1
2	2xGPI-16 + 1xMAC[1]	0	1	0	2	0	2	1	1	1 or 0	0 or 1
3	1xGPI-16 + 2xMAC[2]	0	2	0	1	0	2	1	1	1 or 0	0 or 1
4	2xGPI-8 + 1xMAC	0	1	2	0	0	2	1	1	1 or 0	0 or 1
5	3xMAC	0	3	0	0	0	2	1	1	1 or 0	0 or 1
6	1xGPI-8 + 2xMAC	0	2	1	0	0	2	1	1	1 or 0	0 or 1
7	3xGPI-8	0	0	3	0	0	2	1	0	1 or 0	0 or 1
8	2xGPI-16 + 1xGPI-8[1]	0	0	1	2	0	2	1	0	1 or 0	0 or 1
9	1xGPI-32 + 1xGPI-8	0	0	1	0	1	2	1	0	1 or 0	0 or 1
10	1xGPI-16 + 1xGPI-8 + 1xMAC[3]	0	1	1	1	0	2	1	1	1 or 0	0 or 1

Notes

1. The 1xMAC/1xGPI-8 modes operate using LVTTL when the GPI-16 interfaces are HSTL or LVTTL.
2. One MAC interface operates at the same GPI-16 voltage level while the second is always LVTTL.
3. The 1xGPI-8 modes operate at the same GPI-16 voltage level while the 1xMAC is always LVTTL.

The RM9x24 microprocessors are shipped with mode 5 set to operate on the daughter card. To operate the device in another mode, adapter cards are required. Contact PMC-Sierra for details.

3.2 RM9x22 Mariposa Daughter Card

The RM9x22 microprocessors' SysAD pins are multiplexed with the GE MAC/GPI interface and have different functions depending on the selected operating mode. The RM9x22 microprocessors have 6 different operating modes as shown in Table 7.

Table 7 RM9x22 (PCI, Local Bus, 2xMAC) Configuration

Mode		SysAD	10/100/1000 MAC	GPI-8	GPI-16	GPI-32	UART	2BI	MDIO	HT	PCI
0	Reserved	-	-	-	-	-	-	-	-	-	-
1	Reserved	-	-	-	-	-	-	-	-	-	-
2	1xGPI-16	0	0	0	1	0	2	1	0	0	1
3	1xGPI-16	0	0	0	1	0	2	1	0	0	1
4	2xGPI-8	0	0	2	0	0	2	1	0	0	1
5	2xMAC	0	2	0	0	0	2	1	1	0	1
6	1xGPI-8 + 1xMAC	0	1	1	0	0	2	1	1	0	1
7	2xGPI-8	0	0	2	0	0	2	1	0	0	1
8	1xGPI-16	0	0	0	1	0	2	1	0	0	1
9	Reserved	-	-	-	-	-	-	-	-	-	-
10	1xGPI-16	0	0	0	1	0	2	1	0	0	1

The RM9x22 microprocessors are shipped with mode 5 set to operate on the daughter card. To operate the device in another mode, adapter cards are required. Contact PMC-Sierra for details.

3.3 RM9x20 Bridal Veil Daughter Card

Table 8 RM9x20 (HyperTransport, Local Bus, SysAD, 3xMAC) Configuration

Mode		SysAD	10/100/1000 MAC	GPI-8	GPI-16	GPI-32	UART	2BI	MDIO	HT	PCI
0	SysAD	1	0	0	0	0	0	0	0	1	0
1	1xGPI-32	0	0	0	0	1	2	1	0	1	0
2	2xGPI-16	0	0	0	2	0	2	1	0	1	0
3	1xGPI-16 + 1xMAC[1]	0	1	0	1	0	2	1	1	1	0
4	2xGPI-8 + 1xMAC	0	1	2	0	0	2	1	1	1	0
5	3xMAC	0	3	0	0	0	2	1	1	1	0
6	1xGPI-8 + 2xMAC	0	2	1	0	0	2	1	1	1	0
7	3xGPI-8	0	0	3	0	0	2	1	0	1	0
8	2xGPI-16	0	0	0	2	0	2	1	0	1	0
9	1xGPI-32	0	0	0	0	1	2	1	0	1	0
10	1xGPI-16 + 1xGPI-8[1]	0	0	1	1	0	2	1	0	1	0

Note

1. GPI-16 operates in HSTL or LVTTL modes. The 1xMAC/1xGPI-8 interfaces operate at the same voltage as the GPI-16 interface.

The RM9x20 microprocessors are shipped with mode 5 set to operate on the daughter card. To operate the device in another mode, adapter cards are required. Contact PMC-Sierra for details.

3.4 SDRAM

The daughter cards each support two standard DDR DIMM memory modules. Both positions may be populated with registered or unbuffered memory modules. The SDRAM interface to the microprocessors is 64 bits wide and runs up to 200 MHz DDR. For supported SDRAM device densities consult the device documentation.

3.5 Clock Generator

The clock generation for the Yosemite and the associated daughter card assembly is largely implemented on the daughter card. The clock generation logic for each daughter card is identical. See Section 2.12 for complete details.

3.6 Mode Bit CPLD and SEEP

The mode bit logic supports two mode bit streams:

- A hard-coded mode bit stream programmed in the CPLD that will normally not change. (The mode bit pattern can only be changed by reprogramming the CPLD.) It is programmed with a "safe" value that guarantees boot-up.
- A soft-coded mode bit stream programmed in a non-volatile memory location that can be programmed using a mode bit programming utility or under similar program control. (This functionality is not yet implemented.)

3.7 SysAD Interface

A 240-pin SysAD connector is provided on the daughter card. This connector is divided into four parts; the first three parts are compatible with the SysAD connector found on the RM9200 RM9000x2 evaluation board and the other part is used for RM922x/RM912x-specific signals. The following voltages and currents are provided on this connector:

12 V
–12 V
5 V
3.3 V
2.5 V
1.8 V
1.5 V

The maximum current supported by the connector depends on the capacity of the externally connected supply (typically an ATX style power supply).

4 Connectors, Jumpers and Stuffing Option Description

The following sections describe the various connectors, jumpers, and resistor stuffing options. Default settings are indicated with an asterisk (*).

4.1 Jumpers and Switches

For convenience, the main board's schematic sheet on which the specified jumper, etc. appear are also noted in the section headers below. For example, "MB Sh2" refers to the main board (Yosemite) schematic sheet number 2.

4.1.1 JP1: 12 V Fan Connection Header (MB Sh2)

A 12 V fan can be connected to this 2-pin header

4.1.2 JP2: 5 V Fan Connection Header (MB Sh2)

A 5 V fan can be connected to this 2-pin header.

4.1.3 JP3: ATX 5VSB Jumper (MB Sh2)

Use this jumper to draw current from the ATX power supply's 5VSB pin.

JP3	Function
Open	No current drawn from ATX 5VSB pin
Installed	Current drawn from ATX 5VSB pin*

4.1.4 JP4: CPU IO Power Select (MB Sh2)

Use this jumper to select between 1.5 V and 3.3 V for the CPU I/O power.

JP4	Function
1-2	Select 1.5V for CPU IO power (HSTL mode)
2-3	Select 3.3V for CPU IO power (LVTTL mode) *

4.1.5 JP5: SysAD Termination and Reference Voltage Select Jumper (MB Sh3)

Use this jumper to select the SysAD Vtt termination/reference voltage.

JP5	Function
1-2	Termination voltage is 0.75 V*
3-4	Termination voltage is VDDIO/2
5-6	Termination voltage is 1.5 V
7-8	Termination voltage is controlled by potentiometer R24 and is equal to (3.3 x R24 ratio)/2
9-10	Termination voltage is controlled by potentiometer R24 and is equal to 3.3 x R24 ratio
11-12	Regulator is in shutdown

4.1.6 JP6: VREF0, VREFM Source Select Jumper (MB Sh3)

Use this jumper to select the source of the VREF0 and VREFM voltage.

JP6	Function
1-2	VREF0/VREFM are sourced from SysAD_Vtt
2-3	VREF0/VREFM are sourced from VREFOUT output of SysAD_Vtt regulator*

4.1.7 JP7: DDR Termination and Reference Voltage Select Jumper (MB Sh3)

Use this jumper to select the DDR Vtt termination/reference voltage.

JP7	Function
1-2	Termination voltage is 0.75V
3-4	Termination voltage is 1.25V*
5-6	Termination voltage is 1.5V
7-8	Termination voltage is 2.5V
9-10	Termination voltage is controlled by potentiometer R35 and is equal to 3.3 x R35 ratio
11-12	Regulator is in shutdown

4.1.8 JP8: DDR VREF Source Select Jumper (MB Sh3)

Use this jumper to select the source of the DDR memory reference voltage.

JP8	Function
1-2	DDR VREF is sourced from DDR_Vtt
2-3	DDR VREF is sourced from VREFOUT output DDR_Vtt regulator*

4.1.9 JP9: VDDI1.2, VDDHT1.2, VDDHTP1.2 Shutdown Jumper (MB Sh4)

Install this jumper to shut down the regulators supplying the VDDI1.2, VDDHT1.2, and VDDHTP1.2 voltages. This jumper is left open by default.

4.1.10 JP10: EJTAG Reset Control (MB Sh5)

JP10	Function
Open	EJTAG Reset does not cause a hard reset.
Installed	Install this jumper to connect the EJTAG_RESETB pin on the EJTAG header (JP49) to the hard reset circuit*

4.1.11 JP11: Hard Reset Jumper (MB Sh5)

This jumper is tied in parallel with the hard reset switch, S1. It can be tied to a front panel reset switch.

4.1.12 JP12- JP13: FPGA Configuration Jumpers (MB Sh9)

These jumpers set the configuration mode for the local bus control FPGA as indicated in the table below. The associated lines are pulled up (1) when the jumper is open, installing the jumper ties the associated line to ground.

JP12 (MSEL)	JP13 (NCE)	Function
Installed	Installed	Passive serial (MasterBlaster)*
Open	Open	Configuration device configuration scheme

4.1.13 JP15: Reset CPLD Programming Header (MB Sh7)

Connect an Altera MaterBlaster cable to this header to program the Reset CPLD.

4.1.14 JP16: Flash Chip Select (MB Sh8)

Use this jumper to connect the decoded Flash Chip Select to the desired Flash memory.

JP16	Function
1-2	U27 (4 Mb) Chip Select*
2-3	U28 (16 Mb) Chip Select

4.1.15 JP21: CTSTMODEB (MB Sh9)

This jumper is tied to the microprocessor's CTSTMODEB pin.

JP21 (DSCENB)	Function
Open	CTSTMODEB is pulled up to 3.3V *
1-2	CTSTMODEB is driven by the Local Bus Control FPGA's P_ CTSTMODEB output (Functionality not supported in current FPGA)
2-3	CTSTMODEB is grounded

4.1.16 JP22: DTSTMODEB (MB Sh9)

This jumper is tied to the microprocessor's DTSTMODEB pin.

JP22 (DSCENB)	Function
Open	DTSTMODEB is pulled up to 3.3V *
1-2	DTSTMODEB is driven by the Local Bus Control FPGA's P_ DTSTMODEB output (Functionality not supported in current FPGA)
2-3	DTSTMODEB is grounded

4.1.17 JP24: DSCENB (MB Sh9)

This jumper is tied to the microprocessor's DSCENB pin.

JP24 (DSCENB)	Function
Open	DSCENB is pulled up to 3.3V *
1-2	DSCENB is driven by the Local Bus Control FPGA's P_DSCENB output (Functionality not supported in current FPGA)
2-3	DSCENB is grounded

4.1.18 JP25 Interrupt Termination Select (MB Sh10)

Use this jumper to select the interrupt lines' pull-up voltage.

JP25	Function
1-2	Pull-up interrupt lines to 1.5V
3-4	Pull-up interrupt lines to 3.3V *
5-6	Pull-up interrupt lines to SysAD termination voltage (typically 0.75V)

4.1.19 JP26: Interrupt Select Jumper (MB Sh10)

This jumper controls the source of the INTB00 – INTB09 and NMI signals to the microprocessor. Depending on the setting of this jumper, interrupts can be sourced from the:

- SysAD bus connector signals, or
- Main board and a few SysAD bus connector signals.

JP26	Function
1-2	Source of interrupt is the SysAD bus connector
2-3	Source of interrupt is the main board and the SysAD bus connector*

4.1.20 JP28/JP29: LCD Display Connector (MB Sh12)

An Optrex DMC20481LCD module can be connected to this connector. The pinout of this connector is shown below.

Pin	Function
JP28-1	GND
JP28-2	+5 V
JP28-3	Vbias
JP28-4	RS
JP28-5	R/WN
JP28-6	EN
JP28-7	DATA0
JP28-8	DATA1
JP29-1	DATA2
JP29-2	DATA3

Pin	Function
JP29-3	DATA4
JP29-4	DATA5
JP29-5	DATA6
JP29-6	DATA7
JP29-7	BL_POWER
JP29-8	GND

4.1.21 JP32 Serial EEPROM Programming Header (MB Sh13)

The pinout for the serial EEPROM U47 device's programming header is shown below. Note that in the current shipping board, this device is not used since the mode bit functionality is supported on the CPU daughter card using the serial EEPROM device. U14.

Signal	Pin	Pin	Signal
MODEIN	1	2	CEB
CLK	3	4	RESET/OEB
	5	6	
GND	7	8	3.3 V
	9	10	SERENB

4.1.22 JP33 & JP34: MAX1619 Address Select (MB Sh13)

Use these jumpers to set the serial bus address of the MAX1619.

JP33	JP34	Function
Installed	Installed	Address is 0011 000 *
Installed	Open	Address is 1001 100
Open	Installed	Address is 0011 010
Open	Open	Address is 1001 110

4.1.23 JP35, JP36, & JP37: AT24C64 Address Select (MB Sh13)

Use these jumpers to set the serial bus address of the AT24C64.

JP37	JP36	JP35	Function
Installed	Installed	Installed	Address is 1010 000 *
Installed	Installed	Open	Address is 1010 001
Installed	Open	Installed	Address is 1010 010
Installed	Open	Open	Address is 1010 011
Open	Installed	Installed	Address is 1010 100
Open	Installed	Open	Address is 1010 101
Open	Open	Installed	Address is 1010 110
Open	Open	Open	Address is 1010 111

4.1.24 JP42: Miscellaneous CPLD Programming Header (MB Sh14)

Connect an Altera MasterBlaster cable to this header to program the miscellaneous CPLD.

4.1.25 JP45: Interrupt (INTB2) select (MB Sh10)

Use this jumper to select DUART interrupt or 5 V PCI interrupt.

JP45	Function
1-2	5V PCI interrupt is connected to INTB02
2-3	DUART interrupt is connected to INTB02 *

4.1.26 JP47: JTAG Reset Jumper (MB Sh28)

This jumper determines the connection between the COLDRESETB signal and the microprocessor's JTAG reset pin.

JP47	Function
Installed	COLDRESETB is connected to the microprocessor's JTAG reset pin
Open	COLDRESETB is not connected to the microprocessor's JTAG reset pin *

4.1.27 JP48: EJTAG Reset Jumper (MB Sh28)

This jumper determines the connection between the COLDRESETB signal and the microprocessor's EJTAG reset pin.

JP48	Function
Installed	COLDRESETB is connected to the microprocessor's EJTAG reset pin
Open	COLDRESETB is not connected to the microprocessor's EJTAG reset pin *

4.1.28 JP49: EJTAG Header (MB Sh28)

The EJTAG header's pinout is shown below.

Signal	Pin	Pin	Signal
DBRSTB	1	2	GND
DBDI	3	4	GND
DBDO	5	6	GND
DBMS	7	8	GND
DBCK	9	10	GND
RESETB	11	12	GND
	13	14	3.3 V

4.1.29 JP52: JTAG Header (MB Sh28)

The JTAG header's pinout is shown below.

Signal	Pin	Pin	Signal
RSTB	1	2	GND
TDI	3	4	GND
TDO	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
	11	12	GND

4.1.30 S1: Hard Reset Switch (MB Sh5)

Use this switch to cause a hard reset.

4.1.31 S3: Soft Reset Switch (MB Sh6)

Use this switch to cause a soft reset. It is advisable not to use this switch to reset the device (use S1 instead). In future revisions of the board, this switch will be designated 'Do Not Install'.

4.1.32 S5: Miscellaneous Control (MB Sh14)

Use this switch to enable various miscellaneous functions explained in the table below.

S5	Function	
	ON (Low)	OFF (High)
1	Enable Golden mode bits (CPU mode bits applied from U14 on Daughter card) *	Enable User mode bits (CPU mode bits applied from U87) (Function not implemented)
2 (Function not implemented)	Select Little Endian	Select Big Endian
3	Enable Boot Flash Writes (U27, U28) Also see JP16	Disable Boot Flash Writes *
4	User Defined 0	
5	User Defined 1	
6	User Defined 2	
7	User Defined 3	
8, 9, 10	Not used	Not used

4.1.33 R842: PCI M66EN Control (MB Sh25)

Installing this jumper will force the PCI bus to operate at 33 MHz.

R842	Function
Stuff	PCI Bus frequency is restricted to 33 MHz
Do Not Stuff	PCI Bus frequency will be 33 or 66 MHz depending on the installed expansion card(s) *

4.1.34 Ground Connection

TP57, TP58, TP59, TP63, TP64, TP75, TP76, TP77 and TP78 are provided as ground connection.

4.2 Daughter Card Jumpers and Switches

For convenience, the daughter card's schematic sheet on which the specified jumper, etc. appear are noted in the section headers below. For example, DC Sh2, means Daughter Card schematic sheet number 2. In this revision of the document, the DC Sh# references are correct for the Half Dome schematic.

4.2.1 JP3: DDR Reset Jumper (DC Sh13)

This jumper selects the reset source to the DDR modules.

JP3	Function
1-2	DDR module reset is sourced from COLDRESETB*
2-3	DDR module reset is sourced from RESET0B

4.2.2 JP4 & JP5: DDR Module VDDID Select (DC Sh13 and Sh14)

These jumpers select the VDDID for the DDR modules. JP4 corresponds to DDR module 1 and JP5 corresponds to DDR module 0.

JP4/JP5	Function
Install	VDDID is tied to ground
Open	VDDID is unconnected*

4.2.3 JP6: RM9x24 VDDIO_1 Voltage Select (DC Sh17)

Use this Jumper to select the voltage level of the RM9x24's VDDIO_1 pin.

JP6	Function
1-2	VDDIO_1 is at the same voltage as VDDIO*
2-3	VDDIO_1 is tied to 3.3 V

4.2.4 JP7 Mode Bit EEPROM (DC Sh20)

Use this jumper to enable/disable master mode bit.

JP7	Function
Installed	Allow the mode bit load from Serial EEPROM*
Open	Do not allow the mode bit load from Serial EEPROM

4.2.5 S1: Master Clock Setting (DC Sh2)

Use this switch to set the frequency, if the CY7B9940V and ICS8624 devices are stuffed.

S1				Frequency (MHz)
1	2	3	4	
Open	Close	Open	Close	33.000
Open	Close	Close	Close	66.000
Open	Close	Close	Open	99.000*
Close	Close	Open	Close	132.000
Close	Close	Close	Close	165.000
Close	Close	Close	Open	198.000

Use this switch to set the frequency, if the CM5391L device is stuffed.

S1			Frequency (MHz)
5	6	7	
Close	Close	Close	50.000
Open	Close	Close	66.667
Close	Open	Close	83.330
Open	Open	Close	100.000*
Close	Close	Open	125.000
Open	Close	Open	133.000
Close	Open	Open	166.667
Open	Open	Open	200.000

Use this switch to set the frequency, if the CM5371 device is stuffed.

S1			Frequency (MHz)
8	9	10	
Close	Close	Close	50.000
Open	Close	Close	66.667*
Close	Open	Close	83.330
Open	Open	Close	100.000
Close	Close	Open	125.000
Open	Close	Open	133.000
Close	Open	Open	166.667
Open	Open	Open	200.000

4.2.6 SysAD33 Function Select (DC Sh9)

This resistor stuffing option is used to select the function of the microprocessor's SysAD33 pin.

Resistors	Function
Stuff R174 Do Not Stuff R173	SysAD33 pin functions as SysAD33*
Do Stuff R174 Stuff R173	SysAD33 pin functions as PREFCLK (also see section 4.2.7 GPI-16 PREFCLK Select)

4.2.7 GPI-16 PREFCLK Select (DC Sh9)

Use this resistor stuffing option to select HSTL (1.5 V) or LVTTL (3.3 V) mode.

Resistors	Function
Stuff R242 and R178	HSTL (1.5V) mode
Stuff R243 and R177	LVTTL (3.3) mode

4.2.8 R530 - R532: PCI Grant Connections (DC Sh11)

Use these resistors to connect the microprocessor's PCI Grant 0-2 pins to the Yosemite's PCI Grant 0-2 signals. R530-R532 correspond to PCI_GNTB0 – PCI_GNTB2 respectively.

R530 - R532	Function
Open	Microprocessor's PCI Grant pin is not connected to Yosemite's PCI Grant signal
Install	Microprocessor's PCI Grant pin is connected to Yosemite's PCI Grant signal *

4.2.9 R342 - R344: PCI Request Connections (DC Sh11)

Use these resistors to connect the microprocessor's PCI Request 0-2 pins to the Yosemite's PCI Request 0-2 signals. R342 – R344 correspond to PCI_REQB0 – PCI_REQB2 respectively.

R342 – R344	Function
Open	Microprocessor's PCI Request pin is not connected to Yosemite's PCI Request signal
Install	Microprocessor's PCI Request pin is connected to Yosemite's PCI Request signal *

A Schematics and Layout

The schematics (in PDF format) are supplied separately.

The layout files (in Gerber format) are available upon request.

B Bill Of Materials

The bill of materials (text file) is available upon request.

B.1 Build Options

There are a number of components that are populated based on the configuration of the board. The following lists the build options for the various microprocessor board assemblies.

B.1.1 Yosemite Build Options

Serial port option:

- RM922x/RM912x native serial port.
- External DUART.

B.1.2 Half Dome Build Options

Clock Generator:

- PMC-Sierra's CM5391L GEN-M9K-20 clock generator.
- Non-PMC clock generator.

B.1.3 Bridal Veil Build Options

TBD

B.1.4 Mariposa Build Options

TBD

C Programmable Logic Code

The FPGA and CPLD code is available upon request.

D Memory Map

The local bus memory map decoded by local bus FPGA is shown in Table 9.

Table 9 Local Bus Memory Map

Device	Size	Chip Select	Base Address
Flash	4M x 8 or 16M x 8	CS0	0x0
Miscellaneous		CS1	0x0
External DUART	16 x 8	CS2	0x00000000 - 0x00200000
LCD Panel	2 x 8	CS2	0x00600000 – 0x007FFFFF
Parity	1 x 8	CS2	0x00E00000
Watchdog Timer/NVRAM	32K x 8	CS3	0x0000 – 0x7FEF NVRAM 0x7FF0 – 0x7FFF WDTimer

E PCB Board Modifications

E.1 Yosemite Modifications

E.1.1 Revision A

- Reset device U57 rework.
- PHY MDIO/MDC U54 rework.
- External DUART IORD U36 rework.
- Remove Soft Reset switch S3 (not implemented yet).
- Internal vs. External DUART option.

DUART Used	R281, R282, R283, R284 and R301, R302, R303, R304 (on solder side)	R827, R828, R829, R830 and R294, R295, R296, R297 (on component side)
Internal	Install	Do Not Install
External	Do Not Install	Install

E.2 Half Dome Modifications

E.2.1 Revision A

- CK2/CK2# rework on DIMM0 and DIMM1 for unbuffered DDR, registered DDR does not require any rework.
- PMC-Sierra or non-PMC-Sierra clock rework.

E.2.2 Revision B

TBD

E.3 Bridal Veil Modifications

E.3.1 Revision A

TBD

E.4 Mariposa Modifications

E.4.1 Revision A

TBD

F Board Bring-up

PMC-Sierra ships the board assembly with the following set-up:

- The appropriate daughter card is plugged into the main board with standoffs.
- The appropriate DRAM is mounted on the daughter card. Note: If the DRAM is supplied separately, mount it in the DIMM socket, J6, farthest from the CPU.
- Default jumper settings.
- U27 (Main Board) stuffed with the appropriate PMON ROM.
- U29 (Main Board) stuffed with the appropriate Local Bus FPGA download pattern.
- U14 (Daughter Card) stuffed with the appropriate mode bit EEPROM.

Note that PMC-Sierra ships the board after performing a PMON and Linux kernel boot test. A printout of the PMON and Linux kernel boot sequence is included with the board for reference. The board is then left operating the PMON based memory test until shipment.

After unpacking the board, use the following checklist to bring up the board on your bench (assuming default jumper settings and memory configuration):

- Connect the serial port J5 with a null model cable connected to your PC serial port running HyperTerminal or TeraTerm. Set the serial port connection speed to 115K 8-N-1.
- Plug the network cable into the appropriate GE port (ge0: J19, ge1: J20, ge2: J21). Note:
  - The initial boards are shipped with a PMON that fixes the port speed to GE. Unless a GE NIC is installed on your PC, a GE switch must be used to connect to a 10/100 port on the NIC.
  - Newer PMONs auto-detect the port speed. When using these PMONs, connect the Yosemite GE ports to any speed NIC in the PC.
- Make sure the CPU fan is connected to the power source. The board ships with two different type of CPU fan connectors:
  - For HDD-style connectors, connect the CPU fan to the appropriate connector from the power supply.
  - For 3-pin-style connectors, connect the CPU fan to JP1 on the board. (Note the red wire should be attached to the pin 1, the black wire to pin 2, and the yellow wire left unused.)
- Connect the ATX power cable to the board.

Once the board powers-up, the PMON boot messages appear on the serial console. After performing the boot up sequence, the PMON prompt appears.

If you have a connection to a tftp server with a Linux image for the board, you can download Linux over the native GE port, otherwise proceed to your own download sequence.

End of Document